

CAN Transceiver NCV7349 Specification Addendum



ON Semiconductor®

www.onsemi.com

TECHNICAL REPORT

Introduction and Document Scope

This document deals with impact of extended supply range of 4.5 V to 5.5 V (VCC pin) to parametric operation of NCV7349 and also impact to specific Velio system test.

Datasheet Parameters in Extended Range

NCV7349 in datasheet clearly specify power supply conditions for parametric operation in the range from VCC = 4.75 V to 5.25 V. Table 1 in NCV7349 datasheet [1] notes that the functional range of the chip is extended to 4.5 V to 5.5 V.

Absolute Maximum Ratings

The chip absolute maximum ratings as defined in NCV7349 datasheet [1] in Table 4 are not affected by extended supply range conditions from VCC of 4.5 V to 5.5 V.

Thermal Characteristics

The chip thermal characteristics as defined in NCV7349 datasheet [1] in Table 5 are not affected by extended supply range conditions from VCC of 4.5 V to 5.5 V.

ELECTRICAL CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.8 V to 5.5 V (NCV7349-3 only); T_J = -40 to +150°C; R_{LT} = 60 Ω unless specified otherwise. On chip versions without V_{IO} pin, reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO}.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Impact of extended supply range of 4.5 V to 5.5 V on V _{CC} pin
SUPPLY (Pin V_{CC})							
I _{CC}	Supply current	Dominant; V _{TxD} = 0 V Recessive; V _{TxD} = V _{IO}	-	48 6	79 10.5	mA mA	Max value 5% impacted
I _{CCS}	Supply current in standby mode	T _J ≤ 100°C, (Note 1)	-	10	15.75	μA	Max value 5% impacted
V _{UVDVCC}	Undervoltage detection voltage on V _{CC} pin		2	3	4	V	NO IMPACT
SUPPLY (pin V_{IO}) on NCV7349-3 Version Only							
V _{IO}	Supply voltage on pin V _{IO}		2.8	-	5.5	V	NO IMPACT
I _{IOS}	Supply current on pin V _{IO} in standby mode	Standby mode	-	1	-	μA	NO IMPACT
I _{IONM}	Supply current on pin V _{IO} in normal mode	Dominant; V _{TxD} = 0 V Recessive; V _{TxD} = V _{IO}	-	-	1 0.2	mA mA	NO IMPACT
V _{UVDVIO}	Undervoltage detection voltage on V _{IO} pin		1.3	-	2.7	V	NO IMPACT
TRANSMITTER DATA INPUT (Pin TxD)							
V _{IH}	High-level input voltage	Output recessive	2.0	-	V _{IO}	V	NO IMPACT

1. Values based on design and characterization, not tested in production
2. The performance is dominantly defined by the same IP like used in NCV7351 and NCV7342 where supply range is guaranteed and characterized from 4.5 V to 5.5 V

NCV7349–ADD/D

ELECTRICAL CHARACTERISTICS $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.8\text{ V to }5.5\text{ V}$ (NCV7349–3 only); $T_J = -40\text{ to }+150^\circ\text{C}$; $R_{LT} = 60\ \Omega$ unless specified otherwise. On chip versions without V_{IO} pin, reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO} .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Impact of extended supply range of 4.5 V to 5.5 V on V_{CC} pin
--------	-----------	------------	-----	-----	-----	------	---

TRANSMITTER DATA INPUT (Pin TxD)

V_{IL}	Low-level input voltage	Output dominant	-0.3	-	+0.8	V	NO IMPACT
I_{IH}	High-level input current	$V_{TxD} = V_{IO}$	-5	0	+5	μA	NO IMPACT
I_{IL}	Low-level input current	$V_{TxD} = 0\text{ V}$	-75	-200	-350	μA	NO IMPACT
C_i	Input capacitance	(Note 1)	-	5	10	pF	NO IMPACT

TRANSMITTER MODE SELECT (Pin STB)

V_{IH}	High-level input voltage	Standby mode	2.0	-	V_{IO}	V	NO IMPACT
V_{IL}	Low-level input voltage	Normal mode	-0.3	-	+0.8	V	NO IMPACT
I_{IH}	High-level input current	$V_{STB} = V_{IO}$	-5	0	+5	μA	NO IMPACT
I_{IL}	Low-level input current, NCV7349-0	$V_{STB} = 0\text{ V}$	-10	-4	-1	μA	NO IMPACT
I_{IL3}	Low-level input current, NCV7349-3	$V_{STB} = 0\text{ V}$	-40	20	-4	μA	NO IMPACT
C_i	Input capacitance	(Note 1)	-	5	10	pF	NO IMPACT

RECEIVER DATA OUTPUT (Pin RxD)

I_{OH}	High-level output current	Normal mode $V_{RxD} = V_{IO} - 0.4\text{ V}$	-0.1	-0.4	-1	mA	NO IMPACT
I_{OL}	Low-level output current	$V_{RxD} = 0.4\text{ V}$	1.6	6	12	mA	NO IMPACT
V_{OH}	High-level output voltage Weaker RxD pin in Standby mode is on NCV7349-0 version only	Standby mode $I_{RxD} = -100\ \mu\text{A}$	$V_{IO} - 1.1$	$V_{IO} - 0.7$	$V_{IO} - 0.4$	V	NO IMPACT

BUS LINES (Pins CANH and CANL)

$V_{o(\text{reces})}$ (norm)	Recessive bus voltage on pins CANH and CANL	$V_{TxD} = V_{IO}$; no load; normal mode	2.0	2.5	3.0	V	NO IMPACT (Note 2)
$V_{o(\text{reces})}$ (stby)	Recessive bus voltage on pins CANH and CANL	$V_{TxD} = V_{IO}$; no load; standby mode	-100	0	100	mV	NO IMPACT (Note 2)
$I_{o(\text{reces})}$ (CANH)	Recessive output current at pin CANH	$-35\text{ V} < V_{CANH} < +35\text{ V}$; $0\text{ V} < V_{CC} < 5.25\text{ V}$	-2.5	-	+2.5	mA	NO IMPACT (Note 2)
$I_{o(\text{reces})}$ (CANL)	Recessive output current at pin CANL	$-35\text{ V} < V_{CANL} < +35\text{ V}$; $0\text{ V} < V_{CC} < 5.25\text{ V}$	-2.5	-	+2.5	mA	NO IMPACT (Note 2)
$I_{L(\text{CANH})}$	Input leakage current to pin CANH	$0\ \Omega < R(V_{CC}\text{ to GND}) < 1\ \text{M}\Omega$ $V_{CANL} = V_{CANH} = 5\text{ V}$	-10	0	10	μA	NO IMPACT

1. Values based on design and characterization, not tested in production
2. The performance is dominantly defined by the same IP like used in NCV7351 and NCV7342 where supply range is guaranteed and characterized from 4.5 V to 5.5 V

NCV7349–ADD/D

ELECTRICAL CHARACTERISTICS $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.8\text{ V to }5.5\text{ V}$ (NCV7349–3 only); $T_J = -40\text{ to }+150^\circ\text{C}$; $R_{LT} = 60\ \Omega$ unless specified otherwise. On chip versions without V_{IO} pin, reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO} .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Impact of extended supply range of 4.5 V to 5.5 V on V_{CC} pin
BUS LINES (Pins CANH and CANL)							
$I_{L(CANL)}$	Input leakage current to pin CANL	$0\ \Omega < R(V_{CC}\text{ to GND}) < 1\ \text{M}\Omega$ $V_{CANL} = V_{CANH} = 5\ \text{V}$	-10	0	10	μA	NO IMPACT
$V_{o(dom)}(CANH)$	Dominant output voltage at pin CANH	$V_{TxD} = 0\ \text{V}$	2.75	3.5	4.5	V	Valid for: $50\ \Omega < R_{LT} < 65\ \Omega$. Guaranteed by design. Covered by corner simulations. (Limits changed according to ISO11898–2 [2])
$V_{o(dom)}(CANL)$	Dominant output voltage at pin CANL	$V_{TxD} = 0\ \text{V}$	0.5	1.5	2.25	V	Valid for: $50\ \Omega < R_{LT} < 65\ \Omega$. Guaranteed by design. Covered by corner simulations. (Limits changed according to ISO11898–2 [2])
$V_{o(dif)}(bus_dom)$	Differential bus output voltage ($V_{CANH} - V_{CANL}$)	$V_{TxD} = 0\ \text{V}$; dominant; $45\ \Omega < R_{LT} < 65\ \Omega$	1.5	2.25	3.0	V	Valid for: $50\ \Omega < R_{LT} < 65\ \Omega$. Guaranteed by design. Covered by corner simulations. This is fully in line with ISO11898–2 [2] which defines 1.5V minimum level for R_{LT} larger than $50\ \Omega$
$V_{o(dif)}(bus_rec)$	Differential bus output voltage ($V_{CANH} - V_{CANL}$)	$V_{TxD} = V_{IO}$; recessive; no load	-120	0	+50	mV	NO IMPACT (Note 2)
$I_{o(sc)}(CANH)$	Short circuit output current at pin CANH	$V_{CANH} = 0\ \text{V}$; $V_{TxD} = 0\ \text{V}$	-100	-70	-45	mA	Guaranteed by design. Covered by corner simulations.
$I_{o(sc)}(CANL)$	Short circuit output current at pin CANL	$V_{CANL} = 36\ \text{V}$; $V_{TxD} = 0\ \text{V}$	45	70	105	mA	Guaranteed by design. Covered by corner simulations. Max value 5% impacted.
$V_{i(dif)R}(th)$	Differential receiver threshold voltage – Dominant to Recessive	$-2\ \text{V} < V_{CANL} < +7\ \text{V}$; $-2\ \text{V} < V_{CANH} < +7\ \text{V}$;	0.5	0.6	0.7	V	NO IMPACT (Derived from internal reference)
$V_{i(dif)D}(th)$	Differential receiver threshold voltage – Recessive to Dominant	$-2\ \text{V} < V_{CANL} < +7\ \text{V}$; $-2\ \text{V} < V_{CANH} < +7\ \text{V}$;	0.7	0.8	0.9	V	NO IMPACT (Derived from internal reference)
$V_{ihcmR}(dif)(th)$	Differential receiver threshold voltage – Dominant to Recessive	$-35\ \text{V} < V_{CANL} < +35\ \text{V}$; $-35\ \text{V} < V_{CANH} < +35\ \text{V}$;	0.4	–	0.8	V	NO IMPACT (Derived from internal reference)
$V_{ihcmD}(dif)(th)$	Differential receiver threshold voltage – Recessive to Dominant	$-35\ \text{V} < V_{CANL} < +35\ \text{V}$; $-35\ \text{V} < V_{CANH} < +35\ \text{V}$;	0.6	–	1	V	NO IMPACT (Derived from internal reference)
$V_{ihcmD12}(dif)(th)$	Differential receiver threshold voltage – Both transitions	$-12\ \text{V} < V_{CANL} < +12\ \text{V}$; $-12\ \text{V} < V_{CANH} < +12\ \text{V}$;	0.5	–	0.9	V	NO IMPACT (Derived from internal reference)
$V_{i(dif)}(hys)$	Differential receiver input voltage hysteresis	$-2\ \text{V} < V_{CANL} < +7\ \text{V}$; $-2\ \text{V} < V_{CANH} < +7\ \text{V}$;	100	200	300	mV	NO IMPACT (Derived from internal reference)
$V_{i(dif)}(th_STDBY)$	Differential receiver threshold voltage in standby mode	$-12\ \text{V} < V_{CANL} < +12\ \text{V}$; $-12\ \text{V} < V_{CANH} < +12\ \text{V}$;	0.4	0.8	1.15	V	NO IMPACT (Derived from internal reference)

1. Values based on design and characterization, not tested in production
2. The performance is dominantly defined by the same IP like used in NCV7351 and NCV7342 where supply range is guaranteed and characterized from 4.5 V to 5.5 V

NCV7349-ADD/D

ELECTRICAL CHARACTERISTICS $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.8\text{ V to }5.5\text{ V}$ (NCV7349-3 only); $T_J = -40\text{ to }+150^\circ\text{C}$; $R_{LT} = 60\ \Omega$ unless specified otherwise. On chip versions without V_{IO} pin, reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO} .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Impact of extended supply range of 4.5 V to 5.5 V on V_{CC} pin
--------	-----------	------------	-----	-----	-----	------	---

BUS LINES (Pins CANH and CANL)

$R_{i(cm)}$ (CANH)	Common-mode input resistance at pin CANH		15	26	37	k Ω	NO IMPACT
$R_{i(cm)}$ (CANL)	Common-mode input resistance at pin CANL		15	26	37	k Ω	NO IMPACT
$R_{i(cm)}$ (m)	Matching between pin CANH and pin CANL common mode input resistance	$V_{CANH} = V_{CANL}$	-3	0	+3	%	NO IMPACT
$R_{i(dif)}$	Differential input resistance		25	50	75	k Ω	NO IMPACT
$C_{i(CANH)}$	Input capacitance at pin CANH	$V_{TxD} = V_{IO}$; (Note 1)	-	-	30	pF	NO IMPACT
$C_{i(CANL)}$	Input capacitance at pin CANL	$V_{TxD} = V_{IO}$; (Note 1)	-	-	30	pF	NO IMPACT
$C_{i(dif)}$	Differential input capacitance	$V_{TxD} = V_{IO}$; (Note 1)	-	3.75	10	pF	NO IMPACT

THERMAL SHUTDOWN

$T_{J(sd)}$	Shutdown junction temperature	Junction temperature rising	150	170	185	$^\circ\text{C}$	NO IMPACT
-------------	-------------------------------	-----------------------------	-----	-----	-----	------------------	-----------

TIMING CHARACTERISTICS

$t_{d(TxD-BUSon)}$	Delay TxD to bus active	$C_i = 100\text{ pF}$ between CANH to CANL	-	50	-	ns	NA
$t_{d(TxD-BUSoff)}$	Delay TxD to bus inactive	$C_i = 100\text{ pF}$ between CANH to CANL	-	60	-	ns	NA
$t_{d(BUSon-RxD)}$	Delay bus active to RxD	$C_{RxD} = 15\text{ pF}$	-	60	-	ns	NA
$t_{d(BUSoff-RxD)}$	Delay bus inactive to RxD	$C_{RxD} = 15\text{ pF}$	-	60	-	ns	NA
t_{pd}	Propagation delay TxD to RxD (NCV7349-0 version)	$C_i = 100\text{ pF}$ between CANH to CANL	-	125	230 (255)	ns	NO IMPACT in range from 4.75V to 5.5V for max level. Design guaranteed to stay within ISO11898-2 [2] for full extended voltage range from 4.5V. ISO limit in bracket.
	Propagation delay TxD to RxD (NCV7349-3 version)	$C_i = 100\text{ pF}$ between CANH to CANL	-	130	250 (255)	ns	NO IMPACT in range from 4.75V to 5.5V for max level. Design guaranteed to stay within ISO11898-2 [2] for full extended voltage range from 4.5V. ISO limit in bracket.
$t_{d(stb-nm)}$	Delay standby mode to normal mode		5	8	20	μs	Guaranteed by design. Covered by corner simulations. This parameter is not required by ISO11898-2.
t_{wake}	Dominant time for wake-up via bus		0.5	2.5	5	μs	Guaranteed by design. Covered by corner simulations.
$t_{dwakerd}$	Delay to flag wake event (recessive to dominant transitions)	Valid bus wake-up event, $C_{RxD} = 15\text{ pF}$	1	4.5	10	μs	Guaranteed by design. Covered by corner simulations. This parameter is not required by ISO11898-2.

1. Values based on design and characterization, not tested in production

2. The performance is dominantly defined by the same IP like used in NCV7351 and NCV7342 where supply range is guaranteed and characterized from 4.5 V to 5.5 V

NCV7349–ADD/D

ELECTRICAL CHARACTERISTICS $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.8\text{ V to }5.5\text{ V}$ (NCV7349–3 only); $T_J = -40\text{ to }+150^\circ\text{C}$; $R_{LT} = 60\ \Omega$ unless specified otherwise. On chip versions without V_{IO} pin, reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO} .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Impact of extended supply range of 4.5 V to 5.5 V on V_{CC} pin
TIMING CHARACTERISTICS							
$t_{d\text{wakedr}}$	Delay to flag wake event (dominant to recessive transitions)	Valid bus wake-up event, $C_{RxD} = 15\text{ pF}$	0.5	–	7	μs	Guaranteed by design. Covered by corner simulations. This parameter is not required by ISO11898–2.
$t_{\text{wake(RxD)}}$	Minimum pulse width on RxD	$5\ \mu\text{s}$ t_{WAKE} , $C_{RxD} = 15\text{ pF}$	0.5			μs	Guaranteed by design. Covered by corner simulations. This parameter is not required by ISO11898–2.
$t_{\text{dom(TxD)}}$	TxD dominant time for time-out	$V_{TxD} = 0\text{ V}$	1.2	2.6	4	ms	Guaranteed by design. Covered by corner simulations. This parameter is not required by ISO11898–2.

1. Values based on design and characterization, not tested in production
2. The performance is dominantly defined by the same IP like used in NCV7351 and NCV7342 where supply range is guaranteed and characterized from 4.5 V to 5.5 V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Velio Certification

NCV7349 was tested for Velio compliance. This test was provided for 3 power supply options. $V_{CC_min} = 4.75\text{ V}$, $V_{CC_typ} = 5\text{ V}$ and $V_{CC_max} = 5.25\text{ V}$.

In the table below is the summary of the results and assessment on supply range sensitivity.

NCV7349 VELIO EVALUATION SUMMARY

Section	Subject	Criteria			Results			Note
		Min	Max	Unit	Vcc_min	Vcc_typ	Vcc_max	
3.1	Output Differential Capacitance		30	pF	–	20,91	–	No VCC effect
3.2.1	Transceiver Delay							
3.2.1.1	Transmitter Delay (R>D)		140	ns	50,156	47,453	45,188	Negligible VCC effect
3.2.1.2	Transmitter Delay (D>R)		140	ns	57,109	56,219	55,734	Negligible VCC effect
3.2.1.3	Receiver Delay (R>D)		140	ns	74,078	72,078	70,609	Negligible VCC effect
3.2.1.4	Receiver Delay (D>R)		140	ns	72,500	70,891	70,000	Negligible VCC effect
3.3.1	dV/dt characteristic							
3.3.1.1	dV/dt characteristic (D>R), Ron		50	Ω	–	29,82	–	No VCC effect
3.3.1.1	dV/dt characteristic (D>R)	See graph			See graph			
3.3.1.2	dV/dt characteristic (R>D)	See graph			See graph			
3.3.2	R>D Distortion Delay		37	ns	10,779	11,170	11,685	Negligible VCC effect
3.3.3	D>R Distortion Delay		587	ns	146,33	145,154	144,7	Negligible VCC effect
3.4.1	Static response of threshold voltage							
3.4.1.1	$V_{\text{Thresh dom-rec}}$	No judgement			–	–	–	–
3.4.1.2	$V_{\text{Thresh rec-dom}}$	0,7	0,9	V	0.857/ 0.878	0.860/ 0.877	0.861/ 0.877	Negligible VCC effect
3.4.2	Frequency response of threshold voltage	See graph			See graph			Positive VCC effect – Lower VCC → Higher margin
3.5.1	Single Ended S–Parameter S11–S22		0,03	–	–	Max 0.01	–	No VCC effect

NCV7349–ADD/D

Conclusion

NCV7349 can be safely used from 4.5 V to 5.5 V. Most of the parameters are guaranteed as stated in the datasheet. Few CAN parameters have small limitations versus NCV7349 datasheet [1] but still being in accordance with CAN ISO norm [1].

Velio testing performed on the device in the range of 4.75 V to 5.25 V is based on the analysis of the report well extendable to the range of 4.5 V to 5.25 V.

Referenced Documents

1. NCV7349 datasheet, December, 2014 – Rev. 1, www.onsemi.com
2. ISO11898–2, DRAFT international standard, ISO/TC 22/SC 31, 2015, 17th December

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative