CS51021ADEMO/D

Demonstration Note for CS51021A/CS51022A

A 36−72 V In, 5 V/5 A Out, Forward Converter Using the CS51021A/22A Enhanced Current Mode Controller

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DEMONSTRATION NOTE

Description

The CS51021A/22A demo board is configured as a compact, full−featured, 25 W DC−DC convertor for telecom applications. This board incorporates all the circuitry required to fully evaluate the performance of the CS51021A Current Mode PWM Controller. Input is 36 to 72 V and output is 5 V at 5 A. Onboard is a resistive load which can be attached to the supply output at 275 mA, 2.5 A or 5 A load, static or dynamic. Also available is a switch for short circuit to demonstrate overcurrent protection. This load arrangement demonstrates the tight load regulation of the circuit. The DC/DC converter section fits in a 2″ × 2−1/8″ space and includes optoisolation.

Features

- Forward Convertor Topology
- Undervoltage and Overvoltage Shutdown
- Overcurrent Protection
- Current Sense Transformer for Improved Efficiency and Regulation
- Soft Start
- SYNC Function Allows External Switching Clock (CS51021A)
- SLEEP Function Provides ON/OFF Primary Side Power Control (CS51022A)
- Small Size (2″ × 2−1/2″), All Components Surface Mount
- 500 V Input−to−Output Isolation
- 300 kHz Switching Frequency
- Bootstrap Section for Circuit Bias Improves Efficiency

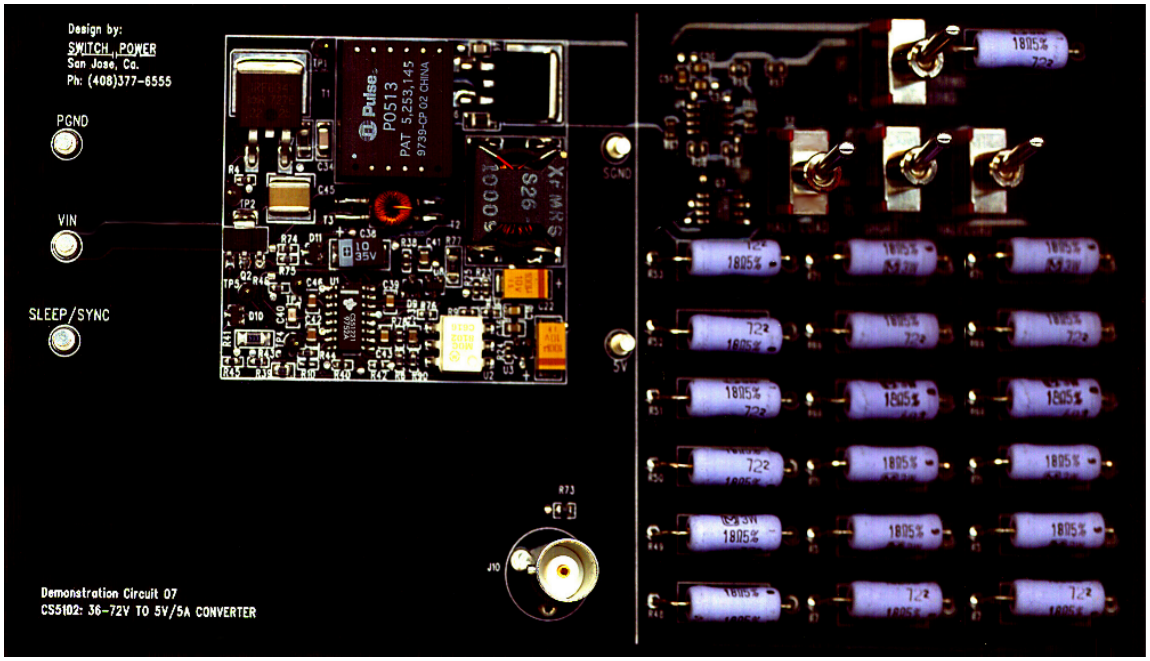

Figure 1. CS51021A/22A Demonstration Board

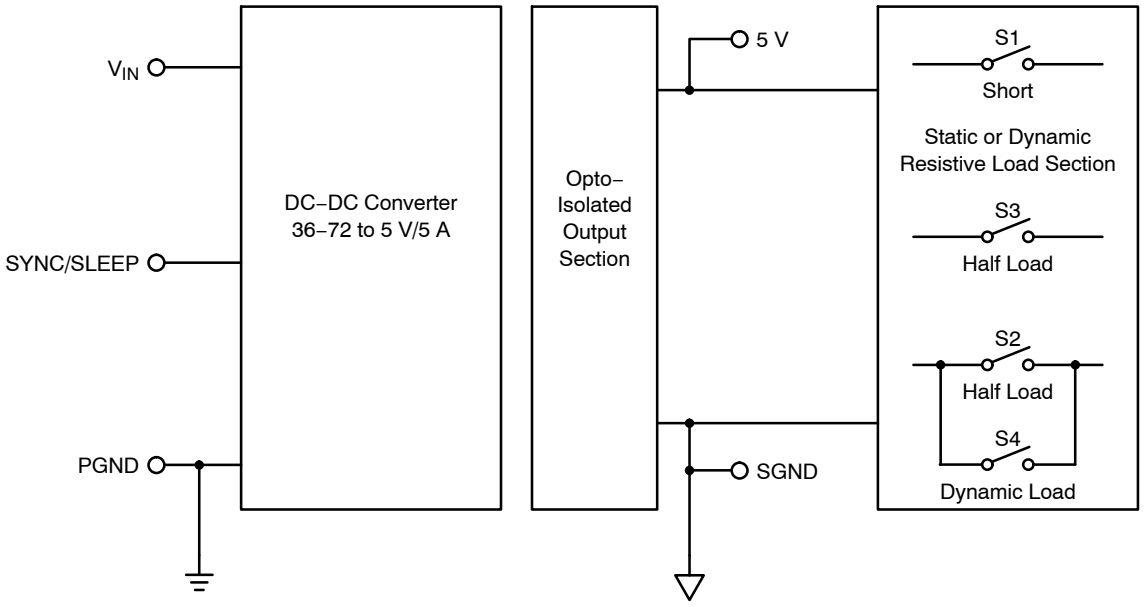

Figure 2. Application Diagram

MAXIMUM RATINGS

Pin Name	Maximum Voltage	Maximum Current
V_{IN}	+100 V/−0.3 V	1.0 A DC
SLEEP/SYNC	+6.0 V/−0.3 V	4.0 mA
PGND	0 V	1.0 A
5 V	6.0 V/−0.3 V	5.0 A
SGND	0 V	5.0 A

ELECTRICAL CHARACTERISTICS ($36 V \le V_{IN} \le 72$ V, I_{OUT} = 275 mA; unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
DC Output Voltage	$0 \le I_{OUT} \le 5.0$ A	4.85	5.00	5.15	V
Switching Frequency	Measure @ R_TC_T	290	330	370	kHz
Load Transient Response	500 mA < I_{LOAD} < 5.0 A 275 mA < I_{LOAD} < 2.5 A	120 35	160 50	220 70	µs µs
Load Regulation	V_{IN} = 48 V, 275 mA < I_{LOAD} < 5.0 A	5.0	10	15	mV
Line Regulation	I_{LOAD} = 5.0 A	10	15	25	mV
Efficiency	V_{OUT} = 5.0 V, I_{OUT} = 5.0 A V_{OUT} = 5.0 V, I_{OUT} = 275 mA	76 35	79 40	82 45	% %
Output Ripple	I_{OUT} = 5.0 A	35	45	55	mV_{P-P}
Power−Up/Soft Start Time	$0 \le I_{OUT} \le 5.0$ A	–	200	–	µs
Isolation	Allowable DC level between input and output	–	500	–	V

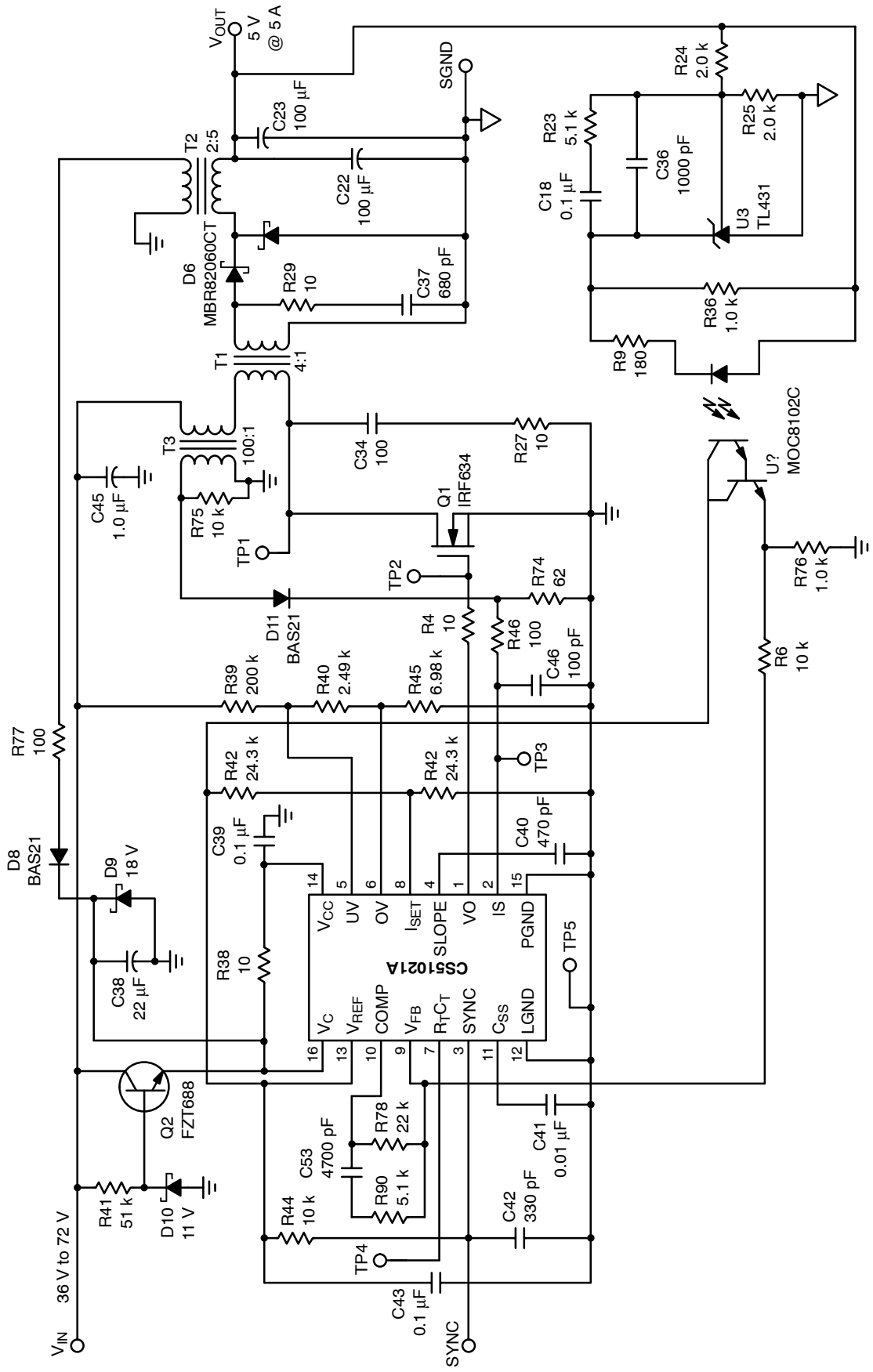

Figure 3. Demonstration Board Schematic, Power Supply Circuitry

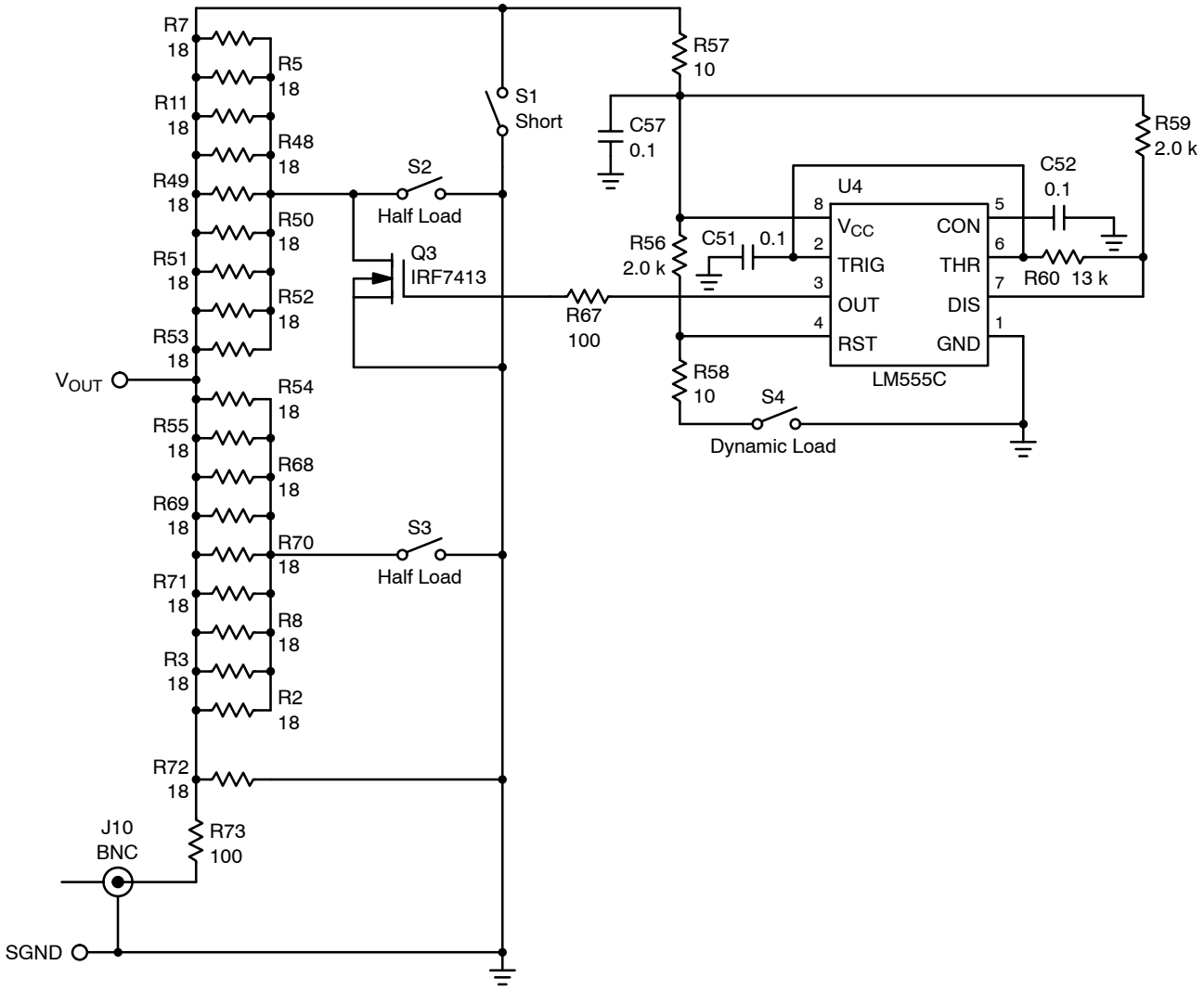

Figure 4. Demonstration Board Schematic, Test Circuitry

OPERATION GUIDELINES

The CS51021A demonstration board is configured to demonstrate the performance features of the CS51021A Current Mode PWM Controller.

- The power supply input connectors, labeled V_{IN} and *PGND*, are the straight turret terminals and are located on the left side of the board. Below the V_{IN} terminal is the SLEEP/SYNC terminal.
- The outputs (+5 V, GND) in the middle, between the DC/DC convertor and load areas.
- The voltage output terminal, *J10*, is a female BNC connector, located near the load resistors. Using a standard BNC coax cable, the output voltage waveform can be observed on an oscilloscope during DC and AC load operation.
- The *Half Load Switches*, *S2* and *S3*, are SPDT type (AMP) and are located on the right side of the board. By turning these switches on, a DC load of 2.5 A is applied for each.
- The *Short Circuit Switch*, *S1*, is a SPDT type (AMP) and is located on the right side of the board. By turning *S1* on, the demo board output is shorted to ground.
- The *Dynamic Load Switch*, *S4*, located on the upper right of the board is used to enable the 555 Timer/FET circuit which is in parallel with *Half Load Switch*, *S2*. When enabled, this switches 2.5 A on and off rapidly. This demonstrates the short reaction time and efficient load handling of the circuit.
- There are five test points in the convertor area; Switching Node, NFET Gate, I_{SENSE} pin, R_TC_T pin (osc.) and GND. These single pin terminals allow easy monitoring of the CS51021A function.

THEORY OF OPERATION

Control Method

The CS51021A is a fixed frequency PWM current mode controller that regulates the output voltage. To perform this task, the controller varies the duration of a current pulse that flows through transformers T1 and T3, and then across T2 to the load. The CS51021A drives FET Q1's gate pin, forcing the FET to switch on and off. Switching the FET creates an AC waveform that is stepped down by T1. The current is proportional to both the output current and the input voltage (V = L[di/dt]) and is used to control the duty cycle of the FET. The current ramp through current sense transformer T3 reaches a level where the controller shuts down the FET, hence the term Current Mode Control. Once the FET switches off, the stored magnetic energy of the transformers produces a current, which is directed through rectifying diodes D6 to produce an output DC voltage. The rectified DC voltage is sensed by the negative input of the controller's error amplifier, at the V_{FB} pin. The error amplifier's output sets the current limit value that will shut down the FET. For example, if the rectified voltage falls below the desired level, the error amplifiers output will increase thereby allowing the duty cycle, inductor current and stored magnetic energy to increase. As a result, a larger amount of current is directed to the rectifier causing the output DC voltage to increase. This process occurs every oscillator clock cycle.

Startup

The CS51021A initially is powered from V_{IN}, with D10 providing regulation and protection. D10 is an 11 V Zener. Dropped down by the V_{BE} of Q2, and the CS51021A sees about 10.3 V at V_C and V_{CC}. As the circuit comes up into operation, the transformer T2 takes over and sources power. C41 is the soft start capacitor. The value of 0.01 μF sets the initial output voltage to ramp up in about 200 μs.

Fault Operation

Output current is tapped at 100:1 transformer T3, then is halfwave rectified by diode D11, then voltage divided by R46 and R74. This point connects to the PWM and Second Threshold comparators via the I_{SENSE} pin. The 75 ns blanking interval is disabled if V_{FB} is below 2 V, as in a short circuit condition. The pulse−by−pulse overcurrent threshold is the level present at the I_{SET} pin. This voltage provides a threshold for both PWM and Second Threshold comparators. When the I_{SENSE} exceeds the second threshold, the soft start capacitor C_{SS} is reset and reinitiates the soft start sequence. This sequence repeats as long as the fault condition is present. The rapid response to overcurrent faults protects the components in the output section as well as the load.

Switching Frequency

For a chosen frequency of 330 kHz, using the R_TC_T graph [Figure 4 in the datasheet (document number CS51021A/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com)], a 10 k resistor with a 330 pF capacitor was found to produce the desired results.

Forward Converter Topology

Advantages:

- High Efficiency
- Small output filter
- Low output ripple
- Isolation between input and output

Disadvantages:

- Only one monitored output possible
- The output voltage is always lower than the input voltage (step−down)

DESIGN NOTE

Design of a Forward Converter Using the CS51022A Enhanced PWM Controller

Specifications

V_{IN} = 36 V to 72 V
V_{OUT} = 5 V ± 5% @ 0.5 A to 5 A
V_{OUT} Ripple ≤ 50 mA
Switching Frequency = 330 kHz

We begin the design on the secondary side by selecting the minimum voltage required to keep the output voltage in regulation. Worst case is at minimum input voltage, 36 V.

$$V_{SEC(min)} = \frac{V_{OUT} + V_D}{D_{max}}$$

Since the CS51022A includes slope compensation circuitry, we can choose the maximum duty cycle at 0.65.

$$V_{SEC(min)} = \frac{5\ V + 0.5\ V}{0.65\ V} = 8.46\ V$$

The transformer turns ration is:

$$n = \frac{V_{IN(min)}}{V_{SEC(min)}} = \frac{36}{8.46} = 4.25 \approx 4:1$$

Based on a turns ratio of 4:1 the maximum duty cycle at low line is:

$$D_{max} = \frac{5\ V + 0.5\ V}{36} \times 4 = 0.61$$

$$D_{min} = D_{max} \times \frac{36}{72} = 0.30$$

The transformer is designed using the basic transformer equation:

$$B_S \times n \times A_e > V_{IN} \times t_{ON}$$

where:
B_S = core saturation flux density in Tesla;
n = number of primary turns;
A_e = core cross sectional area in meters^2;
V_{IN} = the voltage applied to the core in volts;
t_{ON} = the maximum time for which the voltage is applied in μs.

The core selection is an iterative process and usually involves several attempts. This paper shows the attempt that worked.

Using a transformer design kit from Coiltronics Inc., we use the EFT 15 core. For the EFD 15:
A_L, nH/T^2 (ungapped) = 780
A_e, (min core area) mm^2 = 15
V_e, (core volume) mm^3 = 510
For this design f_{SW} = 320 kHz.

$$t_{ON(max)} = \frac{D_{max}}{f_{SW}} = \frac{0.65}{320\ kHz} = 2.03\ \mu s$$

Rearranging the transformer equation:

$$B_S \times n \times A_e > V_{IN} \times t_{ON}$$

$$n = \frac{V_{IN} \times t_{ON}}{B_S \times A_e}$$

$$= \frac{36\ V \times 2.03\ \mu s}{0.3\ T \times 0.0015} = \frac{7.3 \times 10^{-5}}{4.5 \times 10^{-6}} = 16.22$$

We use 16 primary turns.
For 3F3 material, A_L = 780 nH/T^2 or 0.78 μH/T^2.
The maximum inductance is:

$$L = 16^2 \times 0.78\ \mu H = 200\ \mu H$$

Allowing for a 20% range in inductance value gives:

$$L = 200\ \mu H \pm 20\% = 160\ \mu H \text{ to } 240\ \mu H$$

We use 28 AWG wire with one strand on the primary side and three strands on the secondary. The primary and secondary windings are interleaved to minimize leakage inductance.

Output Inductor Calculation

$I_{OUT(min)}$ = 0.5 A
The inductor is designed so that the current remains continuous within the specified load range.

$$\Delta I_L = 2 \times I_{OUT(min)} = 2 \times 0.5\ A = 1\ A$$

The minimum duty cycle is 0.3 so the maximum off–time is:

$$t_{OFF(max)} = \frac{1 - 0.3}{320\ kHz} = \frac{0.7}{320\ kHz} = 2.18\ \mu s$$

Minimum inductor value is:

$$L_{min} = \frac{(V_{OUT} + V_D) \times t_{OFF(max)}}{\Delta I}$$

$$= \frac{(5\ V + 0.5V) \times 2.18 \times 10^{-6}}{1} = 12\ \mu H$$

The maximum inductor current is approximately:

$$I_{L(max)} = 1.2 \times I_{OUT} + \frac{\Delta I}{2} = 6.5\ A$$

The inductor is designed using the basic inductor equation:

$$B_S \times n \times A_e > L \times I_{L(max)}$$

Rearranging gives

$$n = \frac{L \times I_{L(max)}}{B_S \times A_e}$$

where:
B_S = core saturation flux density in Tesla;
n = number of primary turns;
A_e = core cross sectional area in meters^2;
L = the required inductance in μH;
$I_{L(max)}$ = the maximum inductor current in Amps.

Using a Micrometals T50−26B core where:
A_e = 1.48 cm^2 or 0.0000148 m^2
A_L = 43.5 nH/T^2 or 0.0435 μH/T^2

$$n = \frac{12 \times 10^{-6} \times 6.5}{0.3 \times 0.148 \times 10^{-4}} = 17.56$$

With n = 18 the inductance measures 19 μH.

In addition to the acting as the output inductor we can use a flyback winding to generate the supply voltage for the control IC. The voltage across the inductor is approximately 5.5 V (V_{OUT} + V_D).

The turns ratio is chosen from the formula:

$$V_{CC} = \frac{N_S}{N_P} \times (V_{OUT} + V_D) - V_D$$

For a secondary voltage of approximately 13 volts this gives a 2.5 turns ratio so the flyback winding has 45 turns.

Output Capacitor Calculation

The output capacitor value depends on the following:

1. Maximum allowable ripple;
2. Maximum allowable voltage overshoot and undershoot on load transients.

The capacitor is calculated from:

$$C_{OUT} = \frac{\Delta I}{8 \times f_{SW} \times \Delta V_{OUT}}$$

$$= \frac{0.5}{8 \times 320 \times 10^3 \times 50\ mV} = 3.9\ \mu F$$

The maximum ESR of the output capacitor is given by:

$$ESR = \frac{\Delta V_{OUT}}{\Delta I} = \frac{50\ mV}{500\ mA} = 100\ m\Omega$$

A suitable safety margin is added to the values just calculated, one recommendation is that the output capacitor should be at least ten times the minimum value calculated the the ESR should be at least half of the calculated value.

A capacitor that meets the ESR requirements usually also easily meets the minimum capacitance requirements. In this design we use two 100 μF Tantalum capacitors with a maximum ESR = 100 mΩ in parallel.

Slope Compensation

The slope of the compensating ramp should be at least 50% of the down slope of the output inductor current as seen from the primary side.

In a current mode control scheme such as this, the compensating ramp can be either added to the primary current sense signal or subtracted from the error amplifier voltage.

In this case we will add the ramp to the current sense signal.

Steps for Slope Compensation

1. Calculate the inductor current downslope on the secondary side.

$$\text{Secondary Slope} = \frac{\Delta I}{\Delta t} = \frac{V_{OUT}}{L}$$

$$= \frac{5.5\ V}{12\ \mu H} = 0.45\ A/\mu s$$

2. Calculate the slope as seen from the primary side.

$$\text{Primary Slope} = \text{Secondary Slope} \times \frac{N_S}{N_P}$$

$$= 0.45 \times \frac{1}{4} = 0.114\ A/\mu s$$

3. Calculate the slope voltage at the current sense resistor.
4. The amount of slope compensation is chosen at 0.55:

$$S = 0.071\ V/\mu s \times 0.55 = 0.031\ V/\mu s$$

$$V_{Slope} = \frac{\text{Secondary Slope}}{n} \times R_{Sense}$$

$$= \frac{0.114}{100} \times 50 = 0.057\ V/\mu s$$

5. The voltage on the slope pin is divided by 10 and added to the voltage at the I_S pin. The voltage at the slope pin is 10 times the required slope compensation voltage.

$$V_{Slope} = 0.031\ V/\mu s \times 10 = 0.31\ V/\mu s$$

The slope compensation capacitor is chosen from:

$$C_S = \frac{50\ \mu A \times t_{ON(max)}}{V_{Slope}}$$

$$= \frac{50\ \mu A \times 2.03\ \mu s}{0.31} = 320\ pF$$

Current Sense Transformer Selection

The circuit uses a current sense transformer to sense the primary current. The total primary current is the sum of the magnetizing current and the reflected secondary current.

Magnetizing current:

$$I_{Mag} = \frac{V_{IN} \times t_{ON}}{L} = \frac{36\ V \times 2.03\ \mu s}{200\ \mu H} = 0.365\ A$$

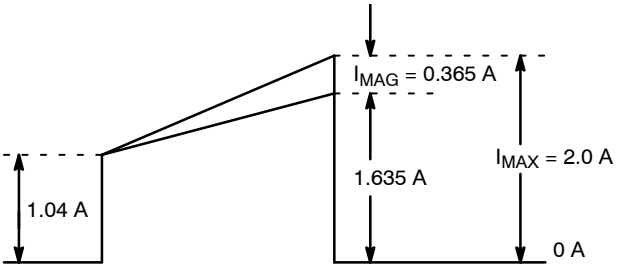

Figure 5. Primary Current Waveform

$$I_{Primary} = \frac{I_{L(max)}}{n} + I_{Mag} = \frac{6.5}{4} + 0.365 = 2\ A$$

Several transformer manufacturers make current transformers with turns ratios of 50:1, 100:1 and 200:1. In this design we use a 100:1 turns ratio transformer manufactured by GB International (part number 3714−G). With a primary current of approximately 2 A peak, the second current will be:

$$I_{Secondary} = \frac{I_{Primary}}{n} = \frac{2\ A}{100} = 20\ mA$$

The voltage required at the I_S pin is determined by the voltage at the I_{SET} pin. This voltage is set up with a voltage divider from V_{REF}.

The overcurrent threshold is given by:

$$V_{I(S)} = 0.8 \times V_{I(SET)} + 0.1\ V + 0.1 \times V_{Slope}$$

where:

$V_{I(SET)}$ = Voltage at the I_{SET} pin;

V_{Slope} = Voltage at the Slope Pin.

The second overcurrent threshold, (the point where the control IC initiates a soft start) is 1.33 times the pulse−by−pulse threshold.

$$V_{I(S)}(2) = 1.33 \times (0.8 \times V_{I(SET)} + 0.1\ V + 0.1 \times V_{Slope})$$

If we arbitrarily choose the maximum voltage on the I_S pin as 1 V during normal operation, we can calculate the required voltage on the I_{SET} pin ($V_{I(SET)}$) from:

$$V_{I(SET)} = \frac{(V_{I(S)} - 0.1\ V - (0.1 \times V_{Slope}))}{0.8}$$

$$= \frac{(1 - 0.1\ V - (0.1 \times 0.46))}{0.8} = 1.07\ V$$

Resistors R24 and R43 set $V_{I(SET)}$ = 1.1 V.

The pulse−by−pulse current limit voltage is 1 V. The current in the secondary winding of the current sense transformer is 20 mA, so the resistor to convert this to the required voltage is:

$$R_{Sense} = \frac{1.0\ V}{20\ mA} = 50\ \Omega$$

Voltage Monitor

The CS51022A has voltage monitoring circuitry for both overvoltage and undervoltage conditions. When the voltage on the OV pin exceeds 2.5 V, an overvoltage condition is detected and VO is disabled in a low impedance state.

If the voltage on the UV pin drops below 1.5 V, VO is also disabled in a low impedance state. Both UV and OV conditions are latched and the CS51022A goes through a power−up sequence. The undervoltage lockout circuitry has a fixed 75 mV of hysteresis. The overvoltage circuitry has programmable hysteresis.

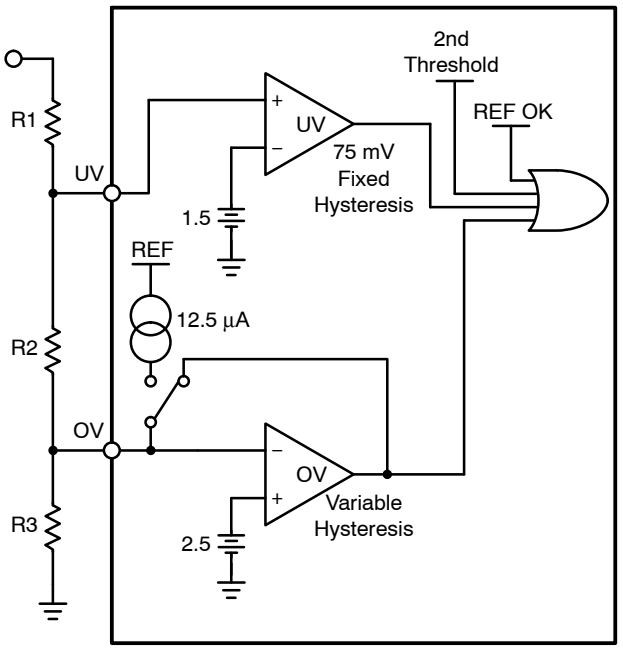

Figure 6. Voltage Monitoring Circuitry from the CS51022A

The amount of overvoltage hysteresis is determined by R3. The internal 12.5 μA current source turns on in an overvoltage condition and adds current to the resistor string raising the voltage on the OV pin. The input voltage must then drop low enough to bring the voltage on the OV pin below 2.5 V (the internal reference) before the CS51022A will resume operation.

In this case we design for:

$V_{OV(Hyst)} = 12.5\ mA \times R3$

$V_{IN(max)} = 75\ V$

$V_{IN(min)} = 34\ V$

Overvoltage Hysteresis = 2.75 V

R3 is calculated from:

$$R3 = \frac{V_{OV(Hyst)} \times 2.5\ V}{V_{IN(max)} \times 12.5\ \mu A} = \frac{2.75 \times 2.5\ V}{75 \times 12.5\ \mu A} = 7.33\ k\Omega$$

The total resistance of the divider is given by:

$$R_{Total} = \frac{V_{IN(max)} \times R3}{2.5\ V} = \frac{75\ V \times 7.33}{2.5\ V} = 220\ k\Omega$$

R2 is calculated based on $V_{IN(min)}$:

$$R2 = \frac{1.5\ V \times R_{Total}}{V_{IN(min)}} - R3$$

$$= \frac{1.5\ V \times 220\ k\Omega}{34\ V} - 7.33\ k\Omega = 2.37\ k\Omega$$

$$R1 = R_{Total} - R2 - R3$$

$$= 220\ k\Omega - 7.33\ k\Omega - 2.73\ k\Omega = 210.3\ k\Omega$$

The resistors used were 210 kΩ, 7.32 kΩ and 2.37 kΩ. The undervoltage hysteresis is given by:

$$\text{Undervoltage Hysteresis} = \frac{V_{IN(min)} \times 75\ mV}{1.5\ V}$$
$$= \frac{34 \times 75\ mV}{1.5\ V} = 1.7\ V$$

Timing Components

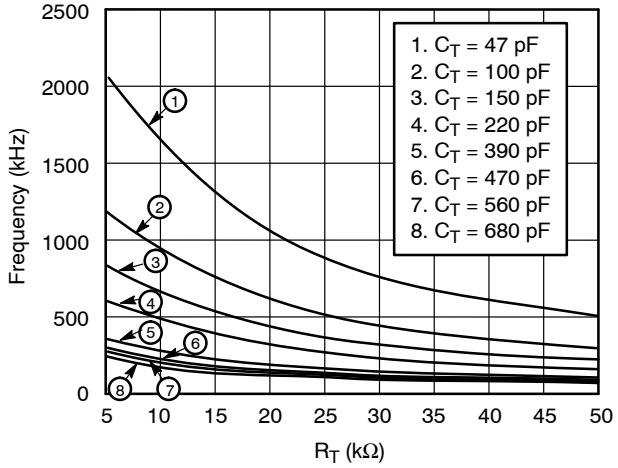

Figure 7. Frequency vs. R_T for Discrete Capacitor Values

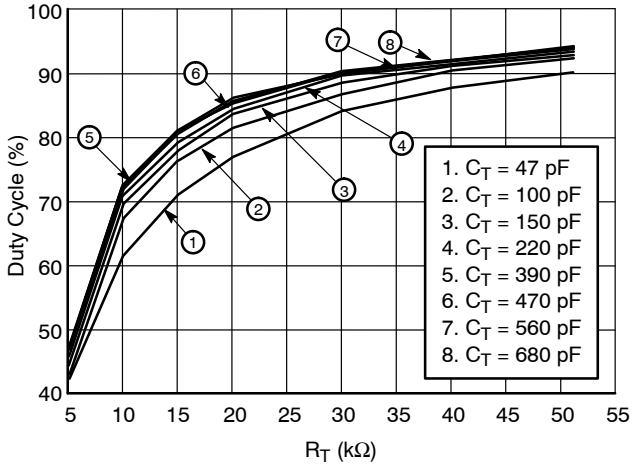

Figure 8. Duty Cycle vs. R_T for Discrete Capacitor Values

Method to select timing components is to use the graphs from the data sheet.

Soft Start

During power up when the output capacitors are completely discharged, the voltage across the soft start capacitor, V_{SS}, controls the duty cycle. The soft start capacitor, C_{SS}, is charged by an internal 50 μA current source. The error amplifier output voltage is clamped to V_{SS}. As V_{SS} continues to rise above the error amplifier output voltage, the feedback loop takes control of the duty cycle. The capacitor charges and discharges between 0.25 V and 4.3 V. In the event of an overcurrent condition, C_{SS} is discharged by a 250 μA current sink circuit, and a soft start cycle begins.

The soft start time is calculated from:

$$C_{SS} = \frac{t_{SS}}{9 \times 10^4}$$

For a 10 ms soft start time:

$$C_{SS} = \frac{10\ ms}{9 \times 10^4} = 0.01\ \mu F$$

Feedback Loop Design

1. Measure, model or calculate the control to output gain.
2. Choose the crossover frequency or the loop bandwidth. The transient response time will be roughly the reciprocal of the bandwidth.
3. Design the error amplifier to have a gain that is the inverse of the control to output gain at the chosen crossover frequency.

As with most industry standard current mode control ICs, the CS51022A has an internal divide by three network on the output of the error amplifier. Current to voltage conversion is done externally with a resistor, R_S, as described previously. The peak voltage across the sense resistor is given by:

$$I_{Peak} = \frac{V_C}{3 \times R_S}$$

where V_C is the control voltage (the error amplifier output voltage).

In this design we are not sensing the output current directly, we sense the reflected output current on the primary side and we also sense it through a current sense transformer.

The equation is modified by the turns ratio of each transformer and becomes:

$$I_{Peak} = \frac{V_C \times n_{T1} \times n_{T3}}{3 \times R_S}$$

The output voltage is given by:

$$V_{OUT} = I_{Load} \times R_{Load}$$

The control voltage, V_C, controls the output current. Combining the equations we get:

$$V_{OUT} = \frac{V_C \times n_{T1} \times n_{T3}}{3 \times R_S} \times R_{Load}$$

So the control to output gain is:

$$\frac{V_{OUT}}{V_C} = \frac{n_{T1} \times n_{T3}}{3 \times R_S} \times R_{Load}$$

The maximum and minimum loads are:

$$R_{Load(min)} = \frac{5\ V}{5\ A} = 1\ \Omega$$

$$R_{Load(max)} = \frac{5\ V}{0.5\ A} = 10\ \Omega$$

The load poles varies between:

$$f_{P(min)} = \frac{1}{2 \times \pi \times R_{Load(max)} \times C_{OUT}}$$

$$= \frac{1}{2 \times \pi \times 10\ \Omega \times 200\ \mu f} = 79.6\ Hz$$

$$f_{P(max)} = \frac{1}{2 \times \pi \times R_{Load(min)} \times C_{OUT}}$$

$$= \frac{1}{2 \times \pi \times 1\ \Omega \times 200\ \mu f} = 796\ Hz$$

The Zero due to the output capacitor ESR (max) is:

$$f_Z = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

$$= \frac{1}{2 \times \pi \times 50\ m\Omega \times 200\ \mu f} = 15.9\ kHz$$

The Zero due to the output capacitor ESR (min) is:

$$f_Z = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

$$= \frac{1}{2 \times \pi \times 25\ m\Omega \times 200\ \mu f} = 31.83\ kHz$$

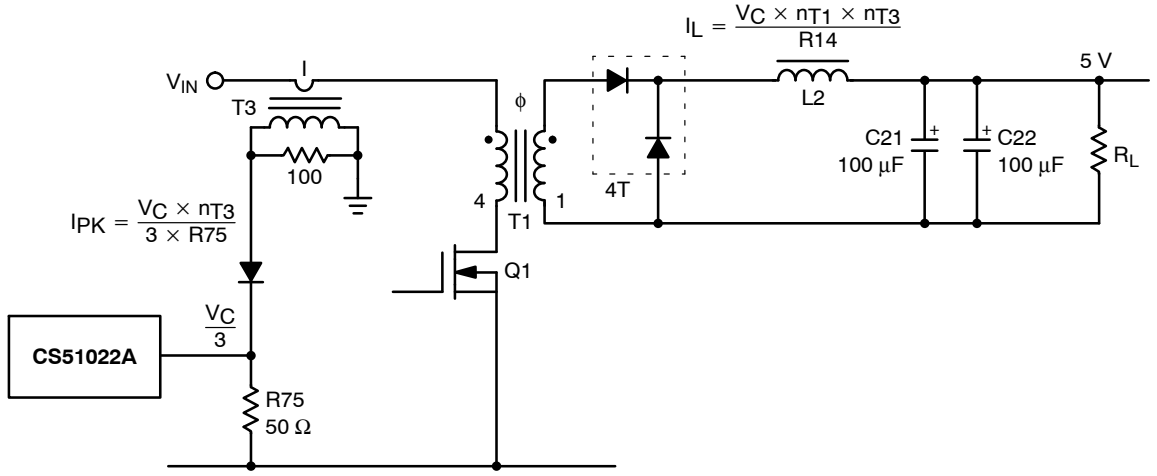

Figure 9. Control to Output Section of a Typical Forward Converter

The control to output gain for the maximum and minimum loads are:

$$\frac{V_{OUT}}{V_C} = \frac{n_{T1} \times n_{T3}}{3 \times R_S} \times R_{Load(max)}$$

$$= \frac{4 \times 100}{3 \times 50} \times 1 = 2.66\ (8.5\ dB)$$

$$\frac{V_{OUT}}{V_C} = \frac{n_{T1} \times n_{T3}}{3 \times R_S} \times R_{Load(max)}$$

$$= \frac{4 \times 100}{3 \times 50} \times 10 = 26.6\ (28.5\ dB)$$

The crossover frequency must now be selected. It is always a compromise between wanting to have as large a bandwidth as possible for the best transient response and wishing to keep it small enough to filter out the switching frequency ripple.

For this design we choose a crossover frequency of 60 kHz.

The required loop gain to cross at 60 kHz is:

$$Gain = 20 \log \frac{60\ kHz}{79.6\ Hz} - 28.5\ dB = 29\ dB\ (28)$$

The feedback loop is isolated from the primary by using an optocoupler. The error amplifier on the secondary side is the industry standard voltage reference circuit, the TL431. If the output voltage drops below its nominal value, the current through the LED decreases. This causes the emitter voltage of the phototransistor to decrease. This results in a higher error signal and a corresponding increase in the duty cycle.

The gain to cross at 60 kHz can be added anywhere in the feedback loop, i.e., it can be all at the optocoupler or divided between the optocoupler and the error amplifier. In this design we will divide the gain between both.

1. Choose the feedback resistors. In this case R24 and R25 = 2 kΩ so the current through the divider network is 1.25 mA. The optocoupler LED bias current is set for 6 mA.

$$R_{Bias} = \frac{5\ V - (2.5\ V + 1.4\ V)}{I_{Bias}} = \frac{1.8}{6\ mA} = 180\ \Omega$$

2. The gain of the TL431 is set by resistors R23 and R24. For a gain of 8 dB:

$$\frac{R24}{R23} = \frac{5.1\ k\Omega}{2\ k\Omega} = 2.55 = 8\ dB$$

3. The optocoupler gain is set by R36 and by R76 on the primary side.

$$Gain = \frac{R76}{R36} \times CTR = \frac{900\ \Omega}{180} = 5\ (13.9\ dB)$$

4. We set a zero in the feedback loop at the TL431 to offset the first load pole that occurs at 79 Hz.

$$C18 = \frac{1}{2 \times \pi \times R23 \times fp} = \frac{1}{2 \times \pi \times 5.1\ k\Omega \times 79\ Hz}$$

$$= 0.39\ \mu F,\ \text{use } 0.33\ \mu F$$

5. On the secondary side we first set the gain of the error amplifier to get the required loop gain.

$$29\ dB - 8\ dB - 13.9\ dB = 7\ dB\ (2.16)$$

Choosing R6 = 10 kΩ gives R78 = 22 kΩ.

6. The error amplifier has a pole zero network to adjust the gain at higher frequencies. At DC the gain is determined by the ratio of R78 and R6 while at higher frequencies the gain is determined by the ratio of R90 and R6. If we place the pole at 1 kHz, and reduce the gain by a factor of four after the zero this means that C53 is:

$$C53 = \frac{1}{2 \times \pi \times (R78 + R90) \times fp}$$

$$= \frac{1}{2 \times \pi \times 27.1\ k\Omega \times 1\ kHz}$$

$$= 5.8\ nF,\ \text{use } 4.7\ nF$$

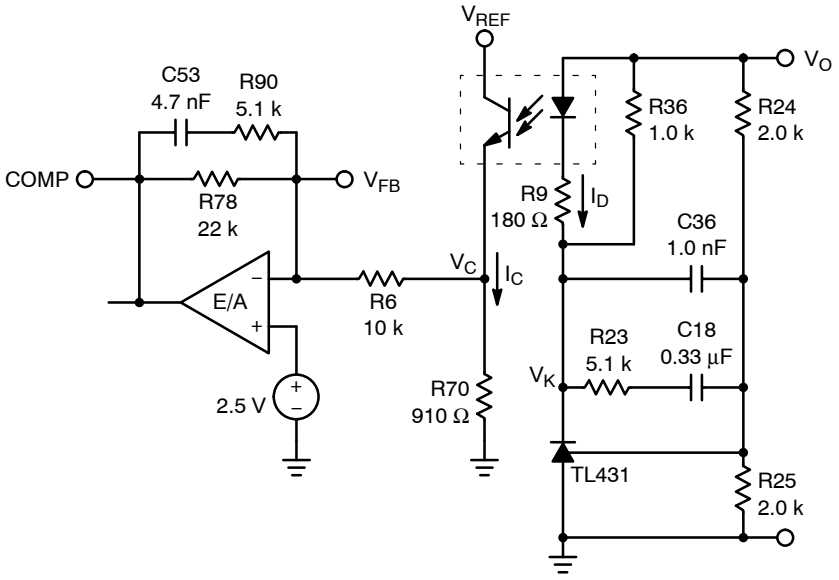

Figure 10. Error Amplifier Feedback with Optocoupler

The zero frequency is given by:

$$fZ = \frac{1}{2 \times \pi \times R90 \times C53}$$

$$= \frac{1}{2 \times \pi \times 5.1\ k\Omega \times 4.7\ nF} = 6.6\ kHz$$

We also need a pole to cancel the zero due to the ESR of the output capacitors.

$$C36 = \frac{1}{2 \times \pi \times R23 \times fp}$$

$$= \frac{1}{2 \times \pi \times 5.1\ k\Omega \times 31\ kHz} = 1\ nF$$

Leading Edge Blanking

A common problem in current mode control is erratic operation due to noise on the current sense input. The main source of this noise is the leading edge noise caused by the transformer interwinding capacitance. The CS51022A contains leading edge blanking circuitry that ignores the first 50 ns (typical) of each current sense pulse and should help eliminate the customary RC filter in the I_S pin. This did not prove to be the case in this design and a small RC filter was required to add an additional 10 ns of delay.

Startup and Bias Circuit

The circuit in Figure 11 is a simple linear regulator bootstrap circuit that supplies start−up current. When the supply is operational the emitter base junction is reverse biased and operating current is supplied from the flyback winding on the output inductor. D9 provides overvoltage protection.

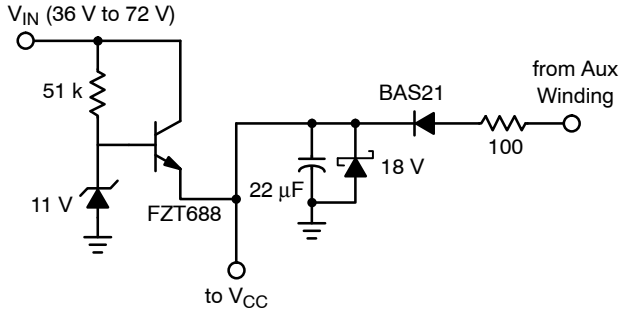

Figure 11. Startup Supply

Resonant Reset

The circuit uses a resonant reset capacitor instead of the more traditional reset winding. This technique uses the resonance between the magnetizing inductance of the transformer and the total capacitance as seen by the transformer. The parasitic capacitance is difficult to measure so the main reset capacitor was chosen by experiment.

$$f_R = \frac{1}{2 \times \pi \times \sqrt{L_M \times C_R}}$$

where:

$$C_R = C_O + C_{OSS} + C_T + n^2 \times C_B$$

C_O = resonant capacitor;
C_{OSS} = junction capacitance of the power switch;
C_B = junction capacitance of the Schottky diode.

DEMONSTRATION BOARD BILL OF MATERIALS

Qty	Ref. Des.	Description	Pkg.	Manufacturer	Manuf. P/N	Phone	Fax
DC/DC Converter							
2	C22, C23	100 μF, 10 V Tant	7343	KOA	TMC1AE1A−D107MLRH	714−751−1185	714−432−7365
1	C34	100 pF, 500 V NPO	1206	Novacap	−	805−295−5920	805−295−5928
1	C36	1000 pF, X7R	805	Novacap	−	805−295−5920	805−295−5928
1	C38	22 μF, 35 V Tant	7343	KOA	TMC1VE1A−D226MLRH	714−751−1185	714−432−7365
3	C18, C29, C43	0.1 μF	805	Novacap	−	805−295−5920	805−295−5928
1	C40	470 pF	805	Novacap	−	805−295−5920	805−295−5928
1	C41	0.01 μF X7R	805	Novacap	−	805−295−5920	805−295−5928
1	C42	330 pF	805	Novacap	−	805−295−5920	805−295−5928
1	C45	1.0 μF	1825	Novacap	−	805−295−5920	805−295−5928
1	C46	100 pF	805	Novacap	−	805−295−5920	805−295−5928
1	C37	680 pF, 100 V	805	Novacap	−	805−295−5920	805−295−5928
1	C53	4700 pF X7R	805	Novacap	−	805−295−5920	805−295−5928
1	D10	11 V Zener	SOT−23	CENTRAL	CMPZ4241B	516−435−1110	516−435−1824
1	D6	2− 60 V Schottkys	DPAK1	ON Semiconductor	MBRB2060CT		
2	D8, D11	G.P. Diode, 250 V	SOT−23	DIODES	BAS21	−	−
1	D9	18 V Zener	SOT−23	CENTRAL	CMPZ5248B	516−435−1110	516−435−1824
1	Q1	MOS Pwr FET	DPAK1	IR	IRF634S	−	−
1	Q2	NPN Bipolar	SOT−223	CENTRAL	CZT3019	516−435−1110	516−435−1824
1	R23, R90	5.1 k, 5%	603	KOA	RM73B1J512J	714−751−1185	714−432−7365
2	R24, R25	2.0 k, 1%	603	KOA	RK73H1JT2001F	714−751−1185	714−432−7365
2	R27, R29	10 Ω, 5%	1206	KOA	RM73B2T100J	714−751−1185	714−432−7365
2	R36, R76	1.0 k, 5%	603	KOA	RM73B1JT102J	714−751−1185	714−432−7365
1	R39	200 k, 1%	805	KOA	RK73H2AT2003F	714−751−1185	714−432−7365
1	R38	10 Ω, 5%	603	KOA	RM73B1JT100J	714−751−1185	714−432−7365
1	R40	2.49 k, 1%	603	KOA	RK73H1JT2491F	714−751−1185	714−432−7365
1	R41	51 k, 5%	1206	KOA	RM73B2BT513J	714−751−1185	714−432−7365

DEMONSTRATION BOARD BILL OF MATERIALS (continued)

Qty	Ref. Des.	Description	Pkg.	Manufacturer	Manuf. P/N	Phone	Fax
DC/DC Converter							
1	R42	24.3 k, 1%	603	KOA	RK73H1JT2432F	714−751−1185	714−432−7365
2	R43, R45	6.98 k, 1%	603	KOA	RK73H1JT6981F	714−751−1185	714−432−7365
1	R46	100 Ω, 5%	603	KOA	RM73B1JT101J	714−751−1185	714−432−7365
3	R6, R44, R75	10 k, 5%	603	KOA	RM73B1JT103J	714−751−1185	714−432−7365
1	R74	62 Ω, 5%	603	KOA	RM73B1JT181J	714−751−1185	714−432−7365
1	R77	100 Ω, 5%	1206	Panasonic	ERJ8GEYJ101V	−	−
1	R78	22 k, 5%	603	KOA	RM73B1JT223J	714−751−1185	714−432−7365
1	R9	180 Ω, 5%	603	KOA	RM73B1JT181J	714−751−1185	714−432−7365
1	T1	25 W Pwr. Xfmr. 4:1	−	Pulse Engineering	P0513	−	−
1	T2	8 μH coil w/overwind, 100:1	−	XFRMS/spi	S26−10009	−	−
1	T3	I_{SENSE} Xfmr, 2:5	−	GB Int'l	2405−J	607−785−938	607−785−1109
1	U1	CS51021AD16	SO−16	ON Semiconductor	CS51021AD16		
1	U2	Optocoupler	SO−6	ON Semiconductor	MOC8102S		
1	U3	Adjustable Reference	SOT−23	Zetex	ZR431FCT	−	−
Test Components							
5	TP1−TP5	1 Pin Header/Test Point	−	Winpoint	201−01−S−3−02−T	−	−
1	J10	BNC Connector	BNC	Digi−Key	DKARKF1066ND	218−681−6674	218−681−3380
5	J1−J3, J5, J9	Turret Terminal	Turret	MillMax	2501−1−00−44−00−00−07−0	−	
1	U4	LM555 Timer	SO−8	National Semi	LM555	−	
19	R2, R3, R5, R7, R8, R11, R48−R55	18 Ω, 5%, 3 W Wirewound	3W	KOA	SPR3180J	−	
4	S1−S4	SPDT Toggle	−	C&K	7101SDGCQE	617−527−6400	617−527−3062
1	Q3	MOSFET, 0.011 mΩ	SO−8	Int'l Rectifier	IRF7413	−	−
2	R57, R58	10 Ω, 5%	0805	Panasonic	ERJ6GEY100V	−	−
2	R56, R59	2.0 k, 5%	0805	KOA	RM73B2AT202J	714−751−1185	714−432−7365
1	R60	13 k, 5%	0805	KOA	RM73B2AT133J	714−751−1185	714−432−7365
3	C50−C52	0.1 μF, 25 V x7r cap	0805	Novacap	−	805−295−5920	805−295−5928

RESULTS AND WAVEFORMS

EFFICIENCY MEASUREMENTS

V_{IN}	I_{IN}	V_{OUT}	I_{OUT}	Efficiency
50	0.095	4.99	0.5	52%
50	0.319	4.986	2.5	78%
50	0.621	4.983	5.0	80%
65	0.079	4.988	0.5	48.6%
65	0.251	4.982	2.5	76.3%
65	0.478	4.98	5.0	80.1%

THERMAL DATA: BOARD UNDER LOAD*

T_A = 23°C	I_{LOAD} = 75 mA V_{IN} = 48 V	I_{LOAD} = 5.0 A V_{IN} = 36 V	I_{LOAD} = 5.0 A V_{IN} = 72 V
T1	50°C	98°C	102°C
T2	31°C	102°C	103°C
T3	38°C	66°C	74°C
Q1 (IRF634)	35°C	76°C	75°C
D6 (MBR82060CT)	33°C	114°C	112°C
U1 (CS51021A)	35°C	55°C	55°C
C38	35°C	61°C	61°C

*Board should only be run with dynamic load at elevated temperatures.

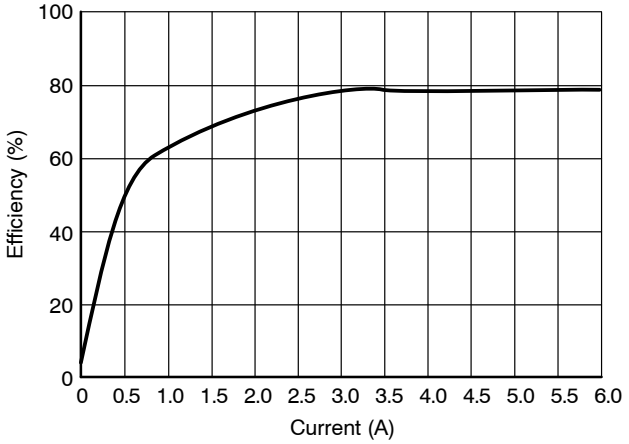

Figure 12. Efficiency

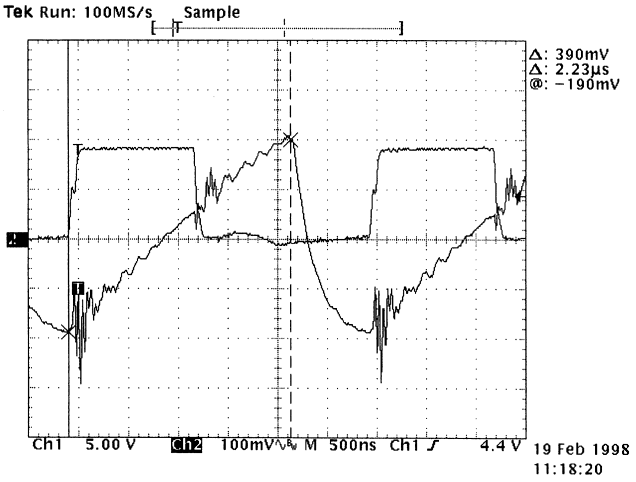

Figure 13. Channel 1 Gate Drive, Channel 2 V_{Slope}

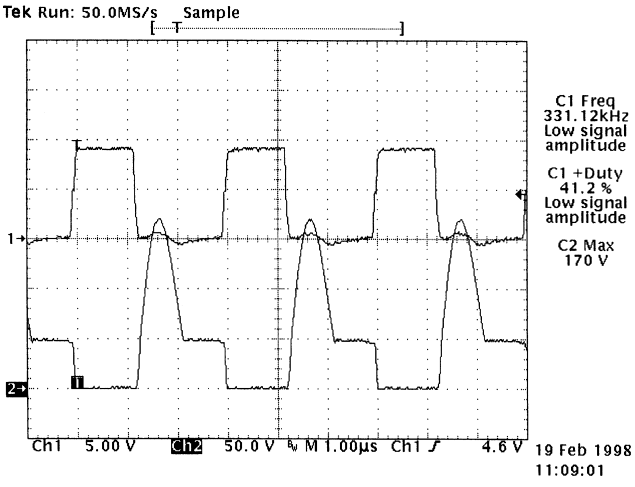

Figure 14. Channel 1 Gate Drive, Channel 2 Vds Reset Pulse

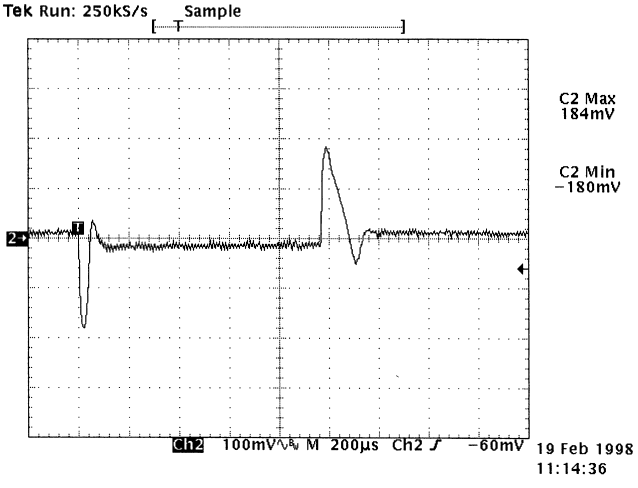

Figure 15. V_{OUT} During Load Transient from 0.5 A to 5.0 A

The Bode plots for the finished circuit are shown in Figures 16 through 19. These were measured using the Venable Industries Model 260 Frequency Response Analyzer and plotted in Microsoft® Excel.

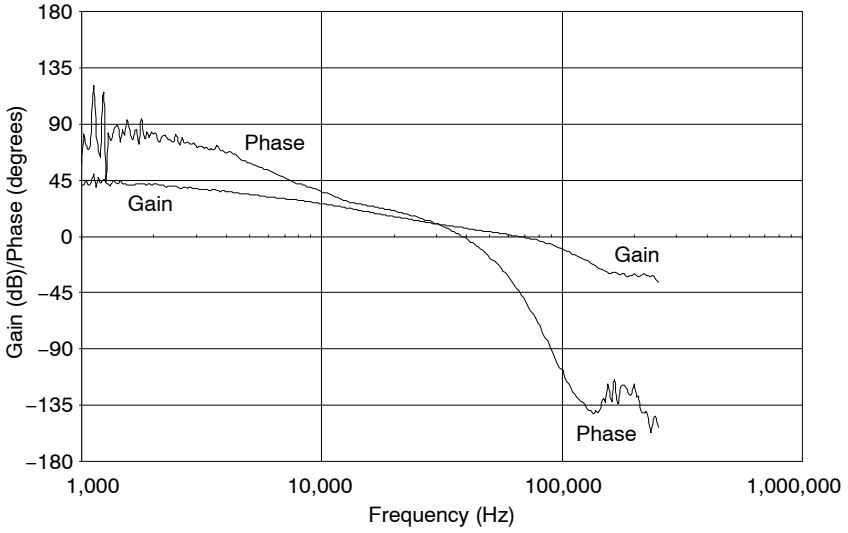

Figure 16. CS51022A Gain and Phase at Half Load (2.5 A)

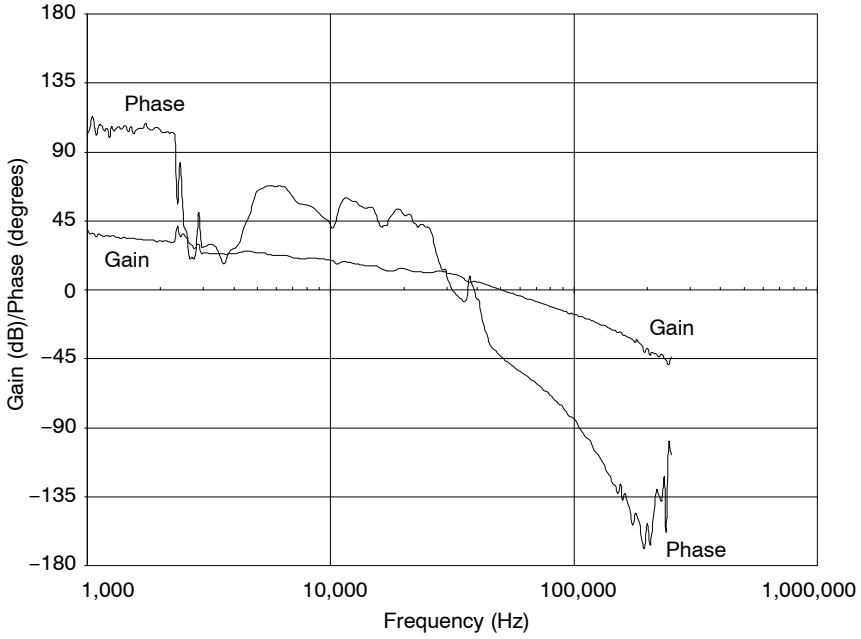

Figure 17. CS51022A Gain and Phase at Minimum Load (500 mA)

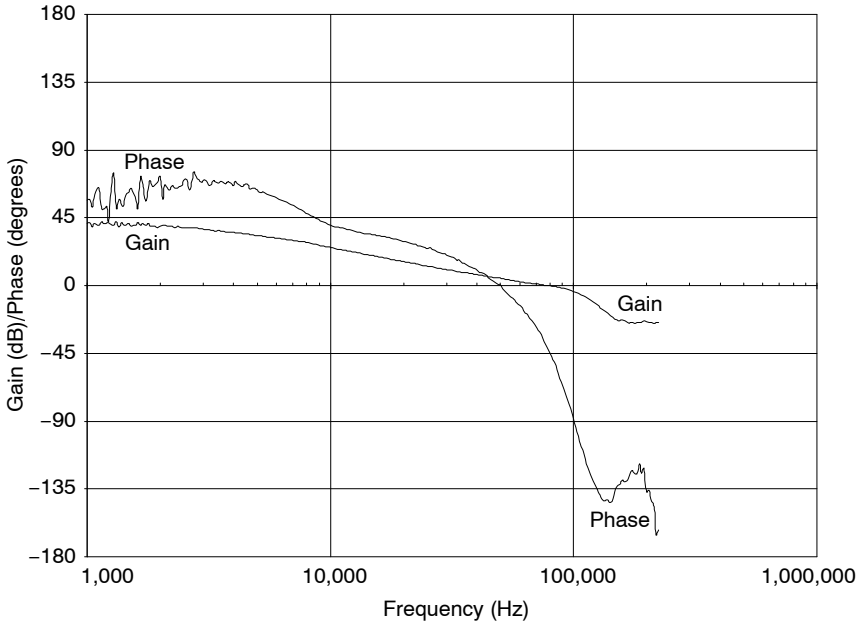

Figure 18. CS51022A Gain and Phase at Full Load (5.0 A)

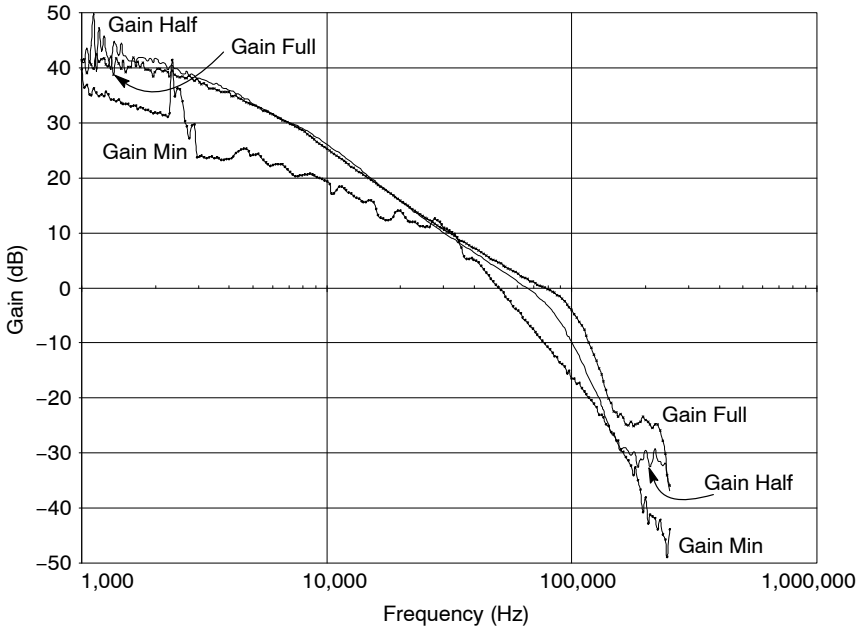

Figure 19. CS51022A Gain Plots for Different Loads

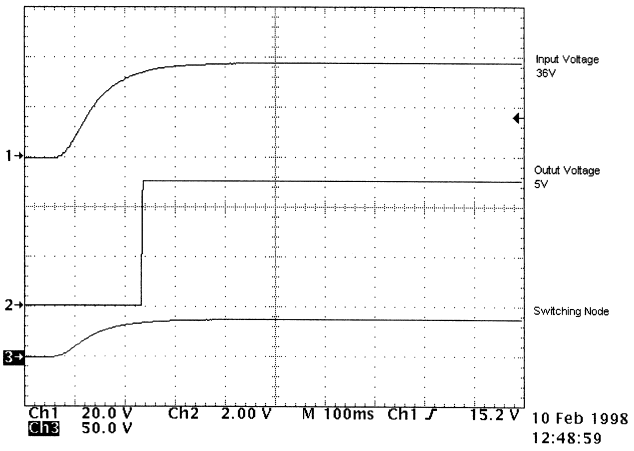

Figure 20. Startup

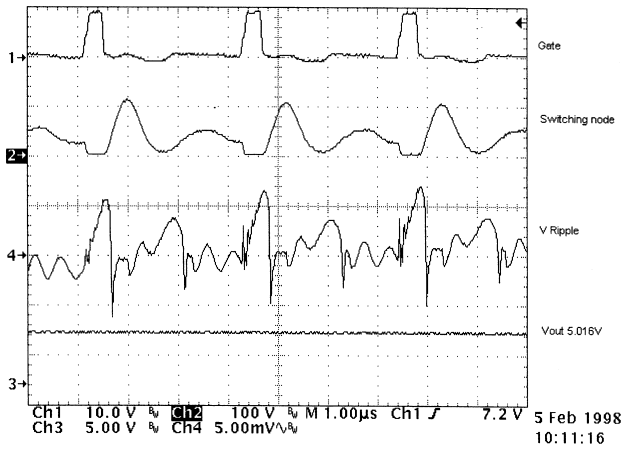

Figure 21. Min. Load Condition

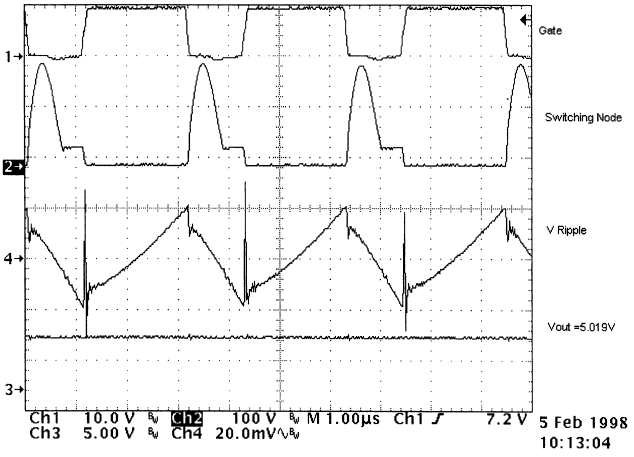

Figure 22. Half Load

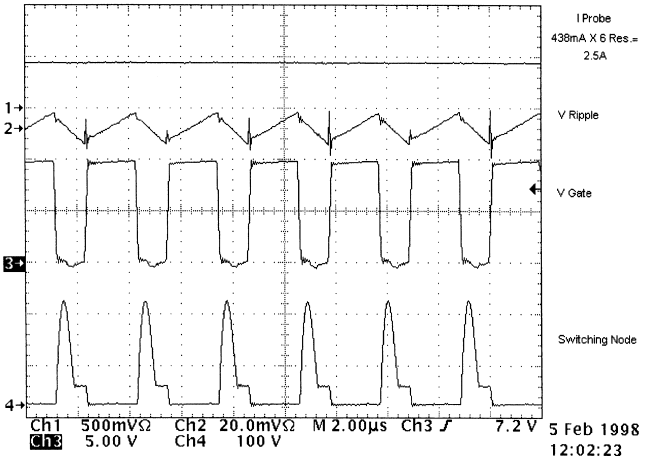

Figure 23. Half Load Showing I Probe

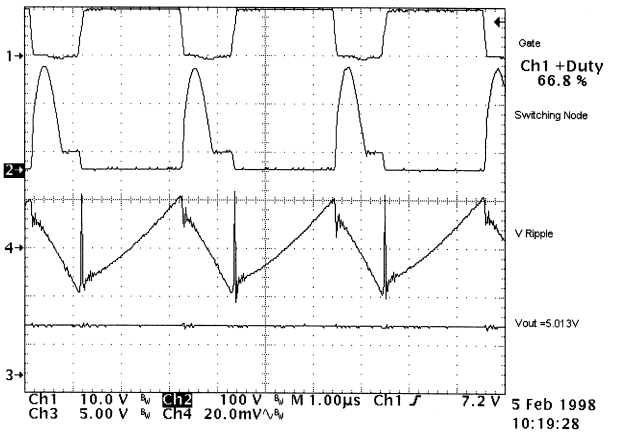

Figure 24. Full Load

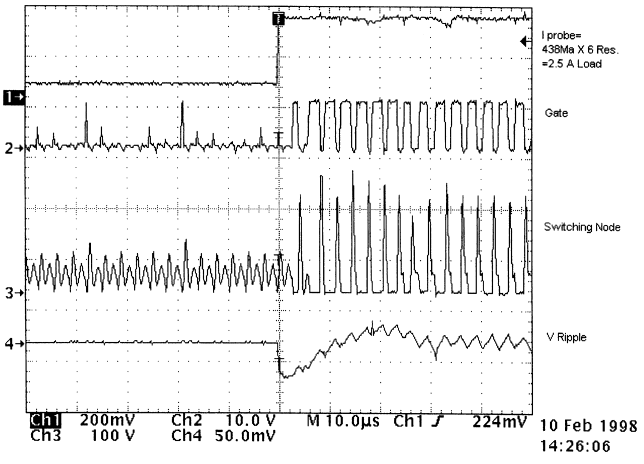

Figure 25. Transient Response Min. to 2.5 A

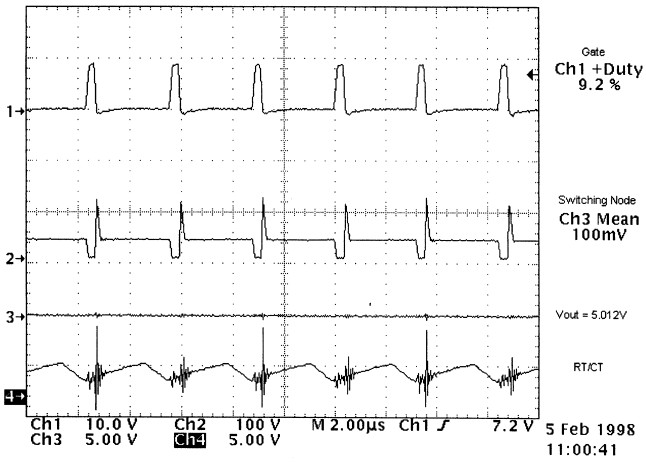

Figure 26. Short Circuit Condition

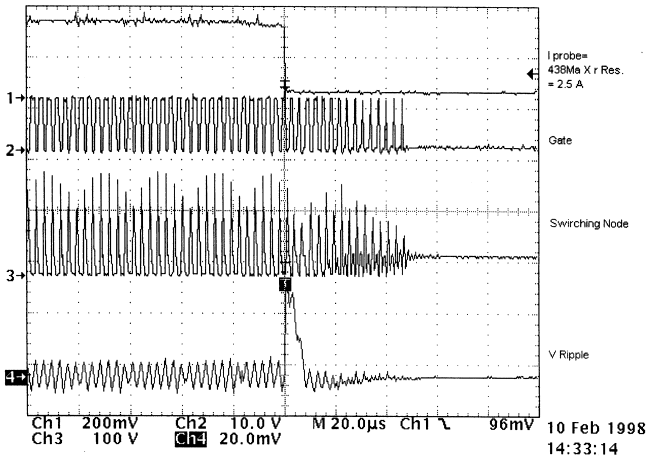

Figure 27. Transient Response 2.5 A to Min. Load

ELTest (Automated Power Supply Test System) Performance Graphs

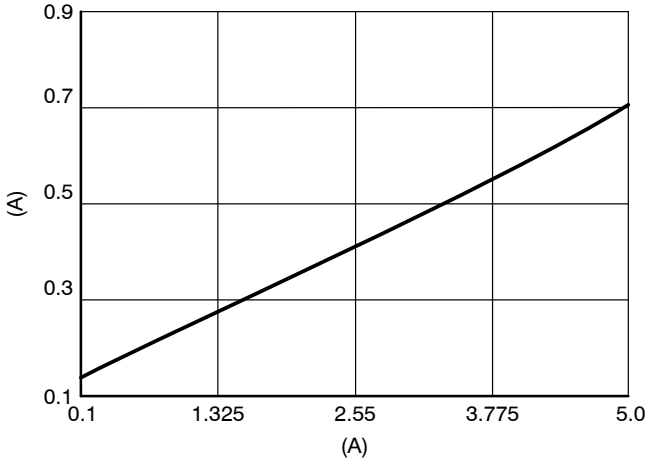

Figure 28. Input Current vs Load

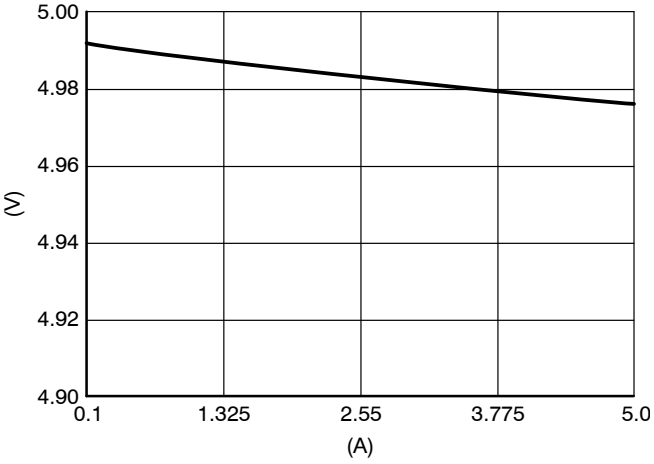

Figure 29. Load Regulation

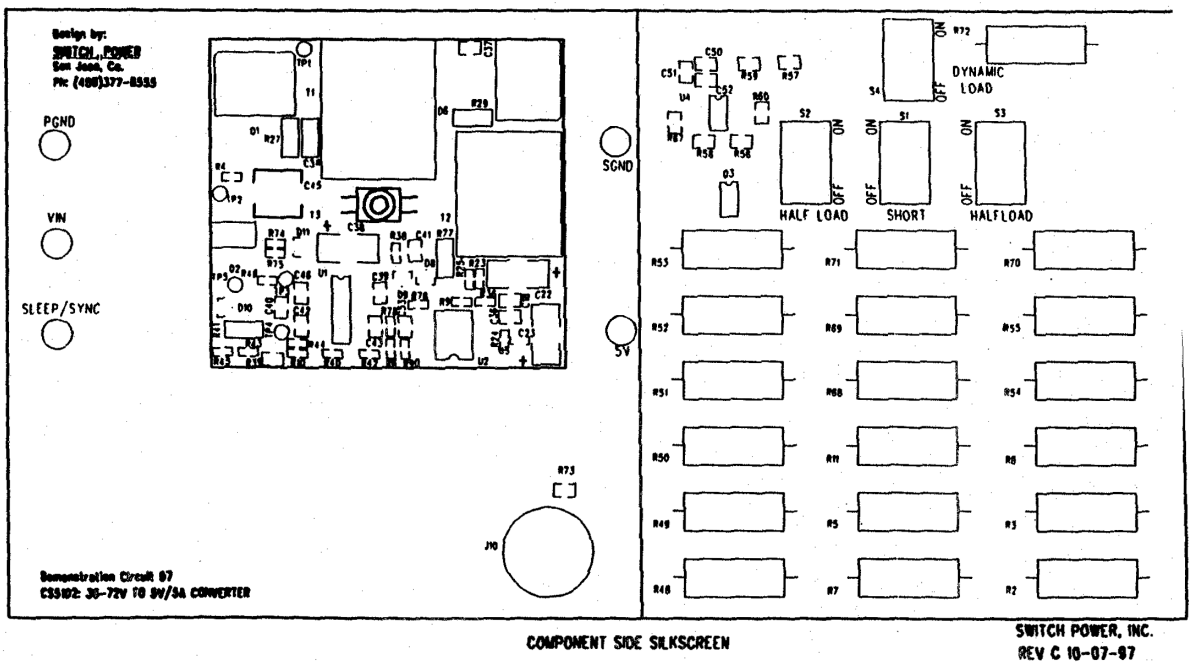

Figure 30. PC Board Layout

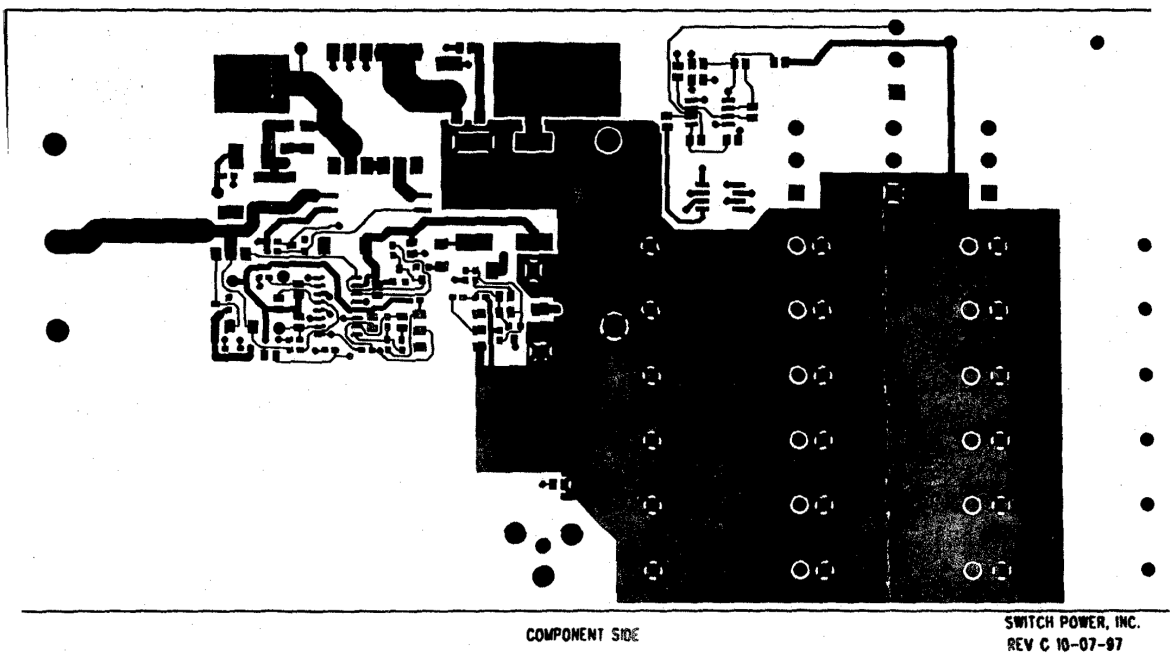

Figure 31. Component Side Copper

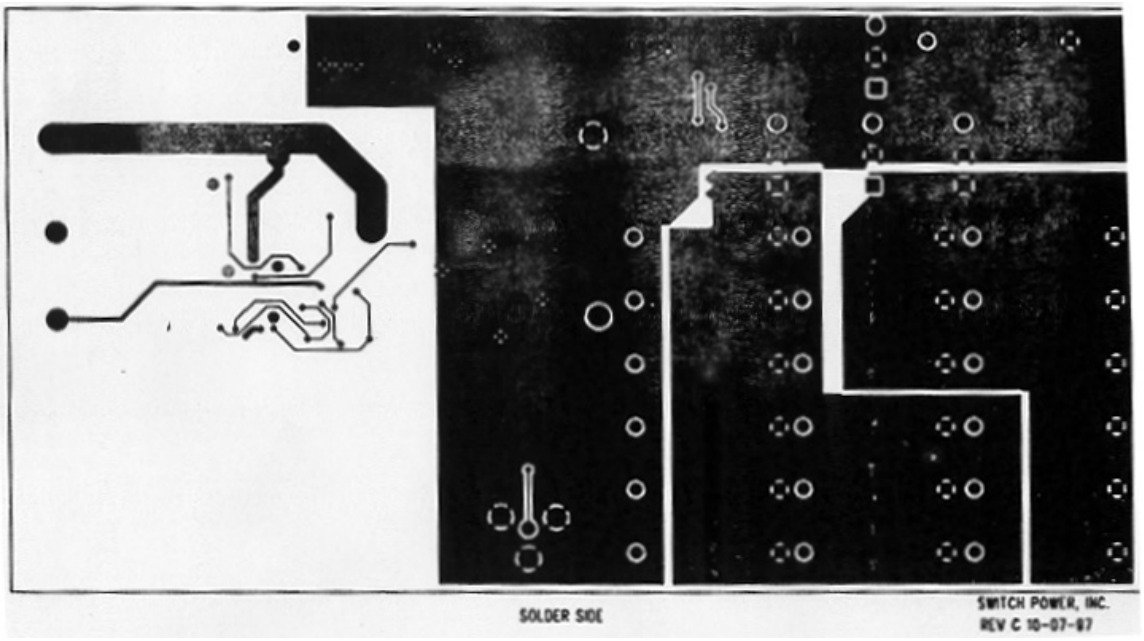

Figure 32. Solder Side Copper

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