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FDMF6704 Power Loss Calculation

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Introduction

The FDMF6704 DrMOS MCM (Multi Chip Module) product has HS and LS FETs and a gate driver all contained within a single module. The design has been optimized for Synchronous Buck applications. The switching and conduction loss of each HS FET, LS FET and gate driver are critical for system and application design. Generally it is hard to get measurement of each internal loss because of its MCM structure. Instead of measuring each power loss elements, expression of module power loss have been used to show MCM product power related performance. Module power loss is defined to be all power losses dissipated by DrMOS module itself. It includes all HS FET, LS FET and gate driver power losses. Using this approach, a system designer can easily estimate total power loss of the system, and do easy and convenient predictions of design related application performance. This application note explains basic theory of module power loss, and how to use the module power loss calculation tool. It is easy and convenient to use the power loss calculator when the system designer does a particular application design.

Power Loss of DrMOS

Figure 1 shows a typical Synchronous Buck application circuit using an FDMF6704 DrMOS product. The application schematic is based on a Fairchild Semiconductor FDMF6704 evaluation board which is used for datasheet characterization testing. The circuit includes all components in a Sync Buck converter except for the PWM controller. The PWM control function is accomplished by external voltage compensation loop using a pulse generator and a PC automation program. All passive components and layout, such as input caps, output caps, output inductor and boot cap, are optimized for DrMOS products.

Power loss sense point pins of FDMF6704 are VIN, VCIN, VDRV and VSWH. VIN is an input pin for main DC/DC power converting. It is connected to the internal HS FET drain. The current into VIN is related to HS FET switching and conduction losses. Its voltage level is typically 12 V in computing application. The VCIN pin is connected to the VCC of internal gate drive logic. The VDRV pin is used for HS and LS FET gate driving voltage. VCIN & VDRV of FDMF6704 are optimized for a 5 V power rail in computing applications. Both pins are normally connected to each other in an application. The VSWH pin is the switch node of Synchronous Buck converter. It is connected to the internal HS FET source and LS FET drain. As a point of view of a module product, VIN, VCIN and VDRV are inputs and VSWH is output. The module power loss and efficiency are defined by formulas as below.

- Module Power Loss

  = Module input power – Module output power

  = (Pin + Pcin&Pdrv) – Psw [W]

- Module Efficiency

  = Module output power / Module input power

  = Psw / (Pin + Pcin&Pdrv) * 100 [%]

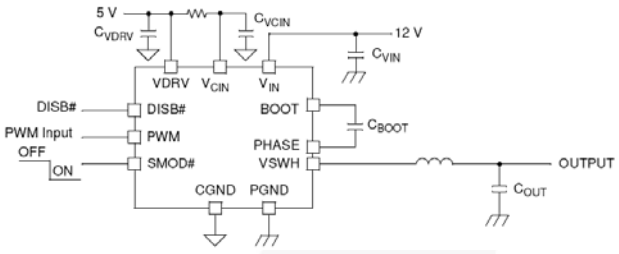

Figure 1. Typical Application Circuit of FDMF6704

The primary power loss elements in a Sync Buck converter are the switching devices and the output inductor. Silicon conduction and switching loss represent the largest element of the power loss in a typical Sync Buck converter. Normally inductor power loss is added to silicon loss to determine the system total performance. Key points of good inductor design include saturation current (adequate to handle peak transients), low DCR, core type, low noise and thermal characteristics. With a properly chosen inductor, module power loss is essentially independent of inductor power loss. Since we want to focus on silicon loss tradeoffs, we will use module power loss as our figure of merit to compare MCM designs.

Power Loss Measurement

Figure 2 shows the power loss diagram of a Fairchild DrMOS evaluation board. The input powers are PIN, PCIN and PDRV. Output power of the module is PSW. POUT is total board output power after power loss of the inductor. POUT is connected to Load.

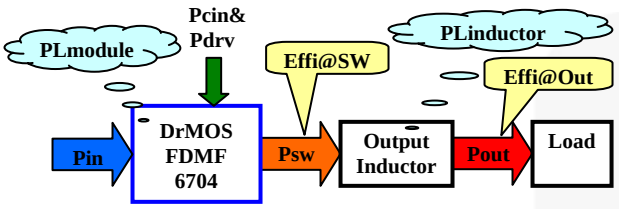

Figure 2. Ploss Diagram of FDMF6704 Eval Board

When designing a Sync Buck application, critical design parameters are input/output voltage, output current, switching frequency and inductor value. Typically input and output voltages are decided by the system application. Switching frequency and output inductor are then optimized to get the best trade-off among dynamic performance, EMI, thermal, BOM, cost, etc.

Using module power loss as a figure of merit, it is easy to judge which DrMOS design point is better or not since the module power loss does not include the inductor power loss. In other words, even using different inductors, module power loss can specify the real and accurate power loss of module itself and it is only slightly affected by inductor power loss, if the inductor value is correct and the application design is optimized.

PIN	VIN x IIN [W]
PCIN&PDRV	VCIN x ICIN [W] (including PDRV)
PSW	VSW x IOUT [W]
POUT	VOUT x IOUT [W]
PLmodule	PIN + PCIN&PDRV – PSW [W]
PLinductor	PSW – POUT [W]
Efficiency@SW	PSW/(PIN+PCIN&PDRV)*100 [%]
Efficiency@Out	POUT/(PIN+PCIN&PDRV)*100 [%]

Table 1. Power, Power Loss and Efficiency

Total Pin [W]	PLmod [W]	Psw [W]	PLind [W]	Pout [W]	Effi @SW [%]	Effi @Out [%]
46.49	6.771	39.72	0.64	39.08	85.44	84.06

Table 2. Power Loss Example at 30A Load

Table 1 and Table 2 show an example of power loss definition, measurement and calculation. A Fairchild FDMF6704 evaluation board was used for the testing. Note that module power loss without inductor power loss makes SW node efficiency higher than output node efficiency. Inductor power loss is 0.64 W and it makes output efficiency 1.3 % lower than SW node efficiency. If the inductor value is not optimized, the whole system performance as well as DrMOS will be affected and decreased. All input/output voltage and current are measured with precise DMM and current shunt resistors for accurate data capture.

Power Loss Graph in Datasheet

The evaluation board total efficiency, SW node efficiency and module power loss are measured and calculated to represent DrMOS product performance in the datasheet. The FDMF6704 datasheet has several graphs which indicate module power loss, output current, normalized module power loss and each design parameter variations. Figure 3 shows an example of a graph in the datasheet for module power loss vs. output current.

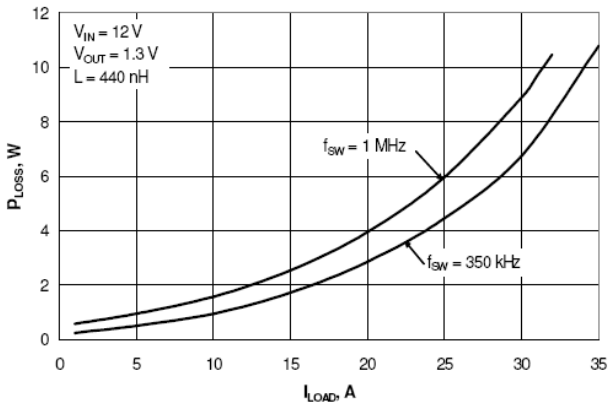

Figure 3. Module Power Loss vs. Iout

Figure 3 represents a performance of FDMF6704 with particular parameter values, such as VIN=12 V, VOUT=1.3 V, LOUT=440 nH, Fsw=350 kHz and output current from 0 to 35 A. This graph shows a performance under specific condition. In order to use the datasheet graphs easily in various system designs, normalized power loss graphs for each key parameter are included in the datasheet. In the Figure 4, power loss of the module is plotted with a normalized value according to the output voltage change. The reference value of module power loss for normalization is chosen as 1.3 Vout because this voltage is typical in a computing application, such as multi-phase VRD for Vcore. When the output voltage is 2 V, normalized module power loss will be around 1.13 times higher compared to 1.3 Vout.

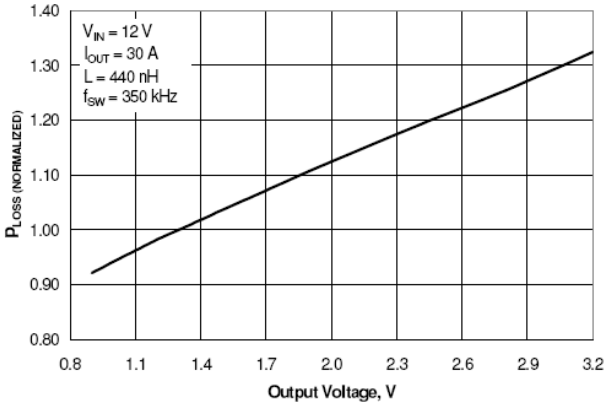

Figure 4. Normalized Module Ploss vs. Vout

FDMF6704 Evaluation Board

The FDMF6704 evaluation board is used for FDMF6704 electrical characterization test. The board specifications and structure are shown in Table 3.

Dimension	15 x 15 cm
No. of layers	4 layers
Layer sequence	TOP-GND-PWR-BOT
Total thickness	1.6 mm
TOP and BOT	1.5 oz (1 oz base + 0.5 oz plating)
GND and PWR	1 oz

Table 3. Evaluation Board Spec. and Structure

Table 4 shows reference test condition of evaluation board.

VIN	12 V
VCIN & VDRV	5 V
VOUT	1.3 V
PWM HI/LO	5 V/0 V
FSW	350 kHz
IOUT	0~35 A, 5 A step
Soaking time	5 minutes
LOUT	440 nH/0.32 mOhms/35 A
Snubber	Not used
Air flow	Not used
Heat sink	Not used
Ambient Temp.	25 C

Table 4. Evaluation Board Reference Test Condition

Calculation Example of Power Loss

All power loss graphs in the FDMF6704 datasheet are generated from measured evaluation board test data. System designer can calculate module power loss with normalized power loss graphs, and estimate performance of the module and application. Examples below show how to calculate module power loss with normalized power loss graphs in datasheet.

- Example 1

1. Define design parameters

   Vin=12 V

   Vcin & Vdrv=5 V

   Vout=1.5 V

   Iout=30 A

   Fsw=600 kHz

   Inductor=440 nH

2. Calculate each steps

   - Find reference design parameter values and module power loss with Figure 3 → 6.8 W with 12 Vin, 5 Vcin, 1.3 Vout, 30 A, 350 kHz and 440 nH

   - Find normalized value of module power loss with Figure 4 when Vout is 1.5 V → 1.04

   - Multiply 6.8 W by 1.04 → 7.072 W

   - Find normalized value of module power loss with Figure 5 when Fsw is 600 kHz → 1.12

   - Multiply 7.072 W by 1.12. → 7.921 W

   - The calculated module power loss is 7.921 W.

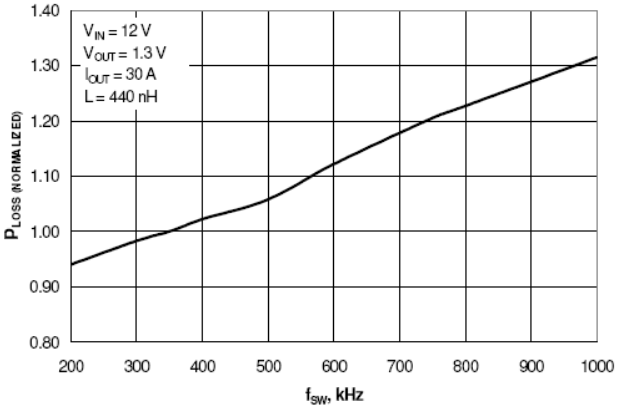

Figure 5. Normalized Module Ploss vs. Fsw

In this example 1, two design parameters, such as Vout and Fsw, are changed from reference values. The calculated module power loss shows under 0.5 % error compared to the real lab test data. Table 5 shows the module power loss

error between calculated result with datasheet graphs and real lab data from test.

Calculated Module Ploss	Real Module Ploss	Ploss Error
7.921 W	7.96 W	(1-7.921/7.96)*100 =0.495 %

Table 5. Power Loss Error of Example 1

- Example 2

1. Define design parameters

   Vin=10 V

   Vcin & Vdrv=5.5 V

   Vout=2 V

   Iout=25 A

   Fsw=600 kHz

   Inductor=320 nH

2. Calculate each steps

   - Find reference design parameter values and module power loss with Figure 3 → 4.6 W with 12 Vin, 5 Vcin, 1.3 Vout, 25 A, 350 kHz and 440 nH

   - Ploss at 10 Vin. Note Figure 6:

     4.6 W * 1.016 = 4.674 W

   - Ploss at 10 Vin and 5.5 Vcin. Note Figure 7

     4.674 W * 0.957 = 4.473 W

   - Ploss at 10 Vin, 5.5 Vcin and 2 Vout. Note Figure 4:

     4.473 W * 1.13 = 5.054 W

   - Ploss at 10 Vin, 5.5 Vcin, 2 Vout and 600 kHz. Note Figure 5:

     5.054 W * 1.12 = 5.661 W

   - Ploss at 10 Vin, 5.5 Vcin, 2 Vout, 600 kHz and 320 nH. Note Figure 8:

     5.661 W * 1.007 = 5.7 W

   - The calculated module power loss is 5.7 W. The error between calculated and real data is around 3.8 %. See Table 6 below for error calculation.

Calculated Module Ploss	Real Module Ploss	Ploss Error
5.7 W	5.489 W	(1-5.7/5.489)*100 =-3.844 %

Table 6. Power Loss Error of Example 2

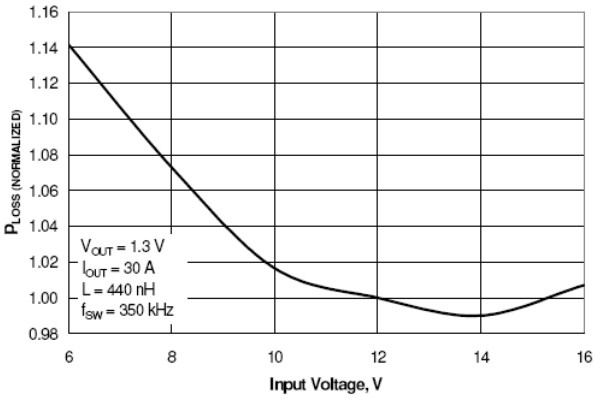

Figure 6. Normalized Module Ploss vs. Vin

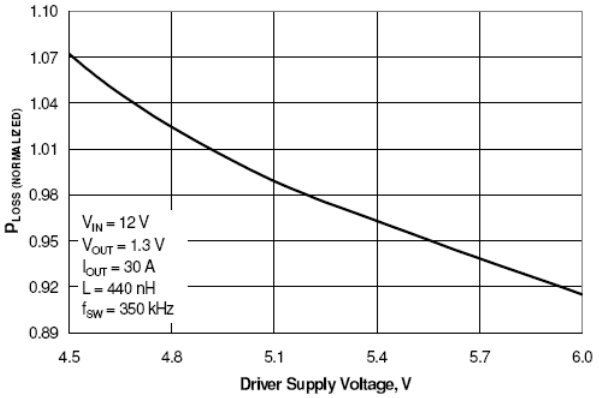

Figure 7. Normalized Module Ploss vs. Vcin&Vdrv

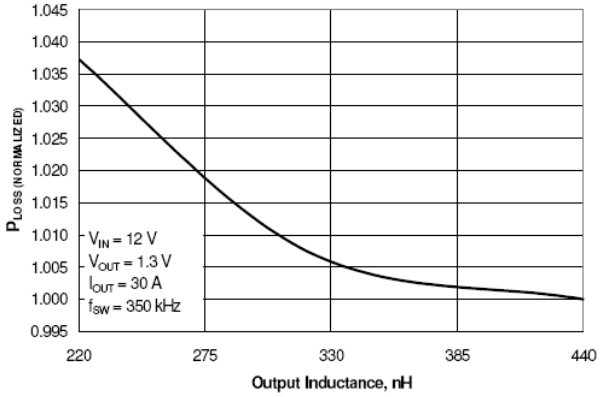

Figure 8. Normalized Module Ploss vs. Lout

FDMF6704 Ploss Calculation Tool

In order to get quick and accurate performance estimation, the automatic power loss calculation tool was developed using concepts mentioned in the previous paragraph. The calculator excel file can be used for estimating FDMF6704 performance regarding power loss and efficiency. Figure 9 shows the table for parameter input. The yellow cells are user input parameters and the blue cells are calculated parameters by internal logic of excel file. Once the user inputs parameter value into the yellow cells, the sheet automatically calculates power loss, efficiency and module temperature, and also generates performance related charts. Note that each user input parameter has a minimum input step. For example, the "VIN" parameter has input range from 5 V to 16 V with 0.5 V step. The "Recommended OUTL" parameter shows a calculated inductor value according to other parameter input. The user can enter this "Recommended OUTL" value into the yellow "OUTL Value" cell. The "Δ IL Ratio Value" depends on application design related to output voltage ripple. The user inputs this value from 20 % to 30 % of Iout for normal Sync Buck application.

Parameter	Value	Unit	Input Range	Nor. Value
VIN	12	V	5~16 V, 0.5 V step	0.99543
VCIN&VDRV	5	V	4~6 V, 0.1 V step	1.00000
VOUT	1.3	V	0.8~5 V, 0.1 V step	0.99918
Max. IOUT	30	A	0~35 A, 1 A step	1.00000
FSW	350	kHz	200~1000 kHz, 50 kHz step	1.01972
OUTL	440	nH	100~700 nH, 20 nH step	1.00000
ΔIL Ratio	25	%	OUTL ripple current, 20~30 % of Iou	N/A
Recommended OUTL	442	nH	$OUTL = \frac{(VIN-VOUT)\times VOUT}{FSW\times\Delta IL\times VIN}$	N/A
				1.01423

Figure 9. Input Parameters of Ploss Calculation Tool

Figure 10 is a table which is generated by input parameter values. All design parameters, input/output powers, efficiencies and module case top temperature are generated automatically. The red values mean a warning for over-specification of FDMF6704 maximum current and module temperature. For example, current of 35 A would make 10.93 W module power loss and 145 C module case top temperature. The user should consider specification of FDMF6704 and application when using this design tool.

Input Voltage for DC/DC	Input Voltage for Gate Driver	Total Input Power	Module Power Loss	Power at VSW node	Efficiency at VSW node	Inductor Power Loss	Output Voltage	Output Current	Total Output Power	Efficiency at Output	Module Max. Case Temp.
VIN [V]	VCIN&VDRV [V]	PINtot [W]	PD_MOD [W]	PSW [W]	EFFI@SW [%]	PD_L [W]	VOUT [V]	IOUT [A]	POUT [W]	EFFI@OUT [%]	MOD_TEMP [C]
12	5	0.185	0.184	0.001	0.282	0.001	1.3	0	0	0.000	28.4
12	5	1.550	0.250	1.300	83.887	0.000	1.3	1	1.3	83.869	29.1
12	5	2.915	0.313	2.602	89.252	0.002	1.3	2	2.6	89.191	29.8
12	5	4.282	0.377	3.905	91.199	0.005	1.3	3	3.9	91.087	30.5
12	5	5.651	0.442	5.209	92.178	0.009	1.3	4	5.2	92.015	31.2
12	5	7.026	0.511	6.515	92.728	0.015	1.3	5	6.5	92.516	32.0
12	5	8.407	0.585	7.822	93.038	0.022	1.3	6	7.8	92.779	32.8
12	5	9.797	0.667	9.130	93.192	0.030	1.3	7	9.1	92.887	33.6
12	5	11.197	0.758	10.439	93.233	0.039	1.3	8	10.4	92.884	34.6
12	5	12.608	0.859	11.749	93.188	0.049	1.3	9	11.7	92.796	35.7
12	5	14.033	0.972	13.061	93.074	0.061	1.3	10	13	92.640	37.0
12	5	15.472	1.098	14.374	92.903	0.074	1.3	11	14.3	92.427	38.3
12	5	16.926	1.238	15.688	92.686	0.088	1.3	12	15.6	92.168	39.8
12	5	18.395	1.392	17.003	92.431	0.103	1.3	13	16.9	91.871	41.5
12	5	19.882	1.562	18.320	92.143	0.120	1.3	14	18.2	91.542	43.3
12	5	21.385	1.747	19.638	91.830	0.138	1.3	15	19.5	91.186	45.4
12	5	22.905	1.948	20.957	91.495	0.157	1.3	16	20.8	90.810	47.5
12	5	24.443	2.165	22.278	91.143	0.178	1.3	17	22.1	90.416	49.9
12	5	25.998	2.398	23.600	90.778	0.200	1.3	18	23.4	90.008	52.4
12	5	27.570	2.647	24.924	90.401	0.224	1.3	19	24.7	89.589	55.1
12	5	29.161	2.912	26.249	90.014	0.249	1.3	20	26	89.159	58.0
12	5	30.771	3.195	27.576	89.618	0.276	1.3	21	27.3	88.721	61.1
12	5	32.400	3.495	28.904	89.212	0.304	1.3	22	28.6	88.272	64.3
12	5	34.050	3.815	30.234	88.795	0.334	1.3	23	29.9	87.812	67.8
12	5	35.723	4.157	31.566	88.364	0.366	1.3	24	31.2	87.339	71.5
12	5	37.422	4.522	32.899	87.915	0.399	1.3	25	32.5	86.848	75.4
12	5	39.149	4.915	34.234	87.444	0.434	1.3	26	33.8	86.336	79.7
12	5	40.911	5.341	35.571	86.946	0.471	1.3	27	35.1	85.795	84.3
12	5	42.713	5.804	36.909	86.412	0.509	1.3	28	36.4	85.220	89.3
12	5	44.562	6.312	38.250	85.835	0.550	1.3	29	37.7	84.602	94.8
12	5	46.466	6.874	39.592	85.206	0.592	1.3	30	39	83.931	100.9
12	5	48.438	7.501	40.937	84.514	0.637	1.3	31	40.3	83.199	107.7
12	5	50.489	8.205	42.284	83.749	0.684	1.3	32	41.6	82.394	115.4
12	5	52.635	9.001	43.634	82.900	0.734	1.3	33	42.9	81.505	124.0
12	5	54.893	9.905	44.987	81.955	0.787	1.3	34	44.2	80.521	133.8
12	5	57.283	10.939	46.344	80.903	0.844	1.3	35	45.5	79.430	145.0

Figure 10. Calculated Power Loss and Efficiency

Figure 11 shows a chart which depicts the calculated efficiency and power loss at module. The user is able to use this chart on another document by copying and pasting.

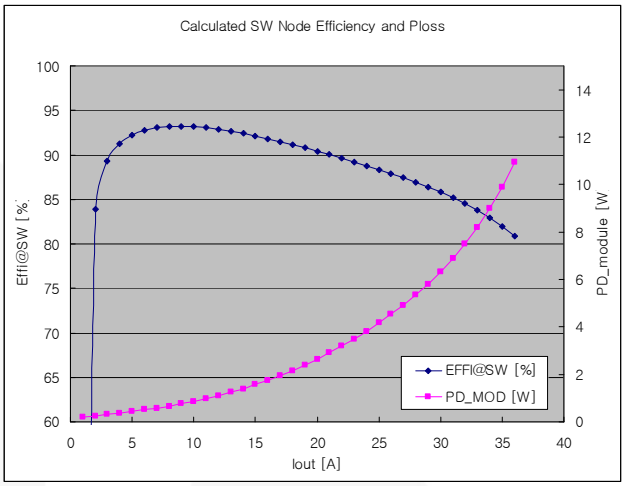

Figure 11. Calculated Efficiency and Power Loss Chart

Figure 12 is another example of a chart for module temperature. This chart can be also copied or pasted for end user documentation.

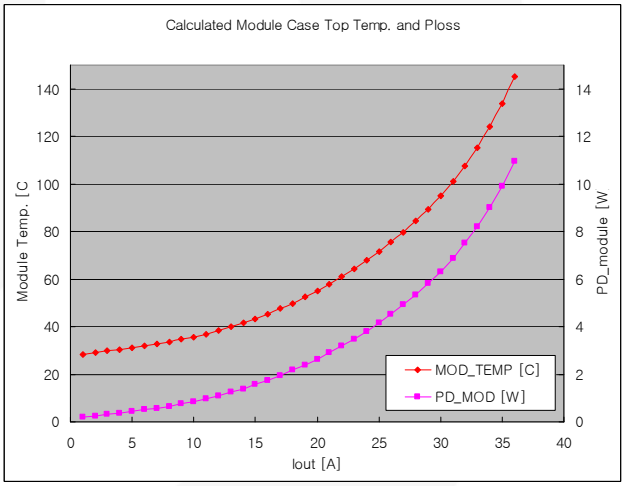

Figure 12. Calculated Module Temp. and Ploss Chart

The data used for this tool is based on a real lab test data, and the models of each parameter are extracted with multi element polynomial equations. So its accuracy is good enough to check brief power loss related to performance of FDMF6704. Typical power loss calculation error of this tool at max load is under 5 % compared to real data. Note that some application at various customers would show different performance, if their application circuit, components, board layout and structure are significantly different from Fairchild evaluation board environment. The internal parameters, equations and calculating logic are Fairchild confidential since they are directly related to the HS FET, LS FET and gate driver electrical characteristics. The locked version of FDMF6704 power loss calculator

tool will be provided to customers so that its internal parameters should not be opened to outside. If the user would like to use an unlocked version, please contact to Fairchild staff.

Summary

Fairchild DrMOS FDMF6704 is a multi-chip module product for Sync Buck applications. To specify its performance, the concept of module power loss measurement and calculation is developed. Normalized power loss graphs are added in the datasheet to let the system designer use them for designing various applications. The graphs are based on the real lab test data and have a good accuracy. To support easy and convenient application design, the FDMF6704 automatic power loss calculation tool has been developed. The tool accuracy is a good to match to real data so that the designer is able to use this tool to know how much FDMF6704 application consumes power loss and how the performance it shows, before system design and test.

Related Documents

FDMF6704 Datasheet:

FDMF6704A Datasheet:

FDMF6704V Datasheet:

FDMF6704/A Power Loss Calculator REV0:

FDMF6704V Power Loss Calculator REV0:

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