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February 2006

AN-8015
FMS6501 Evaluation Board Application Note

Description

The FMS6501 evaluation board is a full functional 12x9 cross point matrix for evaluating the performance of the FMS6501. The demo board operates from standard supply voltages of +5V ±5% and +3.3V ±5%. This device may be driven by a DC-coupled DAC output or an AC-coupled input signal and inputs can be programmed for clamp or bias mode. Device outputs can be either DC or AC coupled and may also be programmed for a gain of 6, 7, 9 or 12dB. In addition unused outputs may be disabled to reduce power dissipation.

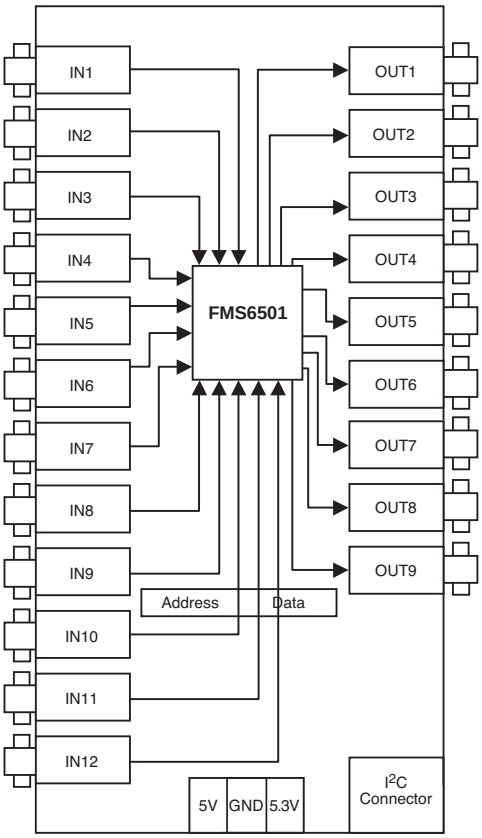
The FMS6501 provides 12 inputs that can be routed to any of 9 outputs. Each input can be routed to one or more output but only one input may be routed to any output. Programming of the FMS6501 is controlled via an I^2C set of inputs or manual register and data settings

Applications

- Cable and Satellite set top boxes
- TV and HDTV sets
- A/V switches
- Security/surveillance
- Personal Video Recorders (PVR)
- Video distribution
- Automotive (in-cabin entertainment)

For a complete description of the FMS6501 please refer to the FMS6501 data sheet.

Evaluation Board Block Diagram



Evaluation Kit Contents

The FMS6501 Evaluation Kit contains the following items:

- AN-8015 – FMS6501 Evaluation Board Application Note
- The latest revision of the FMS6501 data sheet, which also can be obtained from *http://www.fairchildsemi.com*.
- Fully functional FMS6501 eval board
- VIPDEMO™ control software
- Female power connector

Board Setup and Test

The following test equipment is necessary to fully test the FMS6501 evaluation board.

- Installed VIPDEMO™ control software for program control of FMS6501. (follow directions on CD)
- Power supplies +5V ±5%, 250mA and +3.3v ±5%, 250mA
- One high resolution CRT monitor (YC, CV, GBR, Component)
- One HDTV monitor (480I, 480P, 720I, 720P, 1080I)
- One NTSC or PAL video signal source capable of generating necessary outputs. (GBR, Y, C, & Composite)
- One PS/HD video signal source capable of generating necessary outputs. (480I, 480P 720I, 720P, 1080I)
- One video measurement set (VM700)
- One video measurement set (VM5000)
- Assorted video cables

DO NOT turn on power supply until all connections are completed.

1. Set the power supply 1 to 5.0V and supply 2 to +3.3V. Connect the power supplies to the input voltage terminals of the demonstration board.
2. Connect G_{OUT} signal source to the In1 input BNC connector.
3. Connect B_{OUT} signal source to the In2 input BNC connector.
4. Connect R_{OUT} signal source to the In3 input BNC connector.
5. Connect G_{IN} of monitor to Out1.
6. Connect Bin of monitor to Out2.
7. Connect Rin of monitor to Out3.
8. Turn on the power supplies.
9. Check that address select jumper is in place. This sets device address to 0x 06.
10. Execute VIPDEMO™ control software by clicking on VIP demo icon. See test setup configuration diagram below.
11. Click “Show Config” button and verify that Bus_Addr is set to 0x06.
12. Program In1 - Bias, In2 - bias and In3 - bias mode.
13. Program In1 to out1, In2 to Out2 and In3 to Out3.
14. Program Out1 6dB, Out2 6dB and Out3 6dB.
15. Program “ON” Out1 enable, Out2, enable and Out3 enable.
16. Verify monitor is setup to receive GBR signals.
17. Verify test pattern that is produced from the signal generator is the same as the pattern on the monitor. Example 100% color bars.
18. Testing is now complete

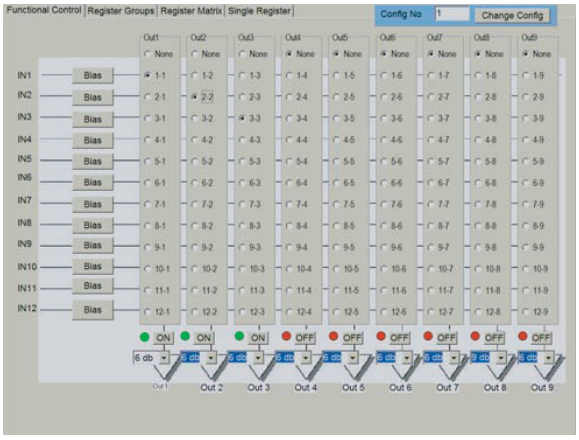


Figure 1. VIPDEMO™ Test Setup Configuration

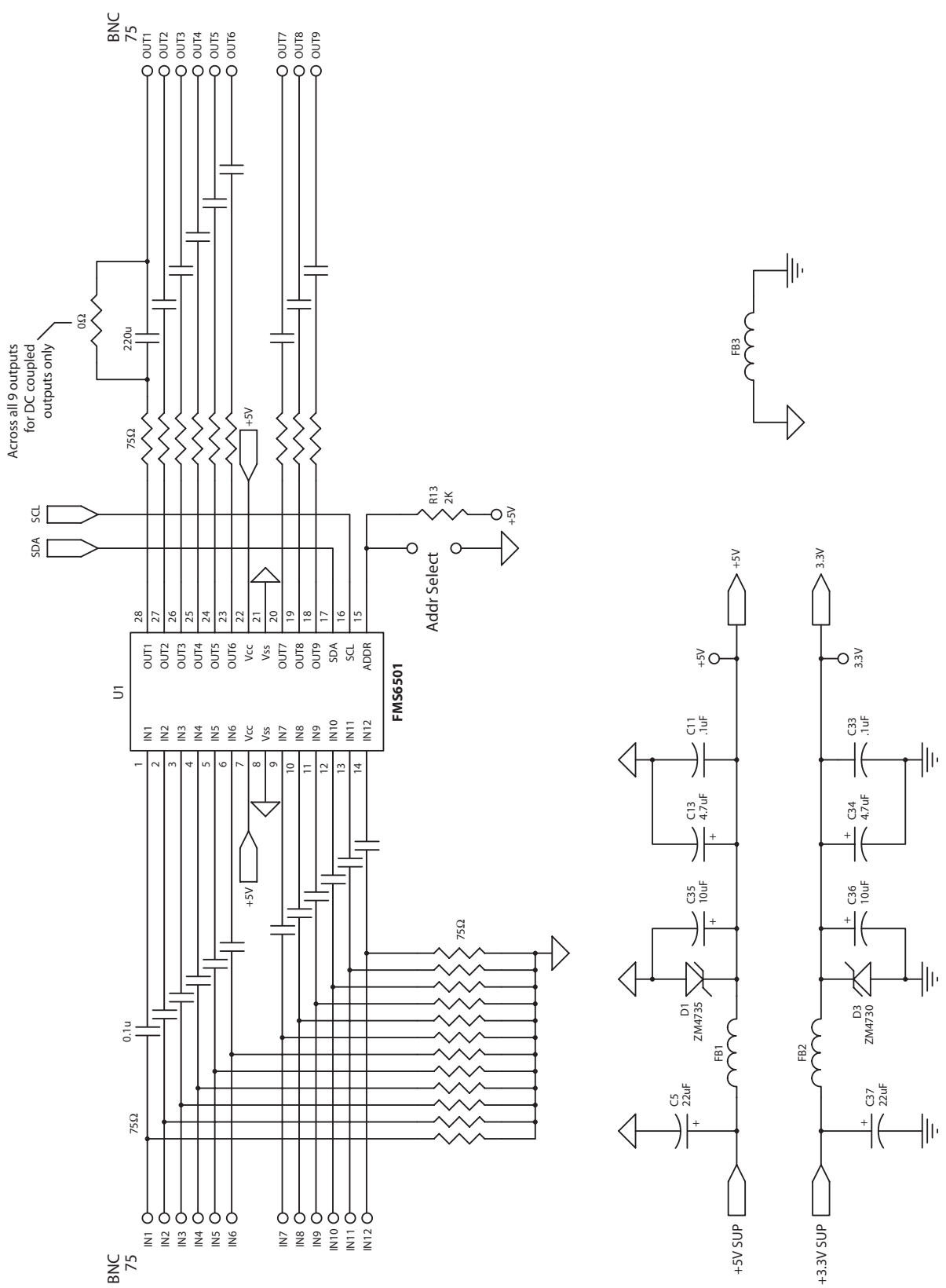


Figure 2. FMS6501 Schematic Diagaram

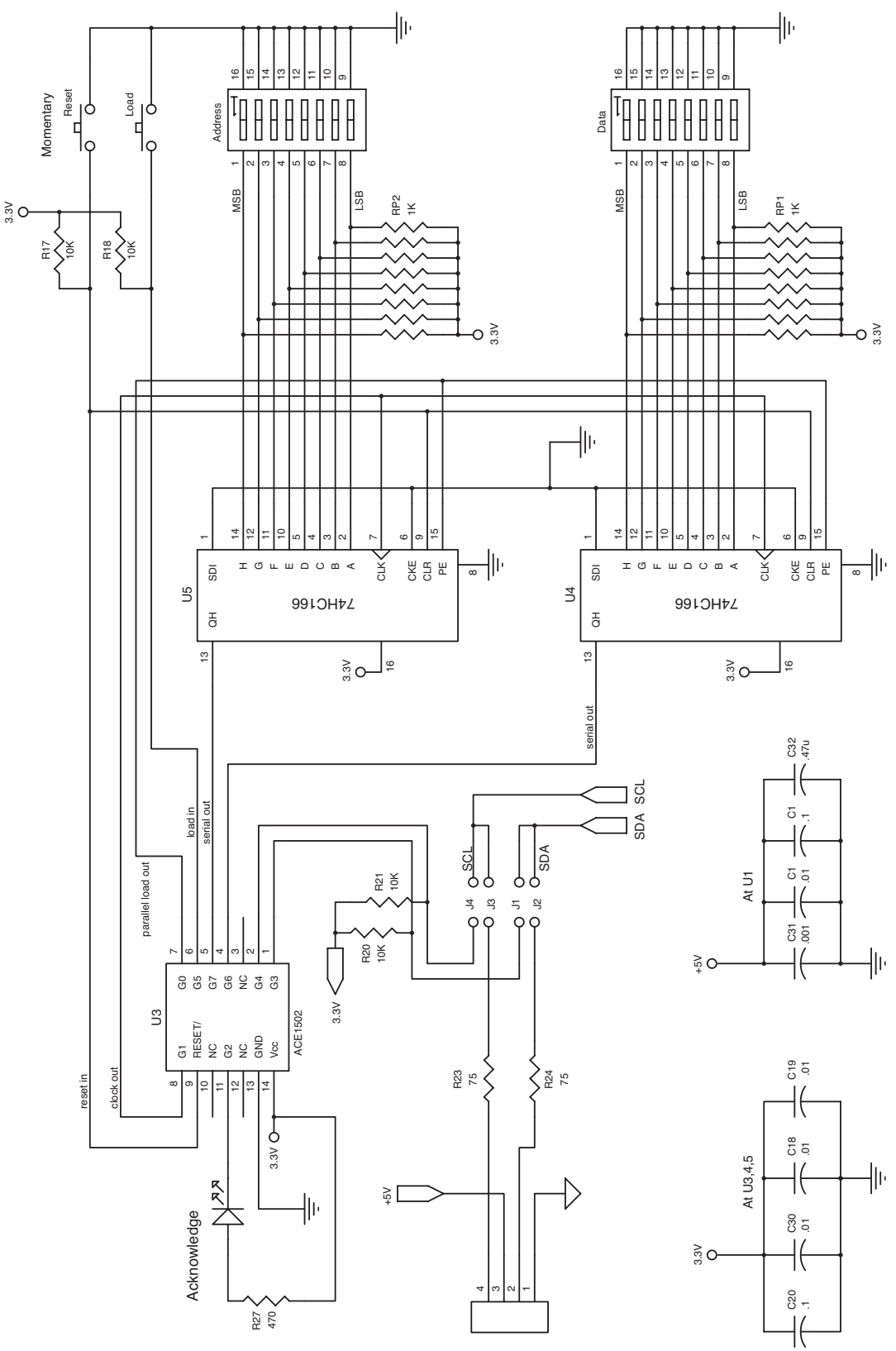
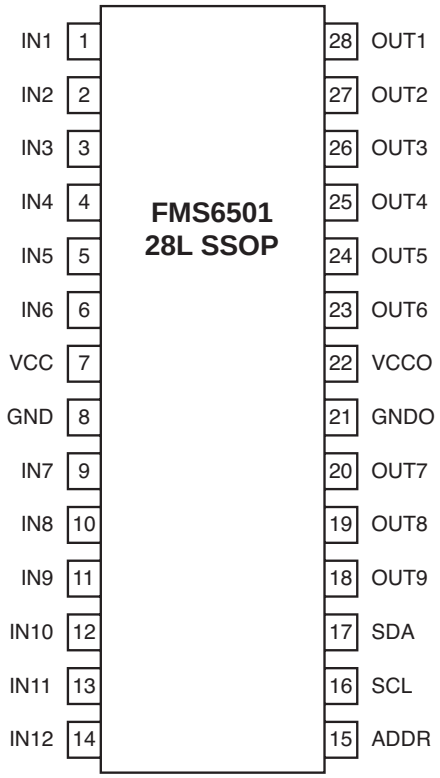


Figure 3. I²C Input/Manual Register Data Control Schematic Diagaram

Pin Configuration



Pin Assignments

Pin #	Pin	Type	Description
1	IN1	Input	Input, channel 1
2	IN2	Input	Input, channel 2
3	IN3	Input	Input, channel 3
4	IN4	Input	Input, channel 4
5	IN5	Input	Input, channel 5
6	IN6	Input	Input, channel 6
7	VCC	Input	Positive power supply
8	GND	Input	Must be tied to GND
9	IN7	Input	Input, channel 7
10	IN8	Input	Input, channel 8
11	IN9	Input	Input, channel 9
12	IN10	Input	Input, channel 10
13	IN11	Input	Input, channel 11
14	IN12	Input	Input, channel 12
15	ADDR	Input	Selects I^2C address. “0” = 0x06 (0000 0110), “1” = 0x86 (1000 0110)
16	SCL	Input	Serial clock for I^2C port
17	SDA	Input	Serial data for I^2C port
18	OUT9	Output	Output, channel 9
19	OUT8	Output	Output, channel 8
20	OUT7	Output	Output, channel 7
21	GNDO	Input	Must be tied to GND
22	VCCO	Input	Positive power supply for output drivers
23	OUT6	Output	Output, channel 6
24	OUT5	Output	Output, channel 5
25	OUT4	Output	Output, channel 4
26	OUT3	Output	Output, channel 3
27	OUT2	Output	Output, channel 2
28	OUT1	Output	Output, channel 1

Bill of Materials

Item	Quantity	Reference	Part
1	13	C20, C7-C9, C17-C26	0.1μF
2	1	C31	0.001μF
3	4	C1, CC18, C19, C30	0.01μF
4	1	C32	0.47μF
5	2	C37, C5	22μF
6	2	C33, C11	0.1μF
7	2	C34, C13	4.7μF
8	2	C35, C36	10μF
9	1	D1	ZM4735
10	1	D2	Red
11	1	D3	ZM4730
12	3	FB1, FB2, FB3	Inductor
13	5	J1, J2, J3, J4, J5	Jumper
14	1	J1	1k
15	2	RP2, RP1	2k
16	1	R13	10k
17	4	R17, R18, R20, R21	3M
18	29	R1-R29	75Ω
19	1	R27	470Ω
20	9	R30-R38	0Ω (stuff option)
21	1	S1	SW DIP-8
22	1	S1	Load
23	1	S2	Reset
24	1	U1	FMS6501
25	1	U3	ACE1502
26	2	U4, U5	74HC166

Applications Information

Input Clamp/Bias Circuitry

The FMS6501 can accommodate either AC or DC coupled inputs.

Internal clamping and bias circuitry are provided to support AC coupled inputs. These are selectable through the CLMP bits via the I^2C compatible interface.

For DC coupled inputs, the device should be programmed to use the 'bias' input configuration. In this configuration, the input is internally biased to 625mV through a 100kΩ resistor. Distortion is optimized with the output levels set between 250mV above ground and 500mV below the power supply. These constraints along with the desired channel gain need to be considered when configuring the input signal levels for input DC coupling.

With AC coupled inputs, the FMS6501 uses a simple clamp rather than a full DC-restore circuit. For video signals with and without sync, (Y,CV,GBR) the lowest voltage at the output pins will be clamped to approximately 300mV above ground when the 6dB gain setting is selected.

If symmetric AC coupled input signals are used, (chroma, Pb, Pr, Cb, Cr) the bias circuit mentioned above can be used to center them within the input common range. The average DC value at the output will be approximately 1.27V with a 6dB gain setting. This value will change, depending upon the selected gain setting.

Gain Setting	Clamp Voltage	Bias Voltage
6dB	300mV	1.27V
7dB	330mV	1.43V
8dB	370mV	1.60V
9dB	420mV	1.80V

The following diagram shows the clamp mode input circuit and the internally controlled voltage at the input pin for AC coupled inputs:

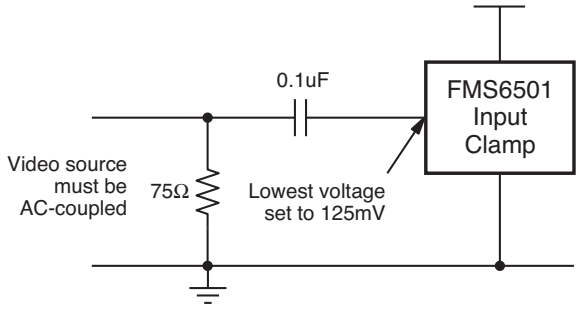


Figure 4. Clamp Mode Input Circuit

The following diagram shows the bias mode input circuit and the internally controlled voltage at the input pin for AC coupled inputs.

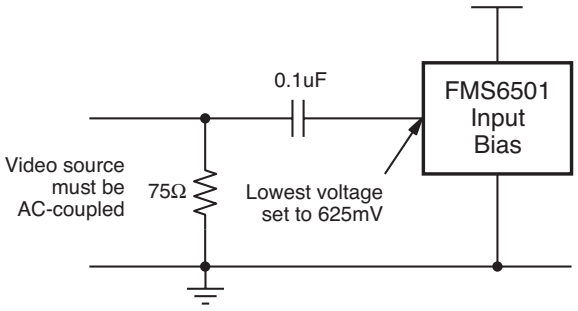


Figure 5. Bias Mode Input Circuit

Output Configuration

The FMS6501 outputs may be either AC or DC coupled. Resistive output loads can be as low as 75Ω, representing a dual doubly terminated video load. High impedance, capacitive loads up to 20pF can also be driven without loss of signal integrity. For standard 75Ω video loads a 75Ω matching resistor should be placed in series to allow for a doubly terminated load. DC coupled outputs should be connected as follows:

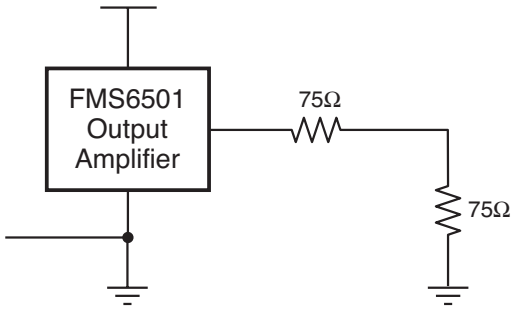


Figure 6. DC-Coupled Load Connection

AC-coupled loads should be configured as shown in Figure 6:

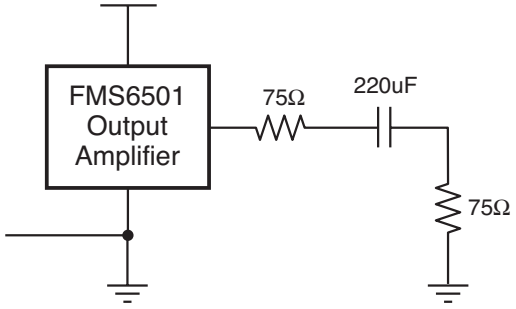


Figure 7. AC-Coupled Load Connection

Thermal Considerations

If multiple low impedance loads are DC coupled, increased power and thermal issues will need to be addressed. In this case, the use of a multi-layer board with a large ground plane to help dissipate heat is recommended. If a 2-layer board is used under these conditions, use of an extended ground plane directly under the device is recommended. This plane should extend at least 0.5" beyond the device. Other PC board layout issues are covered in the “Layout Considerations” section.

Thermal issues are significantly reduced with AC coupled outputs, alleviating the need for special PC layout requirements.

Each of the FMS6501 outputs can be independently disabled and placed in a high impedance state with the ENABLE bit. This function can be used to mute video signals, to parallel multiple FMS6501 outputs, or to save power. When the output amplifier is disabled, the high impedance output presents a 3kW load to ground. The output amplifier will typically enter and recover from the power down state in less than 300ns after being programmed.

When an output channel is not connected to an input, the input to that particular channels amplifier is forced to approximately 150mV. The output amplifier is still active, unless specifically disabled by the I^2C interface. Voltage output levels will depend on the programmed gain for that channel.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance and thermal characteristics. The FMS6501DEMO is a 4-layer board with a full power and ground plane. For optimum results of your system board, follow the steps below as a basis for high frequency layout:

- Include 10μF and 0.1μF bypass capacitors
- Place the 10μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Connect all external ground pins as tightly as possible, preferably with a large ground plane under the package
- Layout channel connections to reduce mutual trace inductance
- Minimize all trace lengths to reduce series inductances. If routing across a board, place device such that longer traces are at the inputs rather than the outputs

If using multiple, low impedance DC coupled outputs, special layout techniques may be employed to help dissipate heat.

If a multi-layer board is used, a large ground plane directly under the device will help reduce package case temperature.

For dual layer boards, an extended plane can be used.

Worse case additional die power due to DC loading can be estimated at ($V_{cc}2/4R_{load}$) per output channel. This assumes a constant DC output voltage of $V_{cc}/2$. For 5V V_{cc} with a dual DC video load, add 25/(4*75) = 83mW, per channel.

Applications for the FMS6501 Video Switch Matrix

The increased demand for consumer multimedia systems has created a large challenge for system designers to provide cost-effective solutions to capitalize on the growth potential in graphics display technologies. These applications will require cost effective video switching and filtering solutions to deploy high-quality display technologies rapidly and effectively to the target audience. Areas of specific interest include HDTV, Media Centers, and Automotive Infotainment (includes navigation, in cabin entertainment, and back up camera). In all cases, the advantages the integrated video switch matrix provides are high quality video switching specific to the application as well as video input clamps and on chip low impedance output cable drivers with selectable gain.

Generally the largest application for a video switch is for the front end of an HDTV. This is used to take multiple inputs and route them to their appropriate signal paths (main picture and picture in picture - PiP). These are normally routed into ADCs that are followed by decoders. There are many different technologies for HDTV including: LCD,Plasma, and CRT that have similar analog switching circuitry.

VIPDEMO™ Control Software

The FMS6501 is configured via an I2C compatible digital interface. In order to facilitate ease of demonstration, Fairchild Semiconductor had developed the VIPDEMOTM GUI based control software to write to the FMS6501 register map. This software is included when ordering an FMS6501DEMO kit. Also included is a Parallel port I2C adapter and an interface cable to connect to the demo board. Besides using the full FMS6501 interface, the VIPDEMOTM can also be used to control single register read and writes for I2C.

Manual Programming of the FMS6501 via Individual Register and Data Settings

The FMS6501 demo board is populated with circuitry that will allow the device to be programmed via manual input of register and data settings. The “EXT” jumpers will need to be moved to the “MAN” position to accomplish this task.

Register maps are described in detail in the FMS6501 datasheet. There are 11 registers that can be programmed to control input to output connections, output gain, output enable and input common mode level settings. An example would be to connect In2 to Out8, gain of 6dB output enabled and bias mode set. The first register that needs to be programmed is at address 0x08. The address and data switches are labeled for a logic low, logic high, LSB and MSB.

The settings for the data switches would be:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	0	0	0	0	1	0

The settings for the address would be:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	1	0	0	0

Next press the load button and this will load the address and data into the FMS6501. To set the device to bias mode, load the following addresses and data.

The settings for the data switches would be:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	0

The settings for the address would be:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	1	1	0	1

Press the load button and set the next data and address.

The settings for the data switches would be:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	0

The settings for the address would be:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	1	1	1	0

Press the load button and the device is programmed.

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