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# AN-7733

## FL7732 设计工具流程（升降压式）

### 概述

本文旨在深入讨论如何使用飞兆半导体设计工具设计采用 FL7732 的升降压拓扑结构。使用设计工具时，请参考产品数据表。

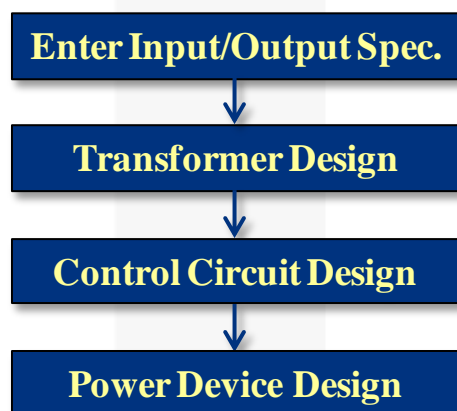
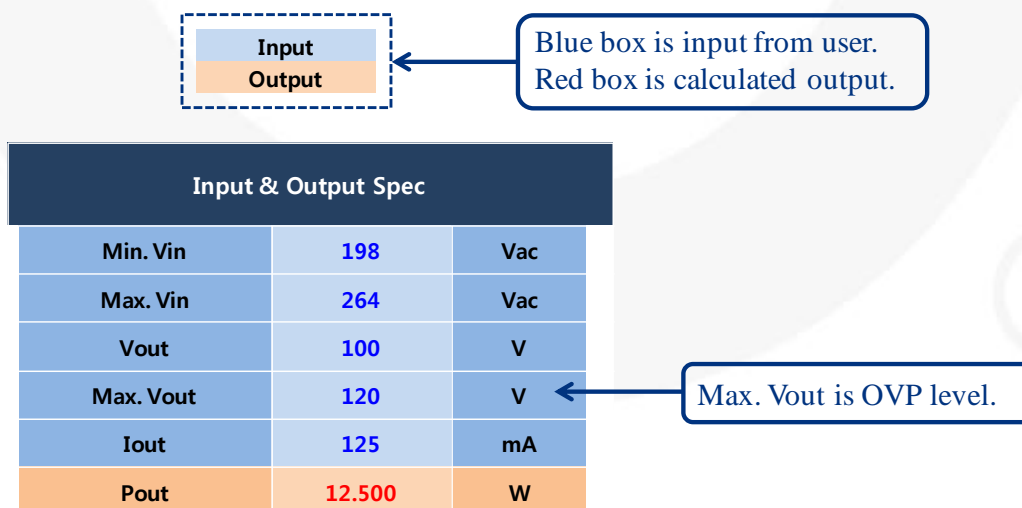


图 1. 设计流程

### 第 1 步 — 输入输入/输出指标



## 第 2 步 — 设计变压器

Transformer Design		
Max. Duty	26	%
Max. Ton	4.727	us
Switching freq.	55	kHz
Efficiency	85	%
Ae	36.6	mm <sup>2</sup>
Bmax	0.25	
Lm	1.638	mH
Np.min	144.667	T
Np	145	T
Na	27.792	T
Nap	0.192	
Vcs.max	0.616	V
Ts	18.182	us
Ton+Tdis	17.964	us

Max. duty is generally between 20 ~ 50%.  
High max. duty → Low conduction loss, Suitable for low-line  
Low max. duty → More Bmax margin, Suitable for high-line

Max.  $t_{on}$  should be less than 10 $\mu$ s.

This switching frequency is the operating frequency at the rated  $V_{OUT}$  condition. The switching frequency should be <65kHz.

Enter Np over Np.min.  
If Np is too big to fit in transformer window, reduce Max. Duty.

Pulse-by-pulse current limit is 0.67V.  
If  $V_{CS,MAX}$  is too close to 0.67V, increase Max. Duty.

$t_{DIS}$  means secondary diode conduction time at peak input voltage. If  $t_{ON}+t_{DIS}$  is longer than  $t_s$ , CRM is shown at peak input voltage area. To operate only in DCM,  $t_{ON}+t_{DIS}$  should be less than  $t_s$ . To make " $t_{ON}+t_{DIS} < t_s$ ", decrease Max. Duty

## 第 3 步 — 设计控制电路

Control Circuit Design		
Rsense	0.762	ohm
Vin.bnk	50	V
Vf	0.5	V
Rvs1	137.631	kohm
Rvs2	15.839	kohm
Cvs	10	pF
Ccomi	1	uF
Cvdd	33	uF
Dvdd Vmax	95.059	V
Rstr	342.857	kohm
Rdummy	400.000	kohm

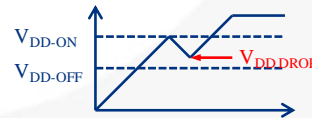
$V_{IN,BNK}$  is  $V_S$  blanking level.  
 $V_S$  blanking:  $V_S$  voltage detection is disabled.  
 $V_{IN,BNK}$  is generally set as 30~70V.

$V_f$  is secondary diode forward voltage.

$C_{VS}$  is  $V_S$  filter capacitor, generally set as 10~30pF.

COMI capacitor is generally 0.68~3.3 $\mu$ F.  
Check output voltage overshoot at startup in max.  $V_{IN}$  condition.  
If output voltage overshoot is too big, increase  $C_{COMI}$ .

$V_{DD}$  capacitor is generally in 10~47 $\mu$ F.  
If  $V_{DD}$  drops too close to  $V_{DD-OFF}$  at startup, increase  $C_{VDD}$ .



$R_{DUMMY}$  helps to maintain over-voltage level at open-LED condition. If output OVP is good, try to increase  $R_{DUMMY}$  to maximize efficiency.

## 第 4 步 — 设计功率器件

Power Device Design		
SW/Dout Vmax	493.352	V
SW/Dout Ipk	0.808	A
Inductor Irms	0.282	A

$V_{MAX}$  is maximum voltage of MOSFET drain-source and output rectifier.

$I_{PK}$  is peak current of MOSFET and output rectifier.

## 相关资源

若要获取设计工具，请访问：

[http://www.fairchildsemi.com/design\\_tools/led-driver-design-tool/](http://www.fairchildsemi.com/design_tools/led-driver-design-tool/)

若要查看产品数据表，请访问：

[FL7732—单级 PFC 初级端调节离线 LED 驱动器](#)

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