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AN-4169

FL7733A 设计工具流程（反激式）

概述

本文件旨在为Fairchild FL7733A 设计工具提供指南。 使用设计工具时，请参考产品数据表。

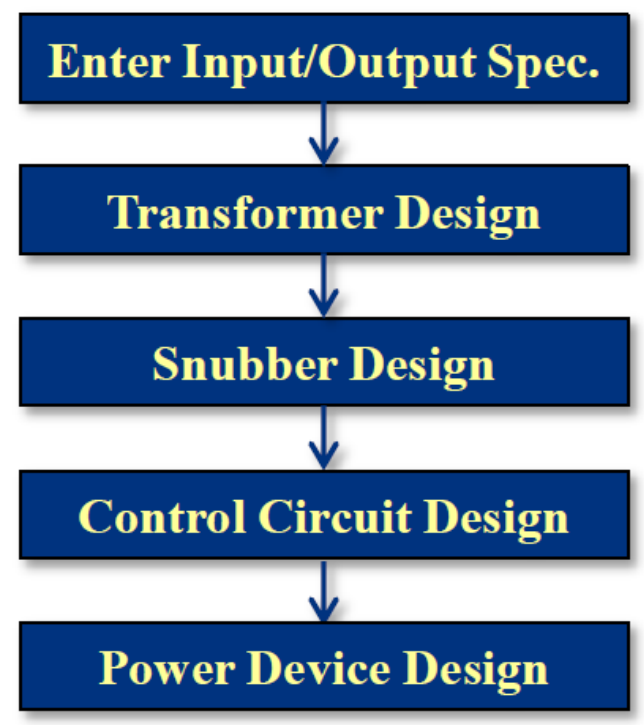
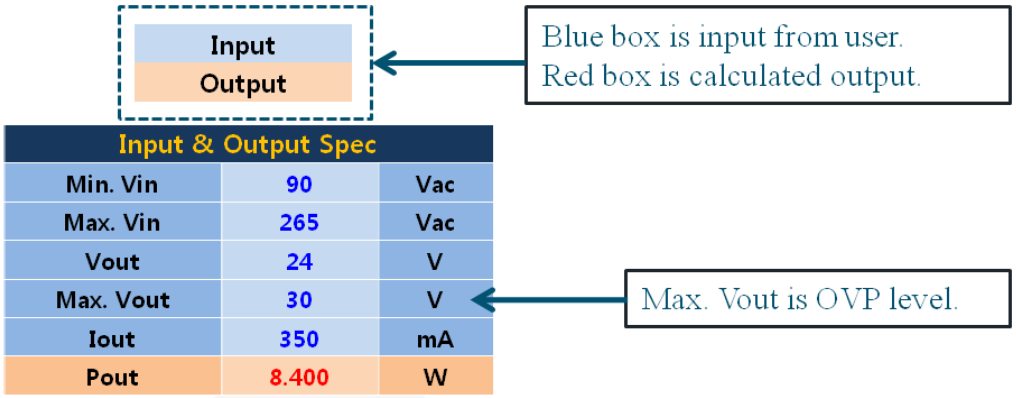


图 1. 设计流程

第 1 步 — 输入输入/输出指标



Input & Output Spec		
Min. Vin	90	Vac
Max. Vin	265	Vac
Vout	24	V
Max. Vout	30	V
Iout	350	mA
Pout	8.400	W

第 2 步 — 设计变压器

Transformer Design		
Max. Duty	40	%
Max. Ton	6.2	us
Switchin freq.	65	kHz
Max. Vcs	0.85	V
Efficiency	86	%
Ae	37	mm^2
Bmax	0.26	
Lm	1.021	mH
Nps	3.101	
Nas	0.767	
Nap	0.247	
Np.min	81.4	T
Np	81	T
Ns	26.1	T
Na	20.0	T

Max. duty is generally between 20 ~ 50%.
High max. duty → Low conduction loss, Suitable for low-line
Low max. duty → More Bmax margin, Suitable for high-line

Max. Ton should be less than 10us.

Pulse by pulse current limit is 1.0 V.
Proper Max.V_{CS} is 0.7 V ~ 0.85 V.

Enter Ae value from Core datasheet.

For safe operation, 0.23 ~ 0.27 is recommended.

Enter Np over Np.min.
If Np is too big to fit in transformer window, reduce Max. Duty.

第3步 — 缓冲电路设计

Snubber Design		
Nps x Vout	83.4	V
Vsn	200	V
ΔVsn	30	V
Rsn	11	kohm
Csn	9	nF

Vsn is snubber voltage.
Vsn is generally set as 2 ~ 2.5 times Nps·Vout

ΔVsn is generally set as 5% ripple of Vsn.

第4步 — 控制电路设计

Control Circuit Design		
Rsense	1.108	ohm
Vin.bnk	50	V
Vf	0.7	V
Rvs1	155	kohm
Rvs2	22	kohm
Cvs	5	pF
Ccomi	1	uF
Cvdd	10	uF

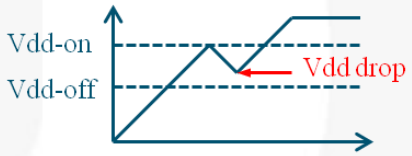
Vin.bnk is VS blanking level.
VS blanking : VS voltage detection is disabled.
Vin.bnk is generally set as 50~70V.

Vf is secondary diode forward voltage.

Cvs is VS filter capacitor, generally set as 5~10pF.

COMI capacitor is generally 0.68~3.3uF.

Vdd capacitor is generally in 10~22uF.
If Vdd drops too close to Vdd-off at startup, increase Cvdd.



第5步 — 功率器件设计

Power Device Design		
MOSFET Vmax	575	V
MOSFET Ipk	4.568	A
Diode Vmax	308	V
Diode Ipk	6.800	A

Vmax is MOSFET drian-source maximum voltage.
Ipk is MOSFET peak current

Vmax is maximum reverse voltage of secondary diode.
Ipk is peak current of secondary diode.

相关资源

若要查看产品数据表，请访问：

FL7733A 一带功率因数校正的初级端调节LED驱动器

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