

# FL7740

## Constant-Voltage Primary-Side-Regulation PWM Controller for Power Factor Correction

The FL7740 provides accurate CV regulation in the steady state with differentiated dynamic function to minimize overshoot and undershoot of output voltage in line and load transient condition. Standby power is less than 0.3 W for smart lighting application and power factor is higher than 0.9 even at half load condition when enabling PF optimizer for wide output power scalability.

Startup time is less than 0.2 sec with built-in high voltage startup circuit and output voltage quickly reaches to the target CV level by loop gain transition technique during startup.

Various protections such as over load, output diode short, sensing resistor short, output short and output over voltage protection guarantee high system reliability.

### Features

- Wide universal input range (90 V<sub>AC</sub> ~ 305 V<sub>AC</sub>)
- Precise CV regulation in the steady state : <math>\pm 3\%</math>
- CV regulation in the load transient : <math>< 10\%</math>
- Overshoot-less fast HV start up time (<math>< 0.2\text{ sec}</math>)
- Low standby power
- PF higher than 0.9 at high-line and half load by PF optimizer
- Pulse-by-pulse current limit
- Output short protection
- Output over voltage protection
- Output diode short protection
- Sensing resistor short & open protection
- Over load protection

### Typical Applications

- LED Lighting System
- AC-DC Adapters, TVs, Monitors
- Off Line Appliances Requiring Power Factor Correction



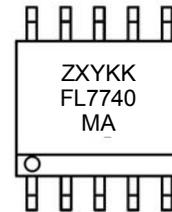
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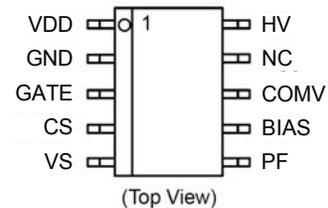
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### MARKING DIAGRAM



Z = Plant code  
M = 1 digit year code  
Y = 1 digit week code  
KK = 2 digit lot traceability code  
M = Package code  
A = Product version

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.



## FL7740

### PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	VDD	IC Supply	IC operating current and MOSFET driving current are supplied using this pin.
2	GND	Ground	Controller ground pin.
3	GATE	PWM Driver Output	This pin uses the internal totem-pole output driver to drive the power MOSFET.
4	CS	Current Sense	Connected to a current sense resistor to detect the MOSFET current for pulse-by-pulse current limit.
5	VS	Voltage Sense	This pin is connected to the auxiliary winding of the transformer via a resistor divider to detect the output voltage.
6	PF	Power Factor	This pin is connected to a resistor to optimize power factor.
7	BIAS	Internal Circuit BIAS	Bypass pin for the internal supply, which powers all control circuitry on the IC.
8	COMV	Loop Compensation	This pin is connected to a capacitor between COMV and GND for compensation.
9	NC	No Connection	
10	HV	High Voltage	This pin is connected to the rectified input voltage via a resistor for fast startup.

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## MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
HV Pin Voltage Range	$V_{HV(MAX)}$	560	V
VDD, GATE Pin Voltage Range	$V_{MV(MAX)}$	-0.3 to 30	V
COMV, PF, BIAS, VS, CS Pin Voltage Range	$V_{LV(MAX)}$	-0.3 to 6	V
VS, CS Pin Negative Pulse Voltage at $I_{LV} < 0.2$ A and $t_{PULSE} < 300$ ns	$V_{LV(PULSE)}$	-1.5	V
Maximum Power Dissipation ( $T_A < 50^\circ\text{C}$ )	$P_{D(MAX)}$	663	mW
Maximum Junction Temperature	$T_{J(max)}$	150	$^\circ\text{C}$
Storage Temperature Range	$T_{STG}$	-55 to 150	$^\circ\text{C}$
Junction-to-Ambient Thermal Impedance	$R_{\theta JA}$	158	$^\circ\text{C/W}$
Junction-to-Case Thermal Impedance	$R_{\theta JC}$	39	$^\circ\text{C/W}$
ESD Capability, Human Body Model (Note 3)	$ESD_{HBM}$	2	kV
ESD Capability, Charged Device Model (Note 3)	$ESD_{CDM}$	2	kV

1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. This device series incorporates ESD protection and is tested by the following methods:  
 ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)  
 ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)  
 Latchup Current Maximum Rating:  $\leq 150$  mA per JEDEC standard: JESD78

## RECOMMENDED OPERATING RANGES (Note 4)

Rating	Symbol	Min	Max	Unit
Ambient Temperature	$T_A$	-40	125	$^\circ\text{C}$

4. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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## ELECTRICAL CHARACTERISTICS

V<sub>DD</sub> = 18 V and T<sub>J</sub> = -40 ~ 125°C unless otherwise specified

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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### VDD Section

Turn-On Threshold Voltage		V <sub>DD-ON</sub>	14.5	16.0	17.5	V
Turn-Off Threshold Voltage		V <sub>DD-OFF</sub>	6.75	7.75	8.75	V
Operating Current	C <sub>LOAD</sub> = 1 nF, V <sub>DD</sub> = 18V	I <sub>DD-OP</sub>	3	5	6.5	mA
Operating Current during Auto Restart		I <sub>DD-AR</sub>	0.3		1	mA
V <sub>DD</sub> Over-Voltage-Protection		V <sub>DD-OVP</sub>	24	25	26	V
V <sub>BIAS</sub> Voltage		V <sub>BIAS</sub>	4.85	5.00	5.15	V

### GATE Section

Output Voltage Low		V <sub>OL</sub>			0.2	V
Output Voltage High	V <sub>DD</sub> = 18 V	V <sub>OH</sub>	17.8			V
Peak Sourcing Current	Design guaranteed C <sub>LOAD</sub> = 1 nF, V <sub>DD</sub> = 20 V C <sub>LOAD</sub> = 1 nF, V <sub>DD</sub> = 23 V	I <sub>source</sub>		180 210		mA
Peak Sinking Current	Design guaranteed C <sub>LOAD</sub> = 1 nF, V <sub>DD</sub> = 20 V C <sub>LOAD</sub> = 1 nF, V <sub>DD</sub> = 23 V	I <sub>sink</sub>		385 435		mA
Rising Time	C <sub>LOAD</sub> = 1 nF	t <sub>r</sub>	110	150	190	ns
Falling Time	C <sub>LOAD</sub> = 1 nF	t <sub>f</sub>	40	60	80	ns

### HV Section

Supply Current From HV Pin	V <sub>HV</sub> = 40 V, V <sub>DD</sub> = 0 V, T <sub>J</sub> = 25 °C	I <sub>HV</sub>	3		9	mA
Leakage Current after Startup		I <sub>HV-LC</sub>		1	10	μA
JFET Regulation Time at Startup	Design guaranteed	t <sub>r-JFET</sub>	400	500	600	ms
V <sub>DD</sub> High Limit during JFET Regulation		V <sub>DD-JFET-HL</sub>	17.5	19.0	20.5	V
V <sub>DD</sub> Low Limit during JFET Regulation		V <sub>DD-JFET-LL</sub>	15.5	17.0	18.5	V

### PWM Section

Min. Turn-on Time Min. Limit	Design guaranteed	T <sub>ON-MIN-MIN</sub>		0.40		μs
Min. Turn-on Time Max. Limit	Design guaranteed	T <sub>ON-MIN-MAX</sub>		2.0		μs
Max. Turn-on Time	Design guaranteed	T <sub>ON-MAX</sub>		23.3		μs

### Oscillator Section

Max. Frequency		f <sub>MAX</sub>	60	65	70	kHz
Min. Frequency		f <sub>MIN</sub>	0.72	0.80	0.88	kHz

### Current Sense Section

Leading-Edge Blanking Time	Design guaranteed	t <sub>LEB</sub>		300		ns
Propagation Delay to GATE	Design guaranteed	t <sub>PD</sub>	50	100	150	ns

### Voltage Sense Section

t <sub>DIS</sub> Blanking Time at VS Sampling	Design guaranteed	t <sub>DIS-BNK</sub>	0.95	1.00	1.05	μs
VS Clamping Voltage	I <sub>VS</sub> =1 mA I <sub>VS</sub> =10 μA	V <sub>VS-CLAMP</sub>	-0.1		0.35	V

### Feedback Section

Reference voltage		V <sub>REF</sub>	3.465	3.5	3.535	V
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# FL7740

## ELECTRICAL CHARACTERISTICS (CONTINUED)

V<sub>DD</sub> = 18 V and T<sub>J</sub> = -40 ~ 125°C unless otherwise specified

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
CV Regulation Tolerance	V <sub>VS</sub> = 3.5 V, T <sub>J</sub> = 25 °C V <sub>VS</sub> = 3.5 V, T <sub>J</sub> = -40~125 °C	CV <sub>REGULATION</sub>	-0.7 -1.2		+0.7 +1.2	%
Transconductance		g <sub>M</sub>	16	20	24	μmho
COMV Sink Current	V <sub>VS</sub> = 4 V	I <sub>COMV-SINK</sub>	8	10	12	μA
COMV Source Current	V <sub>VS</sub> = 3 V	I <sub>COMV-SOURCE</sub>	8	10	12	μA
COMV High Voltage		V <sub>COMV-HGH</sub>	4.7			V
COMV Low Voltage		V <sub>COMV-LOW</sub>			0.1	V

### Start Sequence Section

Soft Start Time	Design guaranteed	t <sub>SOFT-START</sub>		25.6		ms
SS1 Minimum Time	Design guaranteed	t <sub>SS1-MIN</sub>		2		ms
SS1 Maximum Time	Design guaranteed	t <sub>SS1-MAX</sub>		100		ms
SS21 Time	Design guaranteed	t <sub>SS21</sub>		45		ms
SS22 Maximum Time	Design guaranteed	t <sub>SS22</sub>		30		ms

### Dynamic Section

DYN Reference Set Threshold		V <sub>DYN-REF-SET</sub>	0.72	0.80	0.88	V
DYN Reference Set Time	Design guaranteed	t <sub>DYN-REF-SET</sub>		5		μs
OV Reference 5	Design guaranteed	V <sub>OV-REF5</sub>		+20		%
OV Reference 4		V <sub>OV-REF4</sub>	+14	+15	+16	%
OV Reference 3		V <sub>OV-REF3</sub>	+9	+10	+11	%
OV Reference 2		V <sub>OV-REF2</sub>	+4.7	+5.7	+6.7	%
OV Reference 1		V <sub>OV-REF1</sub>	+1.86	+2.86	+3.86	%
UV Reference 1		V <sub>UV-REF1</sub>	-3.86	-2.86	-1.86	%
UV Reference 2		V <sub>UV-REF2</sub>	-6.7	-5.7	-4.7	%
UV Reference 3	Design guaranteed	V <sub>UV-REF3</sub>		-10		%

### Protection Section

Auto Restart Delay Time	Design guaranteed	t <sub>AR</sub>		3		s
VS Ouptut Short Hys. Voltage 'H'		V <sub>VS-OS-H</sub>	0.85	0.90	0.95	V
VS Ouptut Short Hys. Voltage 'L'		V <sub>VS-OS-L</sub>	0.65	0.70	0.75	V
OSP Delay Time	Design guaranteed	t <sub>OSP-DELAY</sub>		35		ms
High Current Limit Threshold		V <sub>CS-HIGH-CL</sub>	1.13	1.20	1.27	V
Low Current Limit Threshold		V <sub>CS-LOW-CL</sub>	0.15	0.20	0.25	V
Over Current Protection Voltage		V <sub>CS-OCP</sub>		1.8		V
CS Threshold Voltage for SRSP		V <sub>CS-SRSP</sub>	0.040	0.075	0.125	V
Max. Turn-on Time for SRSP	I <sub>VS</sub> = 100 uA I <sub>VS</sub> = 700 uA	t <sub>TON-MAX-SRSP</sub>	7.5 1.3	10.0 1.6	12.5 1.9	μs
Threshold Temperature for OTP	Design guaranteed	T <sub>OTP</sub>		150		°C
Junction Temperature Hysteresis	Design guaranteed	T <sub>OTP-HYS</sub>		30		°C

T Y P I C A L C H A R A C T E R I S T I C S

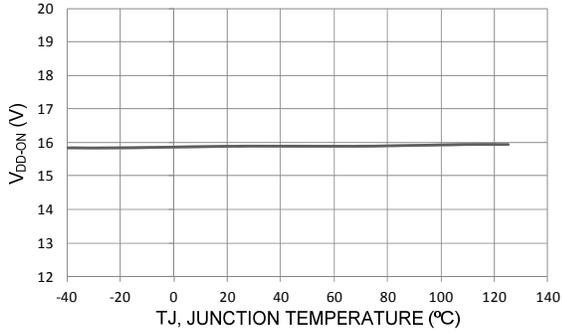


Figure 3 V<sub>DD-ON</sub> vs. Temperature

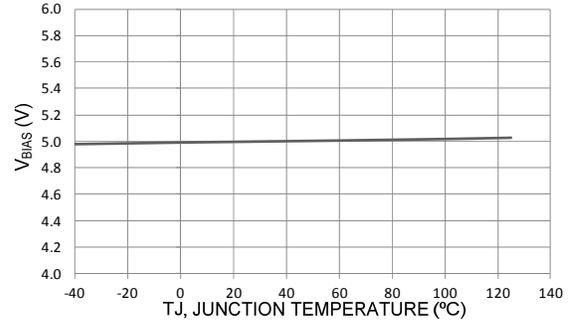


Figure 4 V<sub>BIAS</sub> vs. Temperature

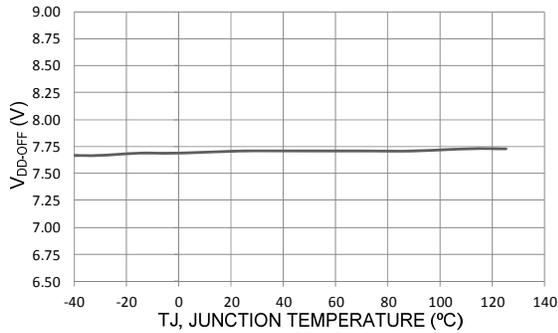


Figure 5 V<sub>DD-OFF</sub> vs. Temperature

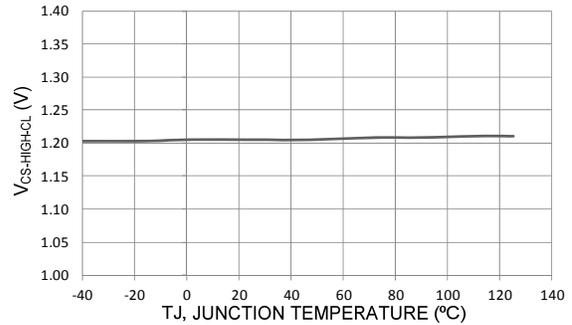


Figure 6 V<sub>CS-HIGH-CL</sub> vs. Temperature

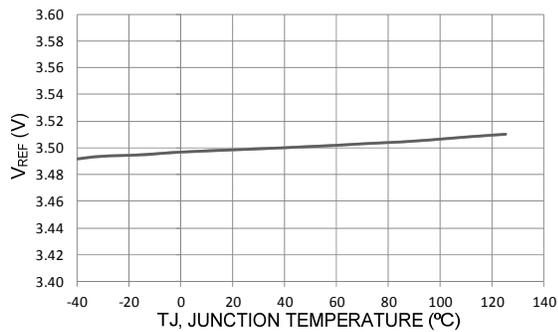


Figure 7 V<sub>REF</sub> vs. Temperature

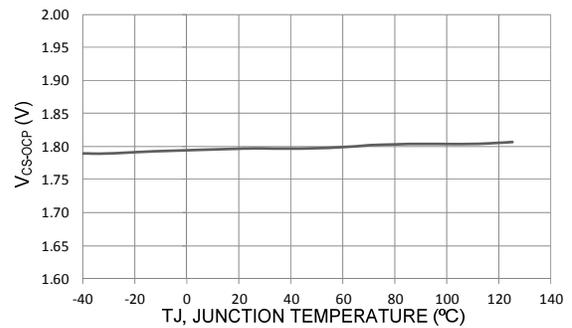


Figure 8 V<sub>CS-OCP</sub> vs. Temperature

T Y P I C A L C H A R A C T E R I S T I C S

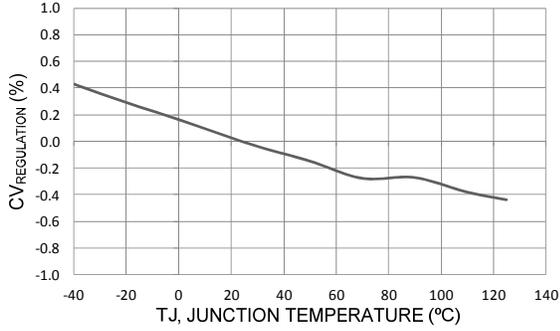


Figure 9  $CV_{REGULATION}$  vs. Temperature

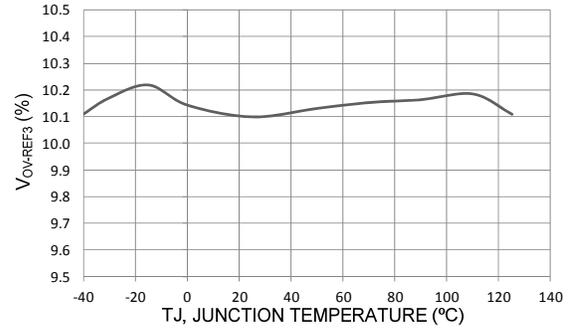


Figure 10  $V_{OV-REF3}$  vs. Temperature

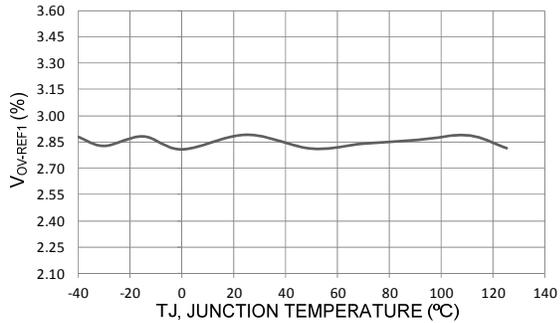


Figure 11  $V_{OV-REF1}$  vs. Temperature

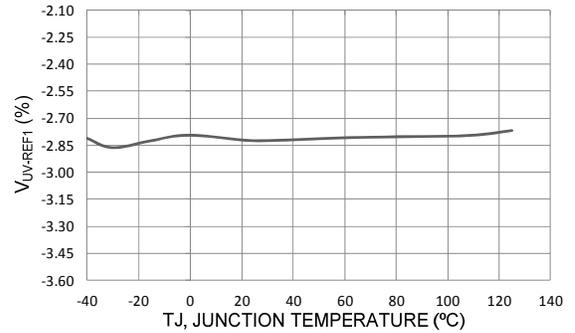


Figure 12  $V_{UV-REF1}$  vs. Temperature

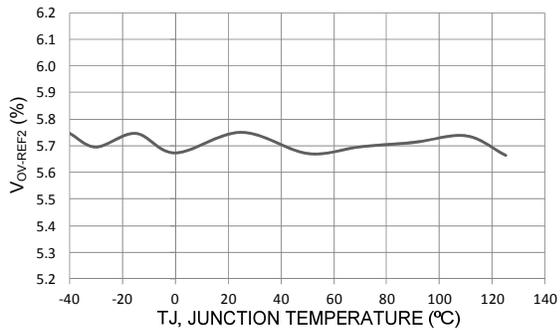


Figure 13  $V_{OV-REF2}$  vs. Temperature

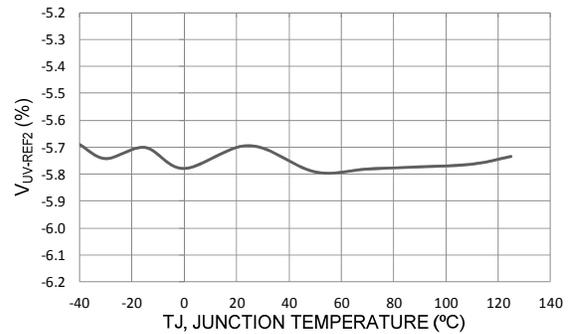


Figure 14  $V_{UV-REF2}$  vs. Temperature

## APPLICATION INFORMATION

### General

FL7740 is high power factor flyback controller with accurate primary side constant voltage regulation for smart LED lighting and AC-DC adapter, TV & monitors application. Precise output voltage detection and dynamic function manage good CV regulation. Startup is fast with internal HV biasing circuit with overshoot-less gain control. It guarantees high system reliable protection functions such as output over voltage, output short, over load, over current and thermal shut down protections.

### Constant Voltage Regulation

VS pin detects output voltage information ( $=V_{EAV}$ ) during secondary side diode conduction time and internal gm amplifier regulates the detected voltage at 3.5 V.

### Dynamic Response at Load Transient

At load transient condition,  $V_{EAV}$  is shortly out of regulation due to the narrow PFC loop bandwidth. When  $V_{EAV}$  is far from 3.5 V regulation reference, duty is quickly changed to bring the  $V_{EAV}$  back to 3.5 V by dynamic control function.

### HV biasing at startup

Internal HV biasing circuit quickly charges external VDD capacitor to begin IC operation at plug-in. After 500 ms initial time, HV biasing stops for low standby power.

### Overshoot-less gain control at startup

Once IC operation starts, feedback loop is dominantly controlled in proportional gain to speed up the output capacitor charging. Once output voltage is settled down close to the regulation target, gain control is smoothly changed to integration gain with no output voltage overshoot.

### Digital PF optimizer

FL7740 compensates input current phase shift caused by EMI filter capacitor current in a half line period. With sophisticated digital PF optimizer, FL7740 significantly improves power factor in the wide load range.

### Pulse-by-pulse current limit

When CS pin voltage reaches to 1.2 V current limit reference, GATE turn-on is terminated to limit primary peak current.

### Auto Restart at Protection

Once protection is triggered, IC operation stops for 3 sec and begin the operation for auto restart.

### Output Short Protection

When  $V_{EAV}$  is less than 0.7 V continuously for 35 ms, output short protection is triggered.

### Output Over Voltage Protection

When  $V_{EAV}$  is higher than  $V_{VS-OVP}$  threshold or VDD is higher than  $V_{DD-OVP}$ , output over voltage protection is triggered.

### Output Diode Short Protection

Once output diode is short circuited, high di/dt in the primary winding is occurred by leakage inductance. Once CS pin voltage reaches to 1.7 V, switching is shut down.

### Sensing Resistor Short Protection

At first switching, sensing resistor short condition is monitored by detecting CS pin voltage. If CS is less than 75 mV during first GATE turn-on time, sensing resistor short protection is triggered.

### Over Load Protection

When output is over loaded, pulse-by-pulse current limit event is occurred. If this event lasts for 60 half line cycles, over load protection is triggered.

### Thermal Shut Down

If internal junction temperature is higher than 150°C, protection is triggered and released with 30°C hysteresis.

**Primary Side Constant Voltage Regulation**

FL7740 utilizes auxiliary winding to detect output voltage during secondary side diode conduction time ( $=T_{DIS}$ ). The true output voltage level without secondary diode forward voltage drop is at the end of secondary diode conduction time. In order to detect the right output voltage, 85% of  $T_{DIS}$  at previous switching cycle is sampling time for  $V_{EAV}$  detection at current switching cycle.

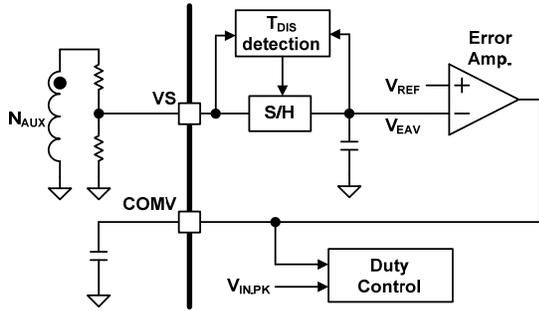


Figure 15. Primary Side Regulation

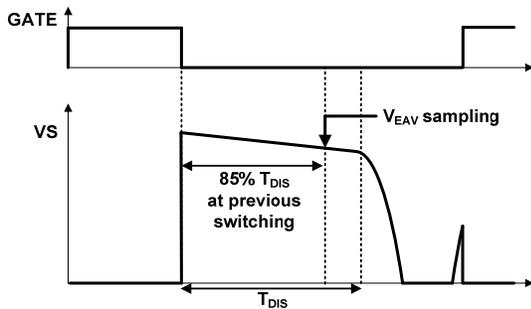


Figure 16.  $V_{EAV}$  Detection

The sampled  $V_{EAV}$  is compared with 3.5 V  $V_{REF}$  at the input of the error amplifier. Several hundreds nF capacitor is connected to the output of the error amplifier at COMV pin to keep feedback loop slow in PFC control. COMV voltage controls duty to regulate  $V_{EAV}$  same as  $V_{REF}$  in the system.

Turn-on time is controlled by both COMV voltage and  $V_{IN.PK}$  information in line feedforward operation in order to keep the constant COMV voltage in the wide input voltage range. So, turn-on time is proportional to COMV voltage and inversely proportional to  $V_{IN.PK}$ .

**Startup**

After plug-in, external VDD capacitor is quickly charged by internal HV biasing supply. Even after VDD is higher than 16 V  $V_{DD.ON}$ , internal HV biasing is still enabled for 500 ms, so HV biasing can relieve VDD capacitor discharging until auxiliary winding builds up VDD voltage.

In order to speed up large output capacitor charging without overshoot, FL7740 starts with proportional gain

during startup sequence (SS1 + SS2) by using internal resistive load at the output of the error amplifier.

In SS1, CCM prevent operation is enabled for the initial 2 ms. When output voltage is 0 V, deep CCM could be entered at initial startup and CS could touch OCP level with startup failure. So, pulse-by-pulse current limit is 0.2 V and switching frequency is 22 kHz during the 2 ms CCM prevent time. Also, duty is gradually increased for 26 ms for soft startup. Once 5 V pulled-up COMV voltage drops less than 4.5 V as  $V_{EAV}$  is close to  $V_{REF}$ , SS1 is ended. Maximum SS1 time is limited up to 100 ms.

In SS2,  $V_{COMV}$  drops from 5 V and goes into p-gain steady state in which  $V_{EAV}$  is little bit lower than  $V_{REF}$  due to the error amplifier input error in p-gain. Once p-gain steady state is settled down in 45 ms, SS2 is finished at min.  $V_{COMV}$  range not to make overshoot when transitioning to i-gain after SS2. FL7740 ends SS2 by monitoring  $V_{IN}$  1.5 ms after  $V_{IN.PK}$  detection moment where  $V_{COMV}$  is generally in the min. range.

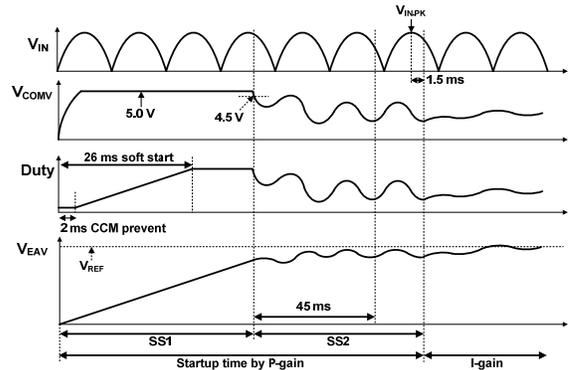


Figure 17. Startup Sequence

**Dynamic CV Regulation**

Due to the narrow loop bandwidth, PFC controller generally does not guarantee good CV regulation at load transient. Especially in secondary side regulation, primary side controller does not know the output voltage level and it only monitors the output of feedback signal through opto-coupler. Therefore, output voltage undershoot is severely happened at no to full load transient in the conventional SSR PFC control.

In order to overcome this, FL7740 utilizes the benefit of PSR with ON semiconductor's proprietary dynamic duty control by monitoring the output voltage. For example, when  $V_{EAV}$  is less than  $V_{UVD.EN}$  (Under Voltage Dynamic Enable threshold), duty is quickly increased not to allow undershoot anymore. Once  $V_{EAV}$  rises higher than  $V_{UVD.DIS}$  (Under Voltage Dynamic Disable threshold), duty quickly drops and follows COMV voltage. During the  $V_{EAV}$  hiccup operation, COMV voltage slowly increases and dynamic operation is terminated when COMV voltage is close to steady state level.

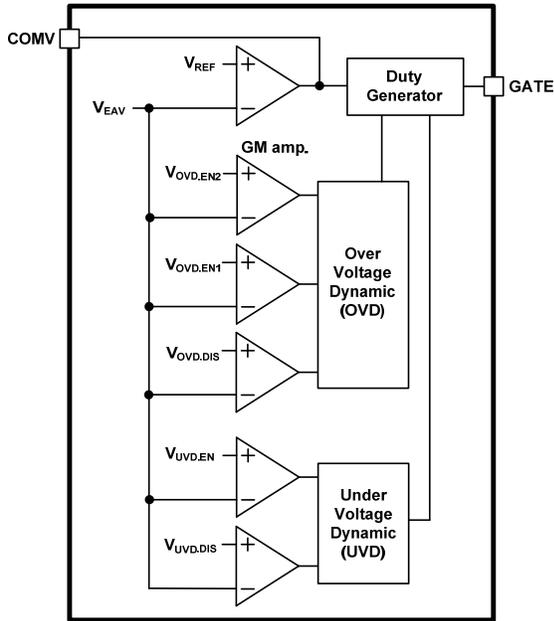


Figure 18. Dynamic Function Block

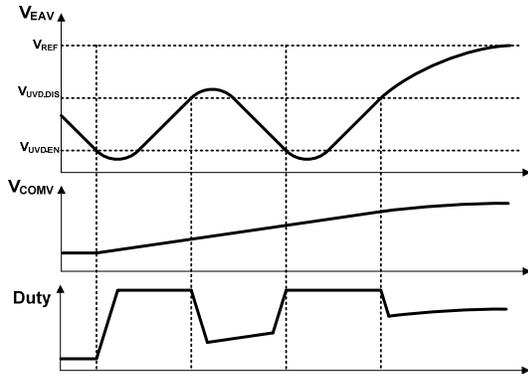


Figure 19. No to full load transient

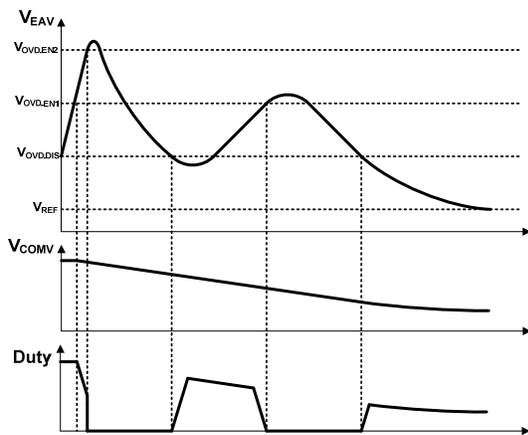


Figure 20. Full to no load transient

In case of OVD (Over Voltage Dynamic) function, it has two enable levels ( $V_{OVD.EN1}$  and  $V_{OVD.EN2}$ ). If output voltage overshoot at load transient is too high,  $V_{EAV}$  increases to  $V_{OVD.EN2}$  passing by  $V_{OVD.EN1}$ . Duty quickly drops when reaching  $V_{OVD.EN1}$  and drops to min. level at once not to allow severe output over voltage when  $V_{EAV}$  increases higher than  $V_{OVD.EN2}$ .

FL7740 provides two sets of dynamic triggering threshold. When user prefers narrow output voltage variation at load transient with large output capacitor, SET0 can be selected without capacitor at PF pin. If wider output voltage variation is allowed and output capacitor should be small due to system size, SET1 can be selected with connection of capacitor around 0.5 nF at PF pin. FL7740 detects capacitance at PF pin at the beginning of switching startup and maintains the SET# until UVLO is triggered. During the 1st switching, PF pin is pulled down to 0 V. In the 2nd switching, PF pull down is disabled and PF voltage is monitored 5 us after 2nd switching period begins. If the PF voltage is higher than 0.8 V  $V_{DYN-REF-SET}$ , SET0 is decided. If not, SET1 is determined.

Dynamic Threshold at SET0 and SET1

	$V_{VS.OVP}$	$V_{OVD.EN2}$	$V_{OVD.EN1}$	$V_{OVD.DIS}$	$V_{UVD.DIS}$	$V_{UVD.EN}$
$V_{OV-REF5} + 20\%V_{REF}$	SET1					
$V_{OV-REF4} + 15\%V_{REF}$	SET0	SET1				
$V_{OV-REF3} + 10\%V_{REF}$		SET0	SET1			
$V_{OV-REF2} + 5.7\%V_{REF}$			SET0	SET1		
$V_{OV-REF1} + 2.9\%V_{REF}$				SET0		
$V_{UV-REF1} - 2.9\%V_{REF}$					SET0	
$V_{UV-REF2} - 5.7\%V_{REF}$					SET1	SET0
$V_{UV-REF3} - 10\%V_{REF}$						SET1

### Digital PF Optimizer

As line voltage increases and output load decreases, PF is degraded due to the effect of EMI filter capacitor charging/discharging current. Input current is the sum of EMI Filter capacitor current and flyback input current. Whether the flyback input current is exactly in-phase sinusoidal current with line voltage, 90° phase shifted EMI filter cap current worsens displacement factor of the overall system input current.

The ON semiconductor's proprietary PF optimizer accurately compensates the EMI filter capacitor current and improves PF more than 0.1 at high line and half load condition.

The calculation coefficient in the PF optimizer is externally programmable by supplying a certain level of voltage at PF pin with external resistive divider from 5 V

BIAS pin. Before 1<sup>st</sup> switching, FL7740 converts the PF voltage into digital value without switching noise and keeps the digital value for the coefficient until UVLO is triggered.

Recommended  $V_{PF}$  is in Equation 1, where  $L_M$  is magnetizing inductance and  $C_{EMI}$  is total EMI filter capacitance.

$$V_{PF} = 5 \times 10^9 \times L_M \times C_{EMI} + 1.5 \quad (\text{eq. 1})$$

As  $V_{PF}$  increases, the coefficient in the PF optimizer calculation is larger with better PF, but THD is worse due to the input current distortion at input voltage zero cross. Therefore,  $V_{PF}$  adjustment by changing PF resistors is recommended to bring the best PF and THD performance to meet user's target. When  $V_{PF}$  is lower than 1.5 V, PF optimizer is disabled.

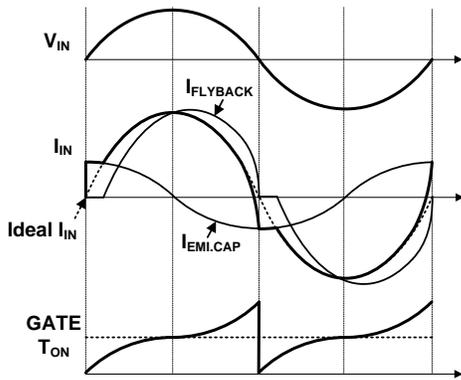


Figure 21. With PF Optimizer

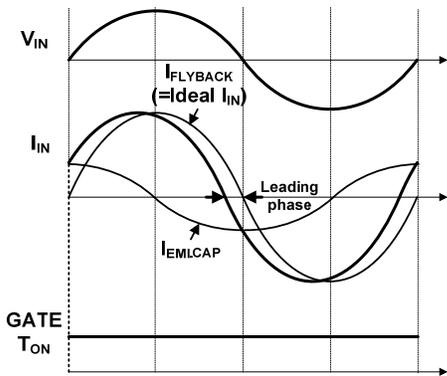


Figure 22. Without PF Optimizer

**Protection**

- Auto-restart

Once protection is triggered, FL7740 terminates switching and internal 3 sec counter makes delay time. In 3 sec, VDD voltage is regulated between 17 V and 19 V by internal HV biasing not to fall in UVLO. After 3 sec, VDD falls down to 7.75 V  $V_{DD-OFF}$  and IC is reset

with released protection. When VDD voltage is up again to 16 V  $V_{DD-ON}$ , FL7740 begins startup sequence.

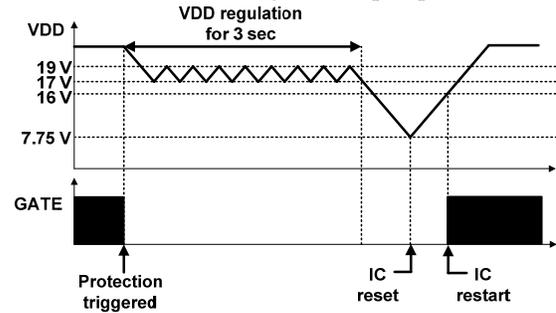


Figure 23. Auto Restart

- Output Over Voltage Protection

Output over voltage is hardly triggered due to the powering limit by dynamic function. But, in the abnormal condition, output OVP is triggered when  $V_{EAV}$  is higher than 4.0 V @ SET0 / 4.2 V @ SET1 for 4 switching cycles or VDD voltage is higher than 25 V for 10 us delay.

- Output Short Protection

At output short condition,  $V_{EAV}$  is less than 0.7 V. If this condition lasts for continuous 35 ms switching time, OSP is triggered.

- Over Current Protection

When CS voltage is higher than 1.8 V over the 1.2 V pulse-by-pulse current limit, protection is immediately triggered. OCP protects output diode short, sensing resistor open and transformer saturation condition.

- Sensing Resistor Short Protection

1<sup>st</sup> switching is 0.2 V current mode. If CS doesn't reach over 75 mV threshold during 1<sup>st</sup> turn-on time, SRSP is triggered. Max. turn-on time at 1<sup>st</sup> switching is inversely proportional to input voltage to limit the primary peak current.

- Over Load Protection

At over load condition, CS reaches to 1.2 V pulse-by-pulse current limit. FL7740 generates internal ZC (Zero Cross) signal and OLP is triggered if the event (1.2V current limit event between the two close ZC signals) is occurred for consecutive 60 ZC signals.

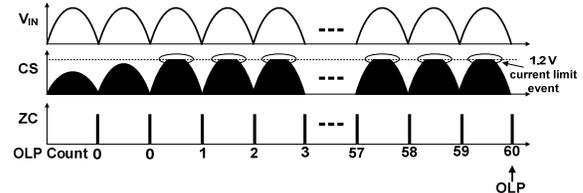
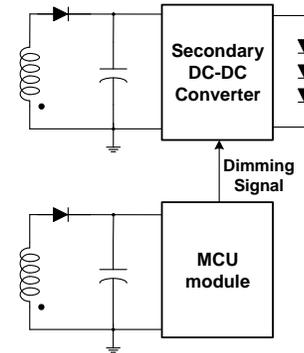
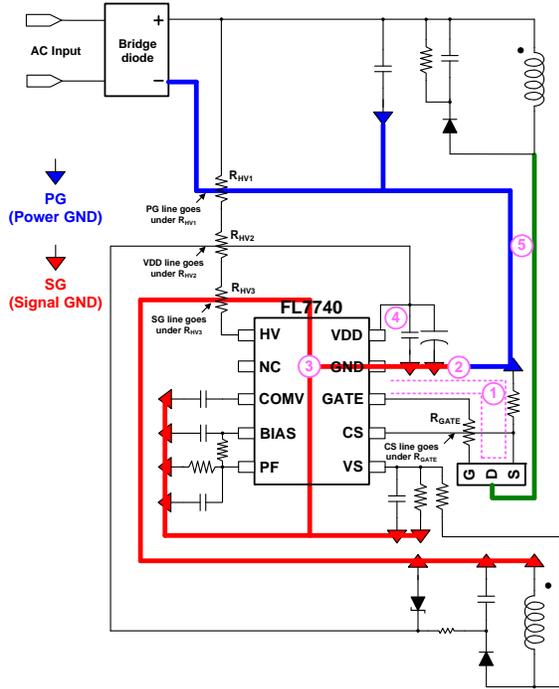


Figure 24. Over Load Protection

- Thermal Shut Down

When internal junction temperature is higher than 150°C, TSD is triggered and protection is released when the junction temperature drops under 120°C.

Single layer PCB layout guidance



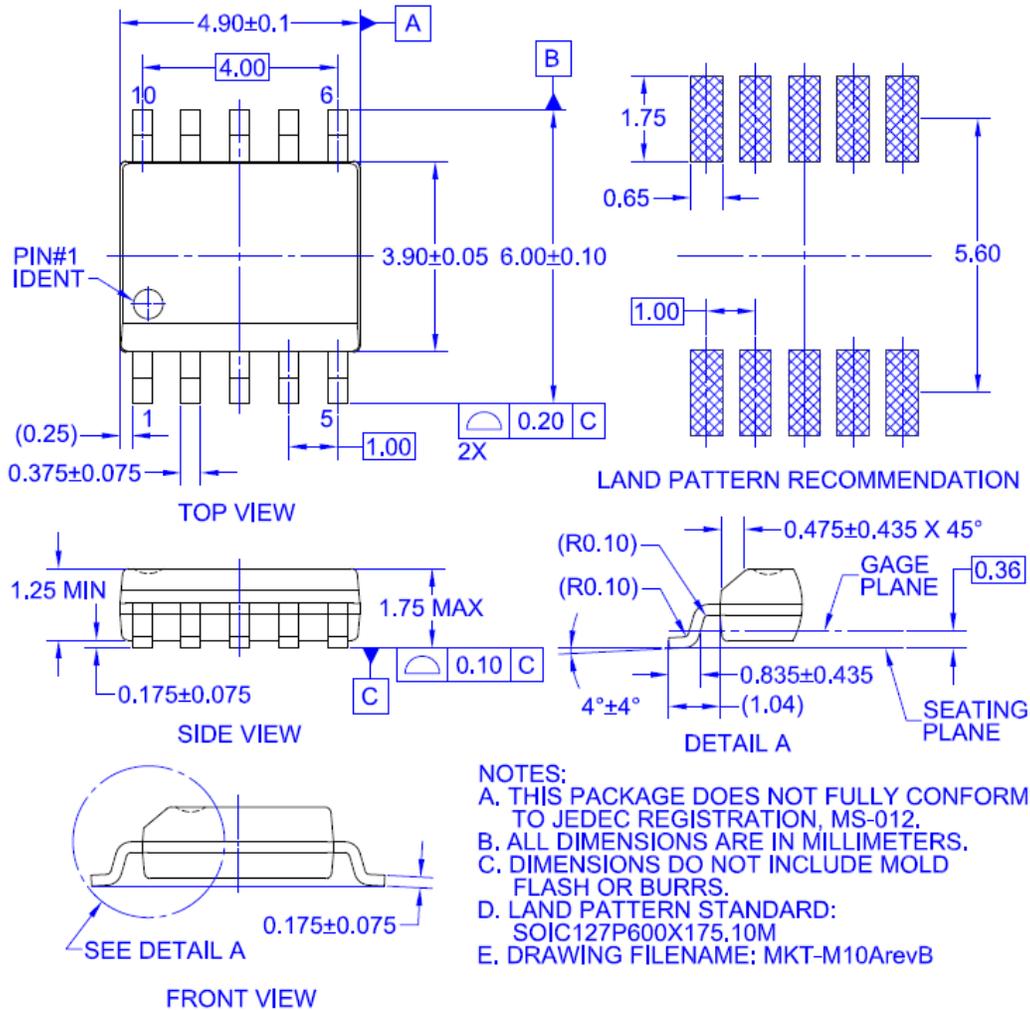
- ① G-GATE and S-GND distance should be short.
- ② SG and PG are connected close at GND pin.
- ③ COMV, BIAS, PF, VS circuit ground and aux. winding VDD circuit ground are connected close at GND pin.
- ④ SMD filter cap is connected close at VDD and GND pin.
- ⑤ Powering lines (Drain and PG) are closely placed and away from FL7740 control circuits.

ORDERING INFORMATION

Device	Package	Shipping
FL7740MX	10 Lead SOIC, JEDEC MS-012, 150" Narrow Body	Tape and Reel

# FL7740

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