

LV8702V



ON Semiconductor®

<http://onsemi.com>

PWM Constant-Current Control High-Efficient Stepper Motor Driver Application Note

Overview

The LV8702V is a 2-channel Full-bridge driver IC that can drive a stepper motor driver, which is capable of micro-step drive and supports quarter step. Current is controlled according to motor load and rotational speed at half step, half step full-torque and quarter step excitation, thereby highly efficient drive is realized. Consequently, the reduction of power consumption, heat generation, vibration and noise is achieved.

Function

- Built-in 1ch PWM current control stepper motor driver (bipolar type)
- Ron (High-side Ron: 0.3Ω, Low-side Ron: 0.25Ω, total: 0.55Ω, Ta = 25°C, IO = 2.5A)
- Micro step mode is configurable as follows: full step/half step full-torque/half step/quarter step
- Excitation step moves forward only with step signal input
- Built-in output short protection circuit (latch method)
- Control power supply is unnecessary
- Built-in high-efficient drive function (supports half step full-torque/half step/quarter step excitation mode)
- Built-in step-out detection function (Step-out detection may not be accurate during high speed rotation)
- BiCDMOS process IC
- IO max=2.5A
- Built-in thermal shut down circuit

Typical Applications

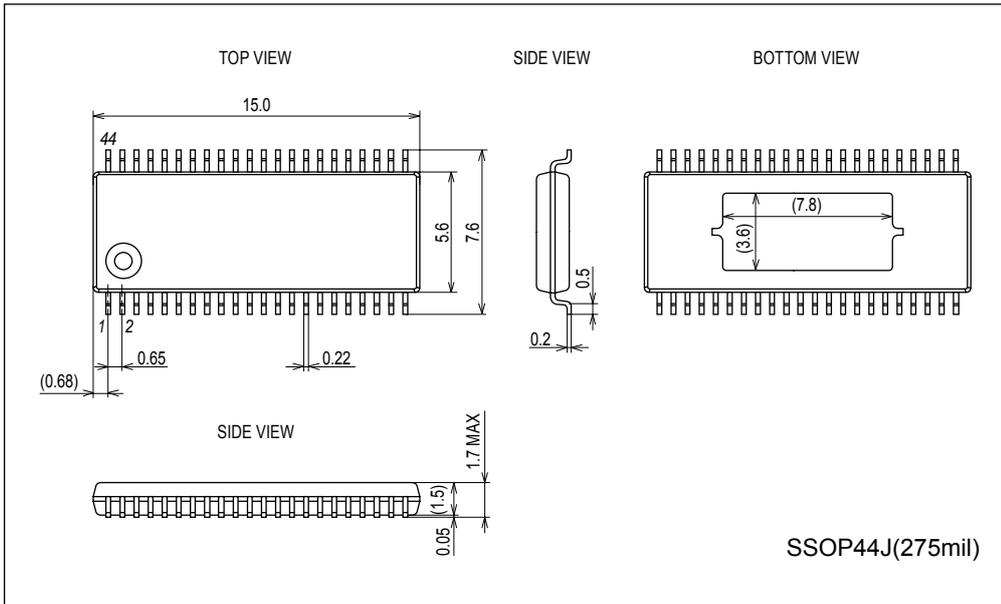
- MFP (Multi Function Printer)
- PPC (Plain Paper Copier)
- Scanner
- Industrial
- Amusement
- Textile

LV8702V Application Note

Package Dimensions

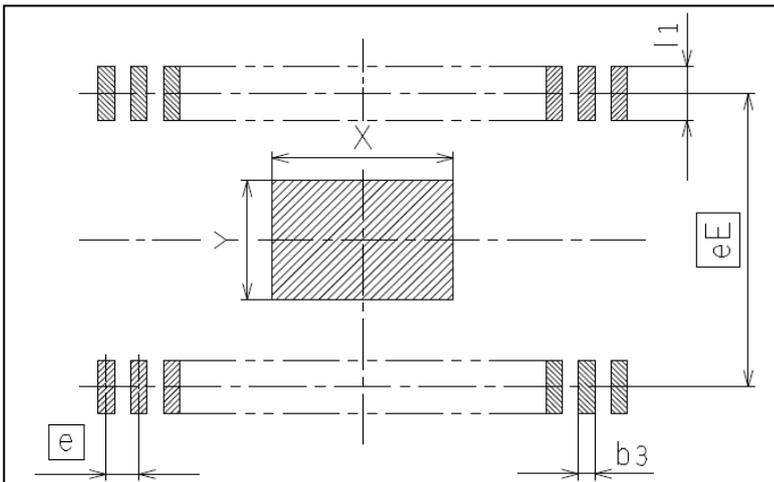
unit : mm (typ)

3285B



Caution: The package dimension is a reference value, which is not a guaranteed value

Recommended Soldering Footprint

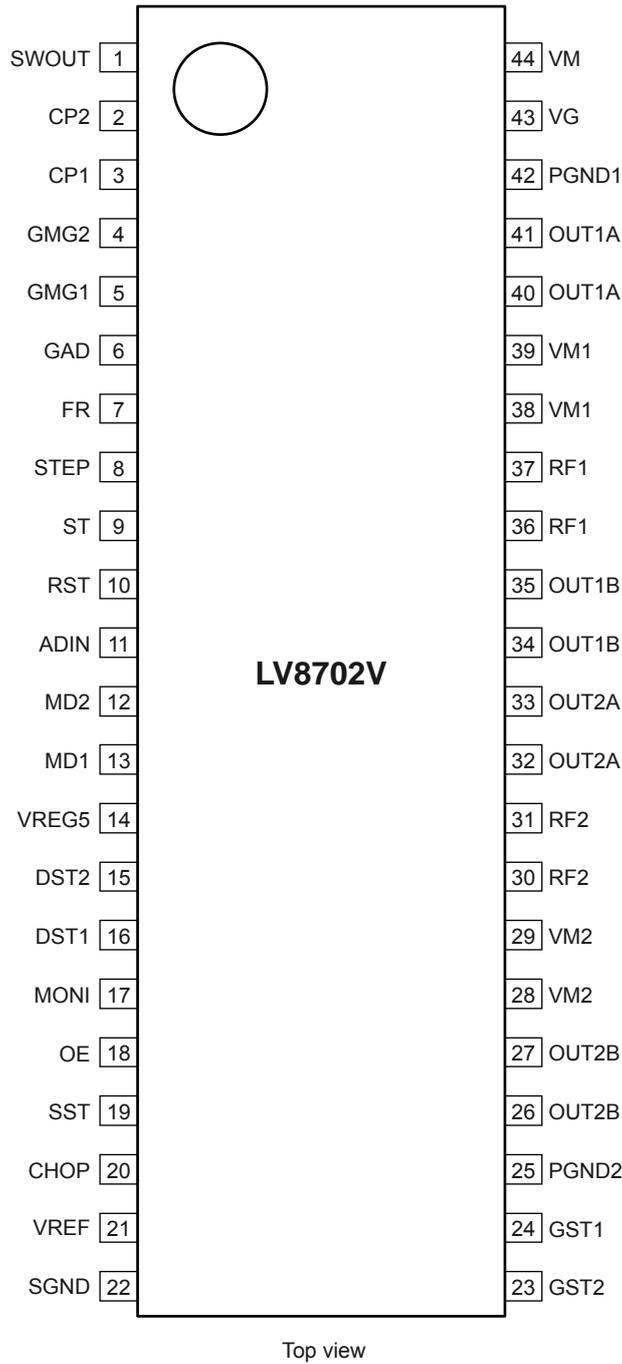


(Unit: mm)

Reference symbol	SSOP44J(275mil)
eE	7.00
e	0.65
b3	0.32
l1	1.00
X	(7.8)
Y	(3.5)

LV8702V Application Note

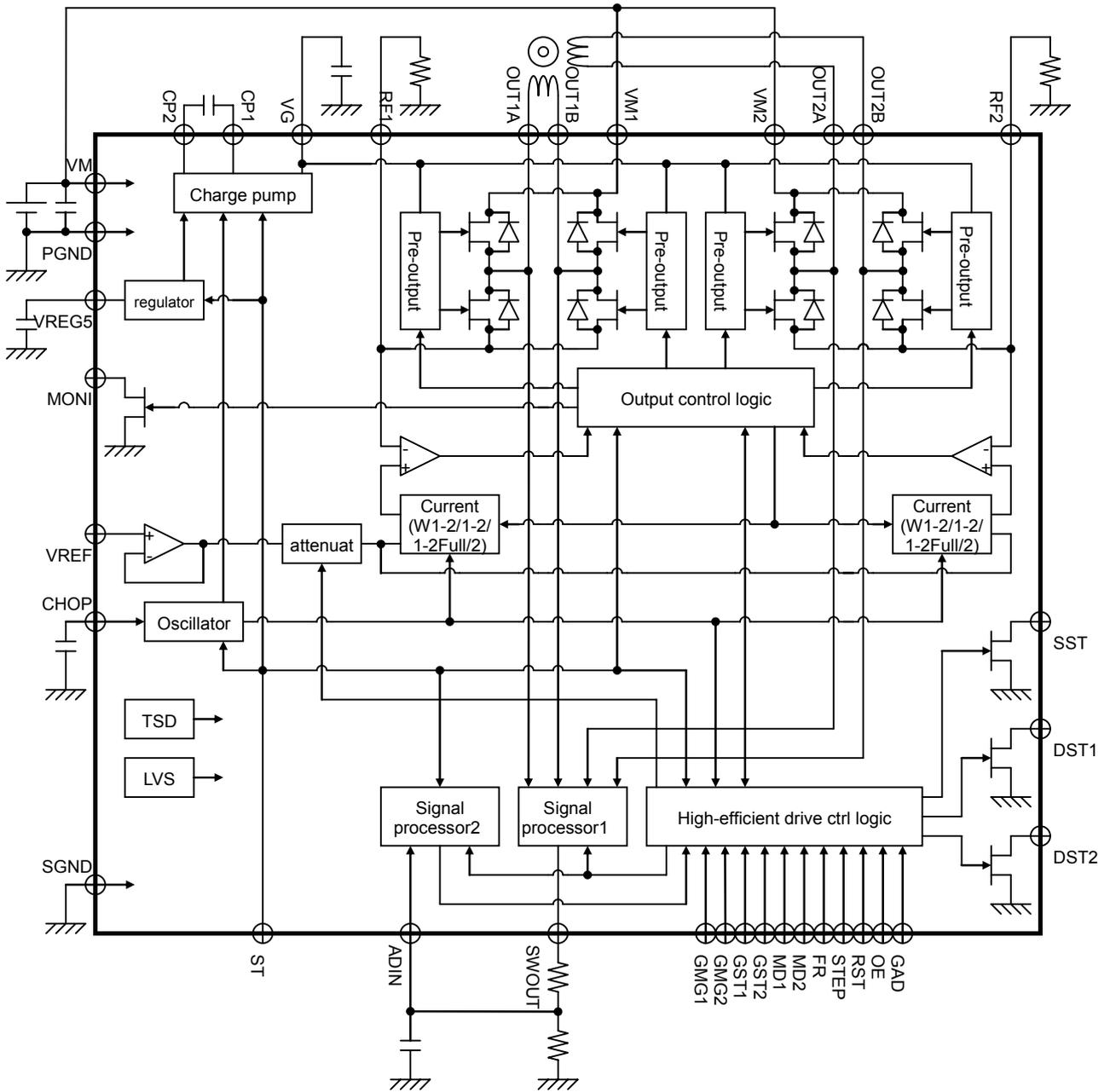
Pin Assignment



It is short-circuited in IC though there are VM1, VM2, OUT1A, OUT1B, OUT2A, OUT2B, RF1 and RF2 of each of two pins.

LV8702V Application Note

Block Diagram



LV8702V Application Note

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VM max	VM , VM1 , VM2	36	V
Output peak current	IO peak	tw ≤ 10ms, duty 20%	3	A
Output current	IO max	Per 1ch	2.5	A
Logic input voltage	VIN max	GMG1, GMG2 , GAD , FR , STEP , ST , RST , MD1 , MD2 , OE , GST1 , GST2	-0.3 to +6	V
DST1, DST2, MONI, SST input voltage	Vdst1, Vdst2, Vmoni, Vsst		-0.3 to +6	V
Allowable power dissipation	Pd max	Ta≤25°C *	5.5	W
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified circuit board: 90.0mm×90.0mm×1.6mm, glass epoxy 4-layer board, with backside mounting.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

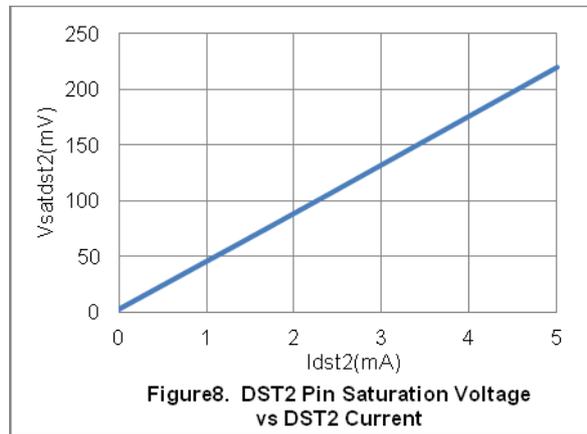
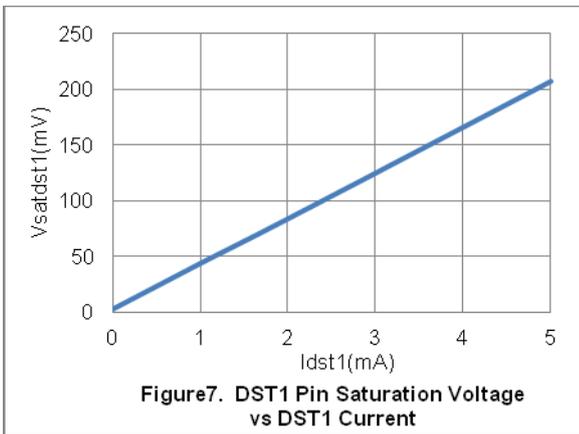
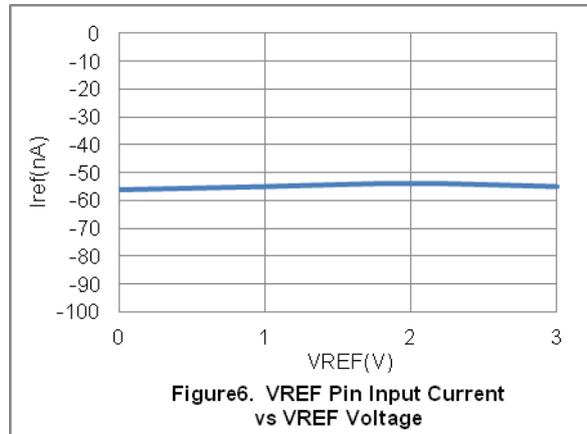
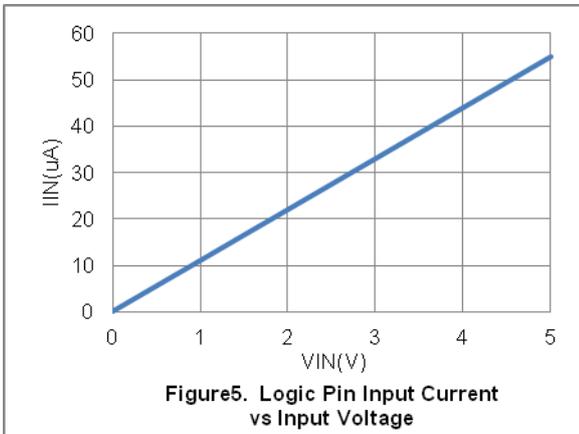
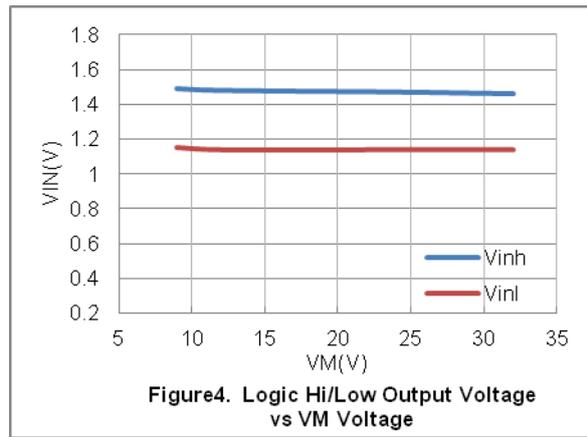
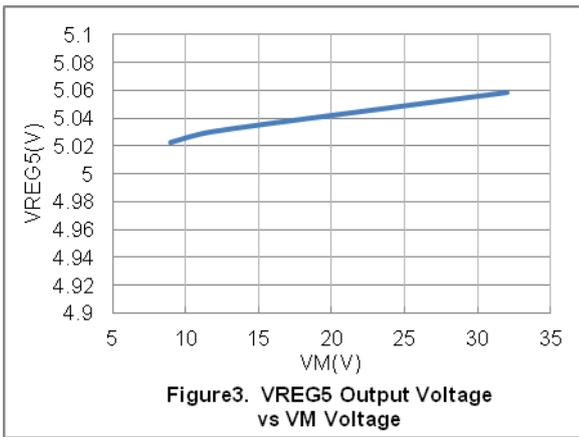
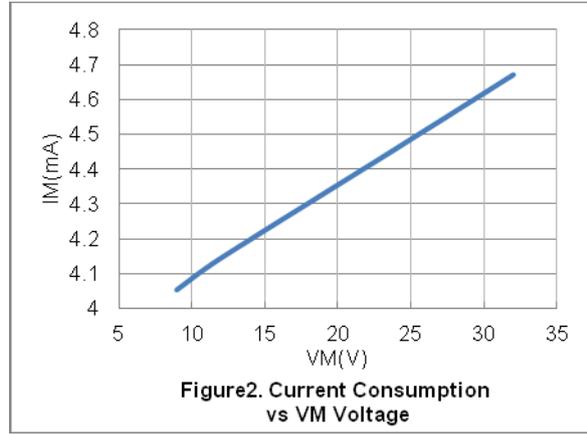
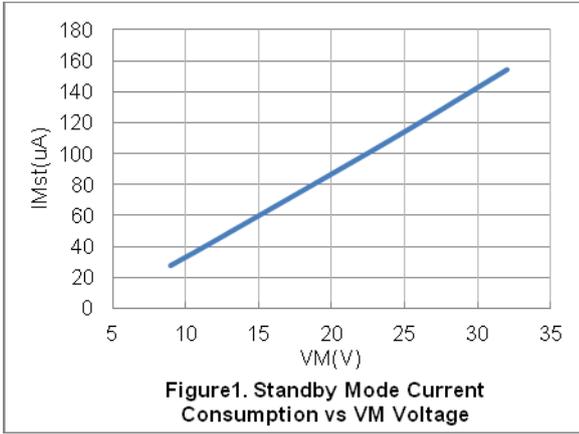
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage range	VM	VM , VM1 , VM2	9		32	V
Logic input voltage	VIN	GMG1 , GMG2 , GAD , FR , STEP , ST , RST , MD1 , MD2 , OE , GST1 , GST2	0		5.5	V
Range of VREF input voltage	VREF		0		3	V

LV8702V Application Note

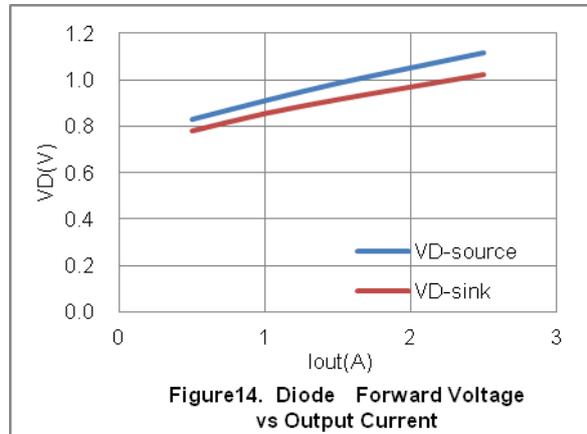
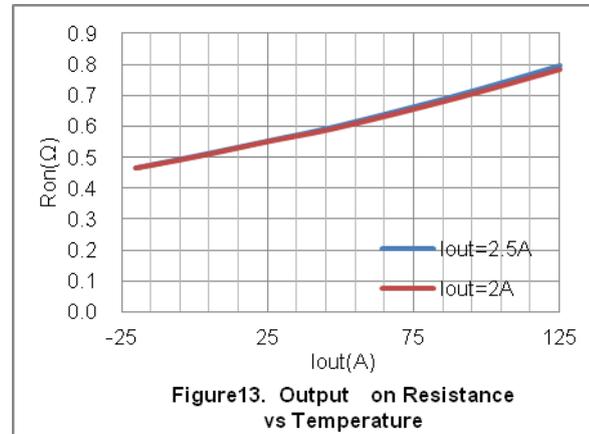
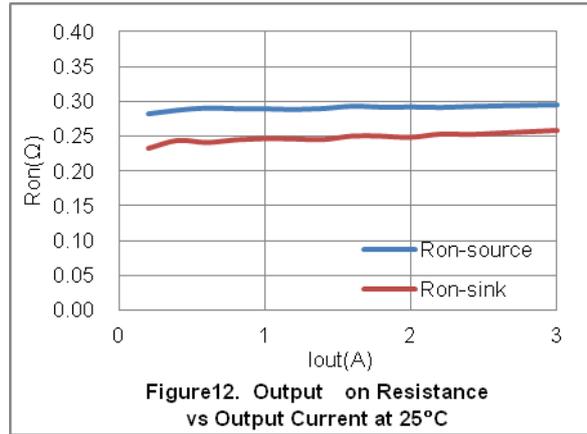
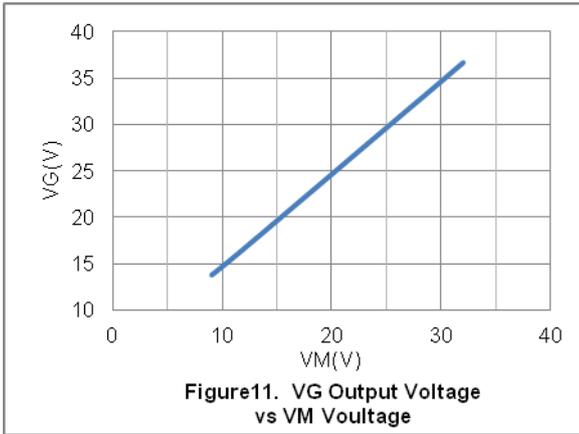
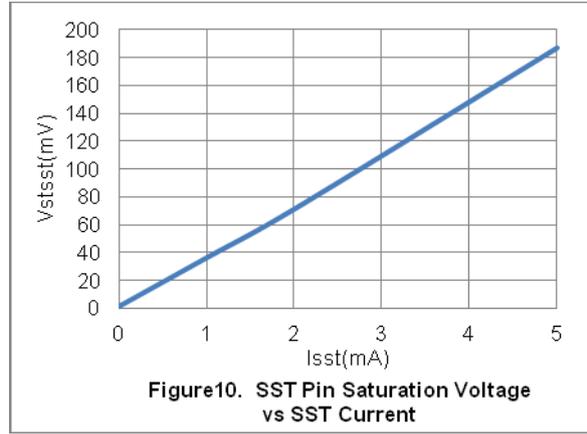
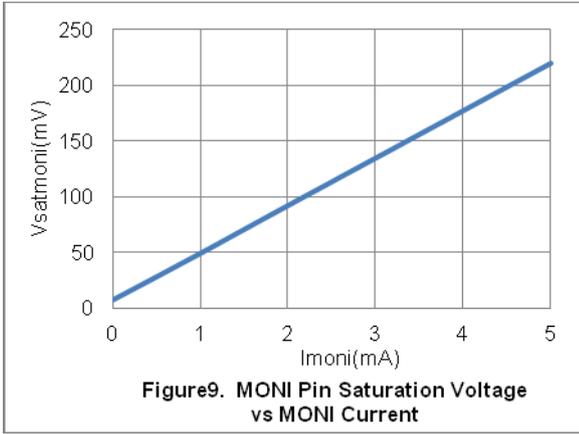
Electrical Characteristics at Ta = 25°C, VM = 24V, VREF = 1.5V

Parameter	Symbol	Conditions	Ratings			Unit	
			min	typ	max		
Consumption current during standby	IMstn	ST = "L" , I(VM)+I(VM1)+I(VM2)		110	400	μA	
Consumption current	IM	ST = "H", OE = "L", STEP = "L", non-load I(VM)+I(VM1)+I(VM2)		4.5	6.5	mA	
VREG5 output voltage	VREG5	IO = -1mA	4.5	5	5.5	V	
Thermal shutdown temperature	TSD	Design certification	150	180	210	°C	
Thermal hysteresis width	ΔTSD	Design certification		40		°C	
Motor driver							
Output on resistor	Ronu	IO = 2.5A, Source-side Ron		0.3	0.4	Ω	
	Rond	IO = 2.5A, Sink-side Ron		0.25	0.33	Ω	
Output leak current	IOleak	VM = 32V			50	μA	
Forward diode voltage	VD	ID = -2.5A		1.2	1.4	V	
Logic pin input current	IINL	VIN = 0.8V	GMG1 , GMG2 , GAD , FR , STEP , ST , RST , MD1 , MD2 , OE , GST1 , GST2	4	8	12	μA
	IINH	VIN = 5V		30	50	70	μA
ADIN pin input voltage	Vadin	Ra2 = 100kΩ, refer to page 24	0		12	V	
Logic input voltage	High	VINH	GMG1 , GMG2 , GAD , FR , STEP , ST , RST , MD1 , MD2 , OE , GST1 , GST2	2.0		5.5	V
	Low	VINL		0		0.8	V
Current selection reference voltage level	quarter step	Vtdac0_W	Step0 (initial status, 1ch comparator level)	290	300	310	mV
		Vtdac1_W	Step1 (initial + 1)	264	276	288	mV
		Vtdac2_W	Step2 (initial + 2)	199	210	221	mV
		Vtdac3_W	Step3 (initial + 3)	106	114	122	mV
	half step	Vtdac0_H	Step0 (initial status, 1ch comparator level)	290	300	310	mV
		Vtdac2_H	Step2 (initial + 1)	199	210	221	mV
	half step (full-torque)	Vtdac0_HF	Step0 (initial status, 1ch comparator level)	290	300	310	mV
		Vtdac2'_HF	Step2' (initial + 1)	290	300	310	mV
full step	Vtdac2'_F	Step2' (initial status, 1ch comparator level)	290	300	310	mV	
Chopping frequency	Fchop	Cchop = 200pF	35	50	65	kHz	
CHOP pin charge/discharge current	Ichop		7	10	13	μA	
Chopping oscillation circuit threshold voltage	Vtup		0.8	1	1.2	V	
	Vtdown		0.4	0.5	0.6	V	
VREF pin input current	Iref	VREF = 1.5V	-0.5			μA	
DST1, DST2, MONI, SST pin saturation voltage	Vsatmoni Vsatsst	ldst1 = ldst2 = lmoni = lsst = 1mA			400	mV	
Charge pump							
VG output voltage	VG		28	28.7	29.8	V	
Rise time	tONG	VG = 0.1μF			500	μS	
Oscillator frequency	Fosc		90	125	160	kHz	

LV8702V Application Note



LV8702V Application Note



LV8702V Application Note

Pin Functions

Pin No.	Pin Name	Pin Function	Equivalent Circuit
4 5 6 7 8 10 12 13 18 23 24	GMG2 GMG1 GAD FR STEP RST MD2 MD1 OE GST2 GST1	Driving capability margin adjuster pin 2. Driving capability margin adjuster pin 1. High-efficient drive switching pin. CW / CCW signal input pin. STEP signal input pin. RESET signal input pin. Excitation mode switching pin 2. Excitation mode switching pin 1. Output enable signal input pin. Boost-up adjuster pin 2. Boost-up adjuster pin 1.	
9	ST	Chip enable pin.	
25 26, 27 28, 29 30, 31 32, 33 34, 35 36, 37 38, 39 40, 41 42	PGND2 OUT2B VM2 RF2 OUT2A OUT1B RF1 VM1 OUT1A PGND1	Channel 2 power system ground. Channel 2 OUTB output pin. Channel 2 motor power supply connection pin. Channel 2 current-sense resistor connection pin. Channel 2 OUTA output pin. Channel 1 OUTB output pin. Channel 1 current-sense resistor connection pin. Channel 1 motor power supply connection pin. Channel 1 OUTA output pin. Channel 1 power system ground.	

Continued on next page.

LV8702V Application Note

Continued from preceding page.

Pin No.	Pin Name	Pin Function	Equivalent Circuit
2 3 43 44	CP2 CP1 VG VM	Charge pump capacitor connection pin. Charge pump capacitor connection pin. Charge pump capacitor connection pin. Motor power supply connection pin.	
21	VREF	Constant current control reference voltage input pin.	
14	VREG5	Internal power supply capacitor connection pin.	

Continued on next page.

LV8702V Application Note

Continued from preceding page.

Pin No.	Pin Name	Pin Function	Equivalent Circuit
15 16 17 19	DST2 DST1 MONI SST	Drive status warning output pin 2. Drive status warning output pin 1. Position detection monitor pin. Motor stop detection output pin.	<p style="text-align: center;">Equivalent Circuit</p>
20	CHOP	Chopping frequency setting capacitor connection pin.	
1	SWOUT	Control signal output pin.	

Continued on next page.

LV8702V Application Note

Continued from preceding page.

Pin No.	Pin Name	Pin Function	Equivalent Circuit
11	ADIN	Control signal input pin.	<p>The diagram shows the equivalent circuit for the ADIN pin. It features a signal source connected to a $2k\Omega$ resistor. The other end of this resistor is connected to the input of a CMOS inverter. The output of this inverter is connected to a $2pF$ capacitor and the input of a second CMOS inverter. The output of the second inverter is also connected to a $2pF$ capacitor. The circuit is powered by VM and GND rails, with protection diodes and a $100k\Omega$ pull-down resistor connected to GND.</p>
22	SGND	Signal ground.	

Description of operation

Input Pin Function

Each input terminal has the function to prevent the flow of the current from an input to a power supply. Therefore, Even if a power supply (VM) is turned off in the state that applied voltage to an input terminal, the electric current does not flow into the power supply.

(1) Chip enable function

The mode of the IC is switched with ST pin between standby and operation mode. In standby mode, the IC is set to power saving mode and all the logics are reset. During standby mode, the operation of the internal regulator circuit and the charge pump circuit are stopped.

ST	Mode	Internal regulator	Charge pump
Low or Open	Standby mode	Standby	Standby
High	Operating mode	Operating	Operating

(2) STEP pin function

The excitation step progresses by inputting the step signal to the STP pin.

Input		Operating mode
ST	STEP	
Low or Open	X*	Standby mode
High		Excitation step proceeds
High		Excitation step is kept

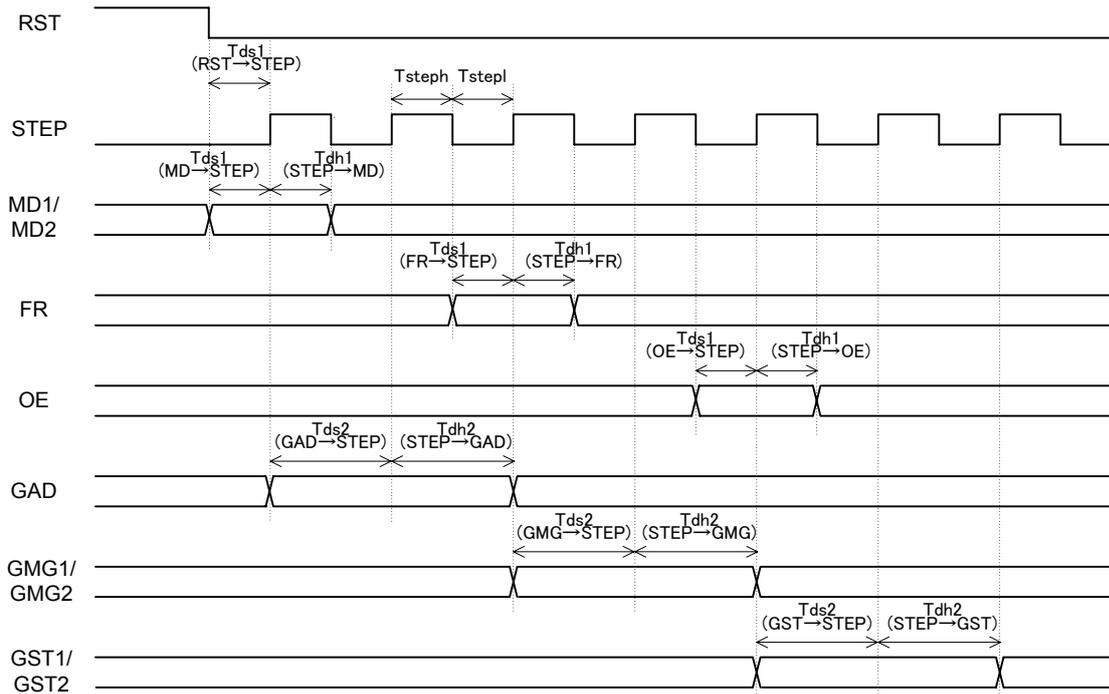
*: Don't care

STEP input MIN pulse width (common in H/L): 12.5us (MAX input frequency: 40kHz)

However, constant current control is performed by PWM during chopping period, which is set by the capacitor connected between CHOP and GND. You need to perform chopping more than once per step. For this reason, for the actual STEP frequency, you need to take chopping frequency and chopping count into consideration.

For example, if chopping frequency is 50kHz (20μs) and chopping is performed twice per step, the maximum STEP frequency is obtained as follows: $f = 1 / (20\mu s \times 2) = 25\text{kHz}$.

(3) Input timing



T_{stepH}/T_{stepL} : Clock H/L pulse width (min 12.5us)
 T_{ds1} : Data set-up time (min 12.5us)
 T_{dh1} : Data hold time (min 12.5us)
 T_{ds2} : Data set-up time (min 25us)
 T_{dh2} : Data hold time (min 25us)

Figure 15. Input timing chart

(4) Position detection monitoring function

The MONI position detection monitoring pin is of an open drain type. When the excitation position is in the initial position, the MONI output is placed in the ON state. (Refer to "Examples of current waveforms in each micro-step mode.")

(5) Setting constant-current control reference current

This IC is designed to automatically exercise PWM constant-current chopping control for the motor current by setting the output current. Based on the voltage input to the VREF pin and the resistance connected between RF and GND, the output current that is subject to the constant-current control is set using the calculation formula below:

$$I_{OUT} = (VREF/5) / RF \text{ resistance}$$

The above setting is the output current at 100% of each excitation mode.

For example, where $VREF=1.5V$ and RF resistance 0.2Ω , we obtain output current as follows.

$$I_{OUT} = 1.5V/5/0.2\Omega = 1.5A$$

When high-efficient drive function is on, I_{OUT} is adjusted automatically within the range of the current value set by $VREF$.

If $VREF$ is open or the setting is out of the recommendation operating range, output current will increase and you cannot set constant current under normal condition. Hence, make sure that $VREF$ is set in accordance with the specification.

However, if current control is not performed (if the IC is used by saturation drive) make sure that the setting is as follows: $VREF=5V$ or $VREF=VREG5$

Power dissipation of RF resistor is obtained as follows: $Pd=I_{out}^2 \times RF$. Make sure to take allowable power dissipation into consideration when you select RF resistor.

(6) Reset function

RST	Operating mode
Low or Open	Normal operation
High	Reset state

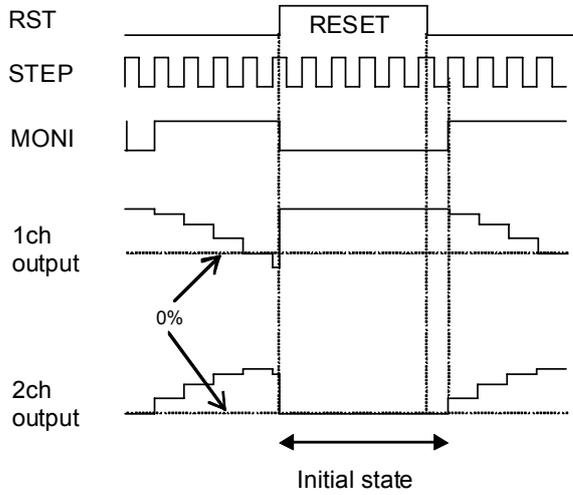


Figure 16. Reset operation

When RST pin = "H", the excitation position of the output is set to the initial position forcibly and MONI output is turned on. And then by setting RST = "L", the excitation position moves forward with the next step signal.

(7) Output enable function

OE	Operating mode
Low or Open	Output ON
High	Output OFF

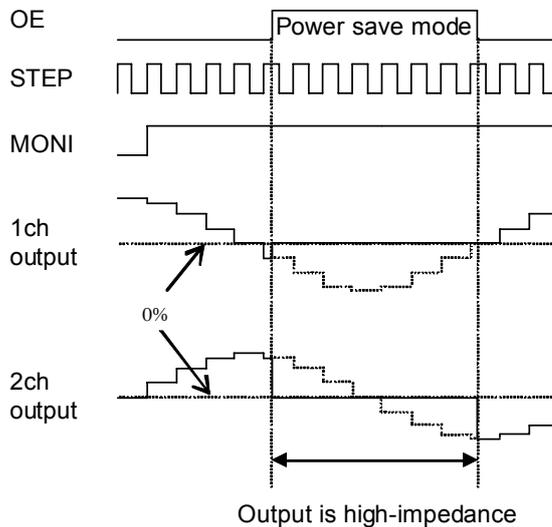


Figure 17. Output enable operation

When OE pin = "H", the output is turned off forcibly and becomes a high-impedance output. However, since the internal logic circuit is in operation, an excitation position moves forward if step signal is input to STEP pin. Therefore, by setting back to OE = "L", the output pin outputs signal based on the excitation position by step signal.

LV8702V Application Note

(8) Excitation mode setting function

MD1	MD2	Micro-step resolution (Excitation mode)	Initial position	
			Channel 1	Channel 2
Low or Open	Low or Open	Full step (2 phase excitation)	100%	-100%
High	Low or Open	Half step (1-2 phase excitation)	100%	0%
Low or Open	High	1/4 step (W1-2 phase excitation)	100%	0%
High	High	Half step full-torque (1-2 phase full-torque excitation)	100%	0%

The position of excitation mode is set to the initial position when: 1) a power is supplied and 2) counter is reset in each excitation mode.

During full step excitation mode, high-efficient drive function is turned off even when GAD = "H".

(9) Forward/Reverse switching function

FR	Operating mode
Low or Open	Clockwise (CW)
High	Counter-clockwise (CCW)

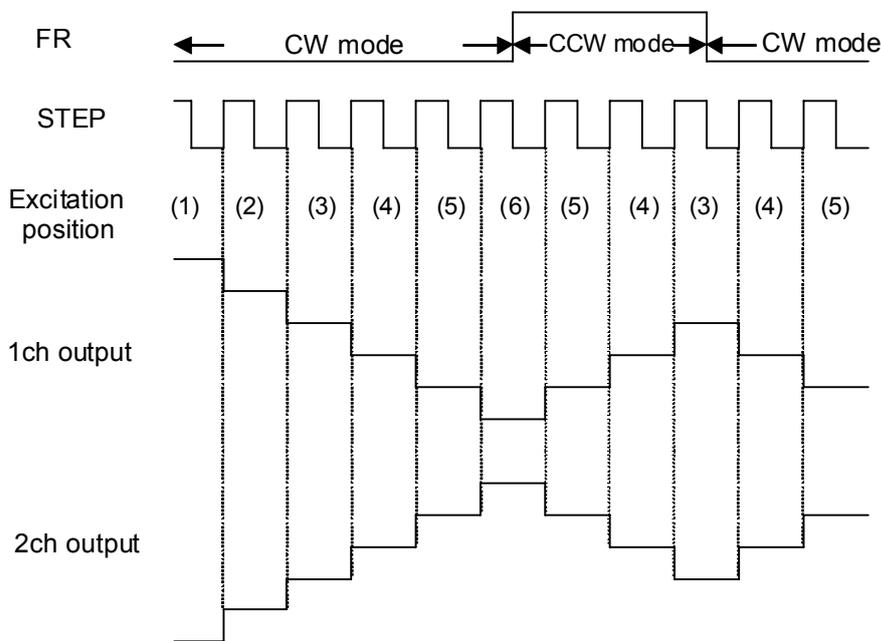


Figure 18. FR operation

The internal D/A converter proceeds by one bit at the rising edge of the input STEP pulse.

In addition, CW and CCW mode are switched by setting the FR pin.

In CW mode, the channel 2 current phase is delayed by 90° relative to the channel 1 current.

In CCW mode, the channel 2 current phase is advanced by 90° relative to the channel 1 current.

(10)Chopping frequency setting

For constant-current control, this IC performs chopping operations at the frequency determined by the capacitor (Cchop) connected between the CHOP pin and GND.

The chopping frequency is set as shown below by the capacitor (Cchop) connected between the CHOP pin and GND.

$$F_{\text{chop}} = I_{\text{chop}} / (C_{\text{chop}} \times V_{\text{tchop}} \times 2) \quad (\text{Hz})$$

I_{chop} : Capacitor charge/discharge current, typ 10 μ A

V_{tchop} : Charge/discharge hysteresis voltage ($V_{\text{tup}} - V_{\text{tdown}}$) , typ 0.5V

For instance, when Cchop is 200pF, the chopping frequency will be as follows:

$$F_{\text{chop}} = 10\mu\text{A} / (200\text{pF} \times 0.5\text{V} \times 2) = 50\text{kHz}$$

The higher the chopping frequency is, the greater the output switching loss becomes. As a result, heat generation issue arises. The lower the chopping frequency is, the lesser the heat generation becomes. However, current ripple occurs. Since noise increases when switching of chopping takes place, you need to adjust frequency with the influence to the other devices into consideration. The frequency range should be between 40kHz and 125kHz.

(11)Blanking period

If you attempt to control PWM constant current chopping of the motor current, when the mode shifts from DECAY to CHARGE, noise is generated in sense resistor pin due to the recovery current of parasitic diode flowing into current sense resistor, and this may cause error detection. The blanking time avoids noise at mode switch. During the blanking time, even if noise is generated in sense resistor, a mode does not switch from CHARGE to DECAY.

In this IC, the blanking time is fixed to approximately 1 μ s.

LV8702V Application Note

(12) Output current vector locus (one step of full step is normalized at 90 degrees)

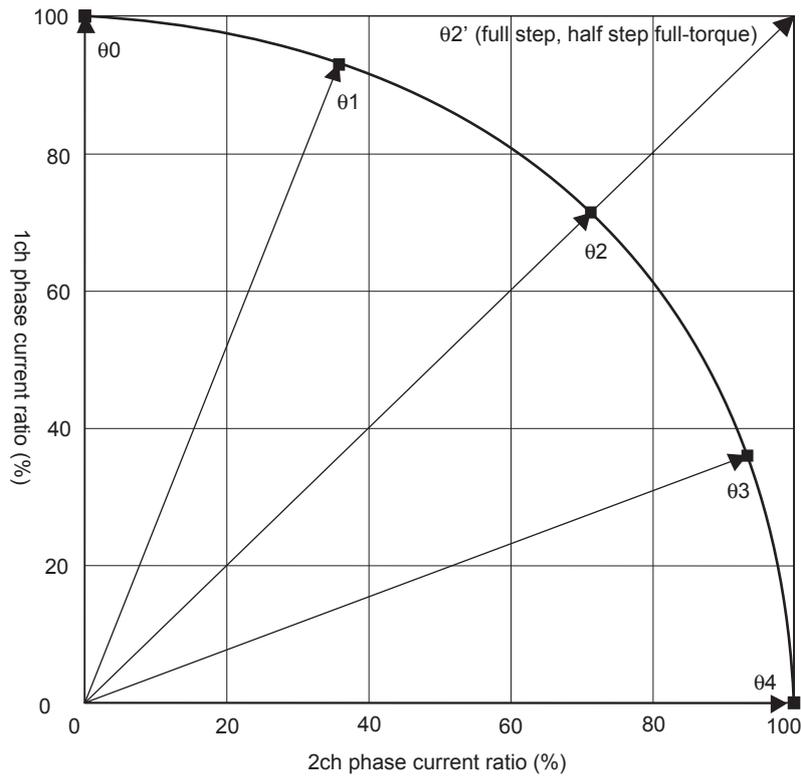


Figure 19. Current vector position

Setting current ration in each excitation mode

STEP	quarter step (%)		half step (%)		half step full-torque (%)		full step (%)	
	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
θ0	100	0	100	0	100	0		
θ1	92	38						
θ2	70	70	70	70	100	100	100	100
θ3	38	92						
θ4	0	100	0	100	0	100		

LV8702V Application Note

(13) Micro-step mode switching operation

When micro-step mode is switched while the motor is rotating, each drive mode operates with the following sequence.

Clockwise mode

Before the micro-step mode changes		Position after the micro-step mode is changed			
Micro-step mode	Position	1/4 step	Half step	Half step full-torque	Full step
1/4 step	00	/	02	02'	02'
	01		02	02'	02'
	02		04	04	02'
	03		04	04	02'
	04		-02	06'	-02'
Half step	00	01	/	02'	02'
	02	03		04	02'
	04	-03		-02'	-02'
Half step full-torque	00	01	02	/	02'
	02'	03	04		02'
	04	-03	-02		-02'
Full step	02'	03	04	04	/

*As for 00 to 04, please refer to the step position of setting current ratio.

If you switch excitation mode while the motor is driving, the mode setting will be reflected from the next STEP and the motor advances to the closest excitation position at switching operation.

(14) The example of current waveform in each excitation mode

Full step (CW mode)

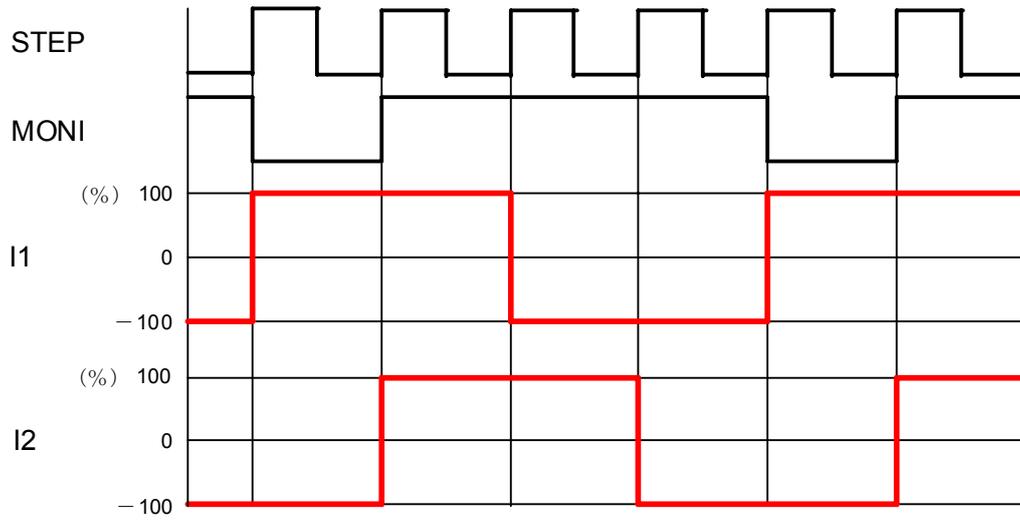


Figure 20. Current waveform of Full step in CLK-IN

Half step full-torque (CW mode)

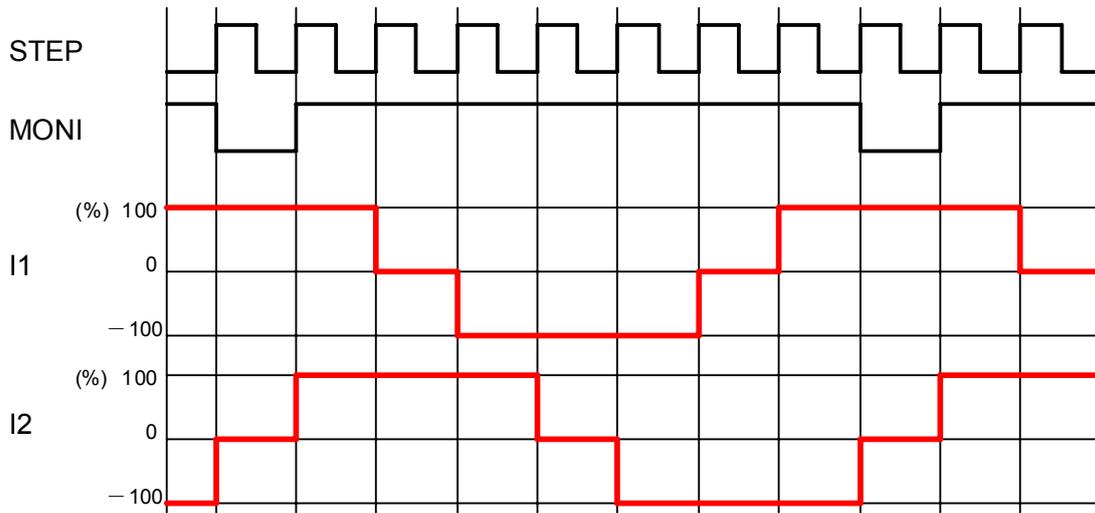


Figure 21. Current waveform of Half step full-torque in CLK-IN

Half step (CW mode)

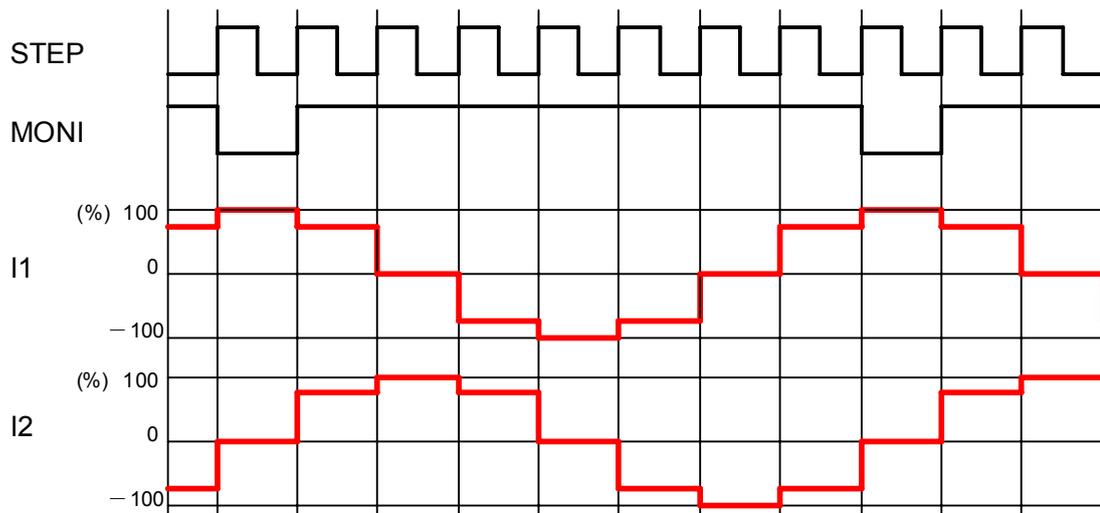


Figure 22. Current waveform of Half step in CLK-IN

Quarter step (CW mode)

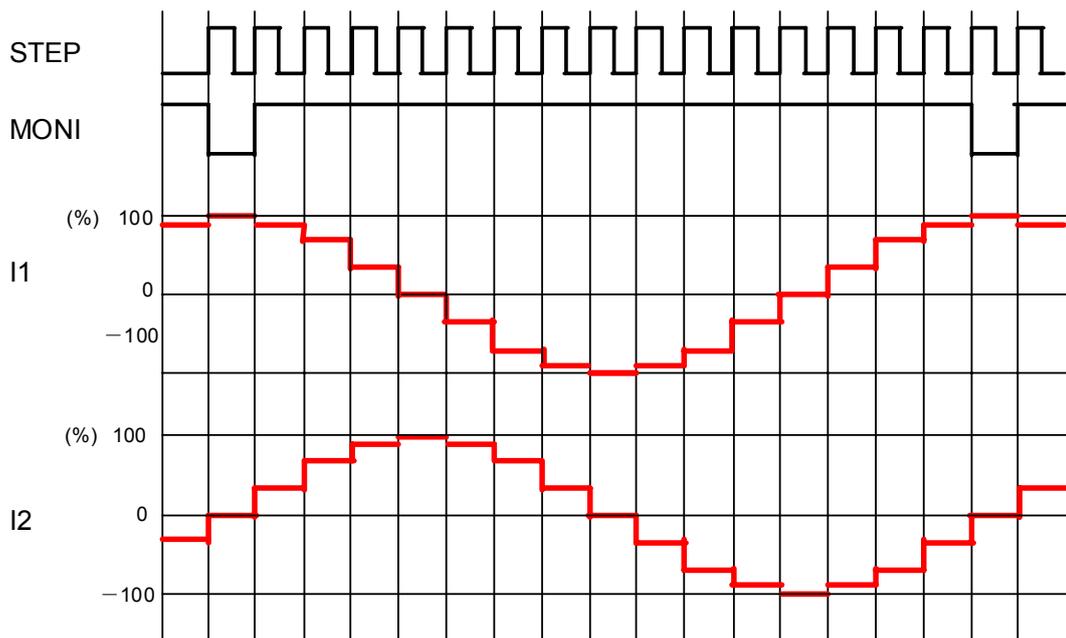
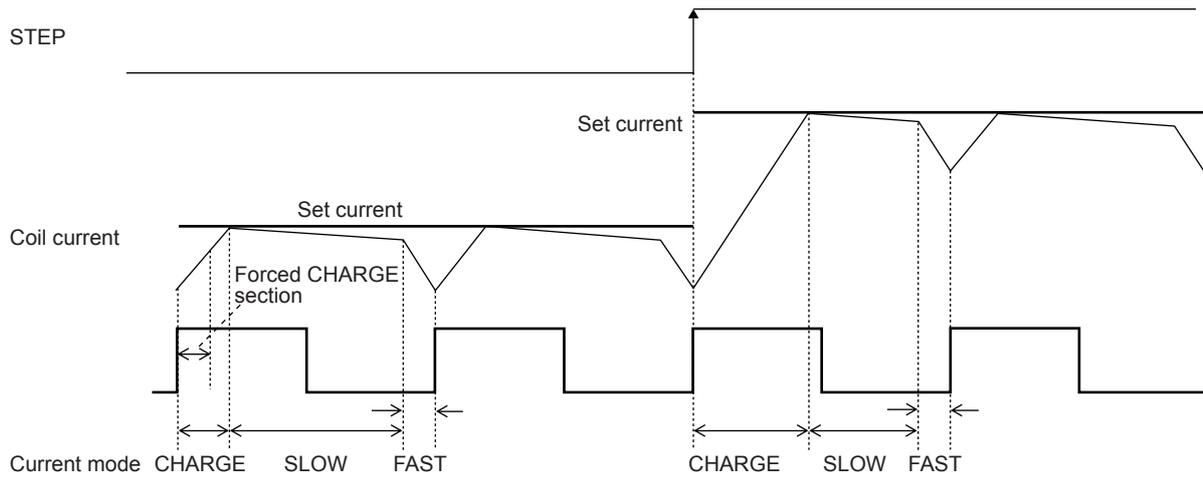


Figure 23. Current waveform of Quarter step in CLK-IN

LV8702V Application Note

(15) Current control operation specification (Sine wave increasing direction)



(Sine wave decreasing direction)

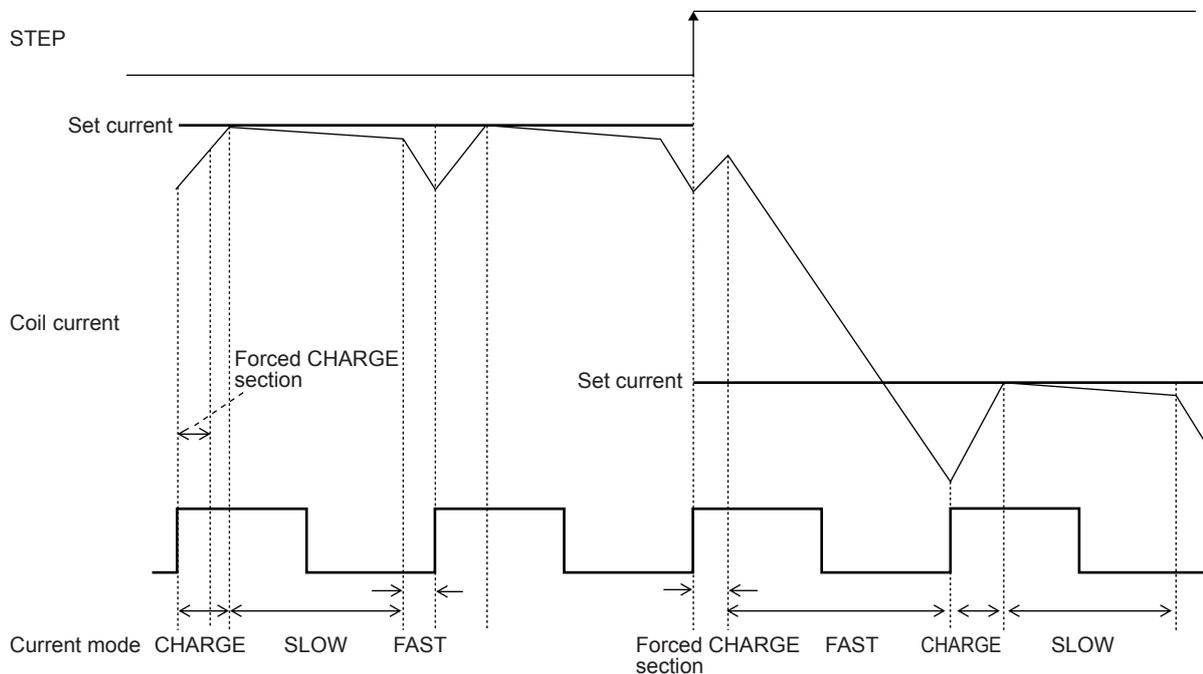


Figure 24. Current control operation

In each current mode, the operation sequence is as described below:

- At rise of chopping frequency, the CHARGE mode begins. (In the time defined as the “blanking time,” the CHARGE mode is forced regardless of the magnitude of the coil current (ICOIL) and set current (IREF) .)
- The coil current (ICOIL) and set current (IREF) are compared in this blanking time.

When $(ICOIL < IREF)$ state exists:

The CHARGE mode up to $ICOIL \geq IREF$, then followed by changeover to the SLOW DECAY mode, and finally by the FAST DECAY mode for approximately $1\mu s$.

When $(ICOIL < IREF)$ state does not exist:

The FAST DECAY mode begins. The coil current is attenuated in the FAST DECAY mode till one cycle of chopping is over.

Above operations are repeated. Normally, the SLOW (+FAST) DECAY mode continues in the sine wave increasing direction, then entering the FAST DECAY mode till the current is attenuated to the set level and followed by the SLOW DECAY mode.

LV8702V Application Note

(16) High-efficient drive function

This IC includes high-efficient drive function. When high-efficient drive function is turned on, I_{OUT} is adjusted automatically within the current value set with VREF pin. When high-efficient drive function is turned off, the current value of I_{OUT} becomes the maximum value set by VREF pin.

It is recommended to evaluate the actual set with the load, because a high efficient is not stable when there is not a load.

1) High-efficient drive enable function

High-efficient drive function is switched on and off with GAD pin.

However, in the case of full step excitation mode (MD1 = MD2 = "L"), even when GAD = "H", high-efficient drive function is turned off.

Even if you adjust the GMG1, GMG2 of 15-2) and GST1, GST2 of 15-3), in the case of abrupt motor acceleration or load variation to the extent that auto adjuster cannot follow up and eventually leads to the rotation stepping-out, it is recommended that you turn off the high-efficient drive function temporarily. As high-efficient control may become unstable due to the control signal from the motor is unstable during low speed rotation, it is also recommended to turn off this function as well.

GAD	Operation mode
Low or OPEN	Normal mode
High	High-efficient mode (except for full step excitation mode)

Recommended speed of high-efficient drive

excitation	Operating conditions	Speed
half step	HB motor/no-load	over 1500pps
half step full-torque	PM motor/no-load	over 1000pps
quarter step	HB motor/no-load	over 3000pps
	PM motor/no-load	over 2500pps

When there is a load, the high-efficient drive is enabled at slower speed.

2) High-efficient drive margin adjuster function

By setting GMG1 and GMG2 pin, margin for step-out is adjusted.

Where GMG1 = GMG2 = "L", I_{OUT} and consumption current are at the lowest. In some case, as the I_{OUT} becomes lower, the number of boost-up process* may increase triggered by slight change of load. With insufficient driving capability, you need to increase the margin setting. One way to set GMG1 and GMG2 is to minimize boost-up level, then lower the margin from high to low to optimize the margin where motor rotates stably.

In the application where load variation is excessive, you need to have a larger margin.

GMG1	GMG2	Setting	Current consumption	Load following capability
Low or OPEN	Low or OPEN	Margin: small	Smallest	Ordinary
High	Low or OPEN	Margin: middle	Smaller	Good
Low or OPEN	High	Margin: large	Small	Better
High	High	Setting is inhibited	-	-

*: This is a function to increase I_{OUT} rapidly as soon as a possible stepping out is detected due to load variation during high efficiency drive.

LV8702V Application Note

3) Boost-up adjuster function

During high-efficient drive, boost-up adjuster function detects a possibility of step-out caused by such factors as abrupt load variation and then boosts up I_{OUT} at once (Boost-up process). You can set a level of boost-up by setting GST1 and GST2 pins. One way to set GST1 and GST2 is to increase boost-up level from minimum to maximum within the maximum load condition and select the optimum boost-up setting where motor rotates without stepping out. Also, boost-up level varies depends on reference current defined by VREF. Therefore, you can increase load following capability by increasing VREF voltage.

The higher the boost-up level is, the more the IC becomes tolerant for abrupt load variation. However, rotation stability may become poor (vibration and rotation fluctuation may occur) because excessively high boost-up level leads to rapid increase of I_{OUT} at load variation. You may be able to improve poor rotation stability with high boost-up level by increasing high-efficient drive margin.

GST1	GST2	Setting	Increase of I_{OUT}	load following capability	Rotation stability
Low or OPEN	Low or OPEN	Boost-up level minimum	$\{(VREF/5)/RF \text{ resistance}\} \times 1/128$	Ordinary	Best
High	Low or OPEN	Boost-up level low	$\{(VREF/5)/RF \text{ resistance}\} \times 4/128$	Good	Better
Low or OPEN	High	Boost-up level high	$\{(VREF/5)/RF \text{ resistance}\} \times 16/128$	Better	Good
High	High	Boost-up level maximum	$\{(VREF/5)/RF \text{ resistance}\} \times 64/128$	Best	Ordinary

4) External component

The resistance value of Ra1, Ra2 (control signal resistors) is adjusted in such a way as to set the maximum SWOUT output voltage during motor rotation to 12V in ADIN pin. Preferably, resistance values of Ra1 and Ra2 are as high as possible to the extent that does not influence waveform. (Recommendation for Ra1: 15k Ω , Ra2: 100k Ω).

In some motor where boost-up process occurs at a high speed rotation of 7000pps to 8000pps or higher (HB motor: Half step excitation), you can suppress boost-up by lowering Ra1. Moreover, you can achieve high efficiency at lower speed of 1500pps or lower by increasing resistance for Ra1 (HB motor: Half step excitation).

Although it depends on a usage motor, step-out is detectable at higher speed rotation by attaching smaller resistor for Ra1.

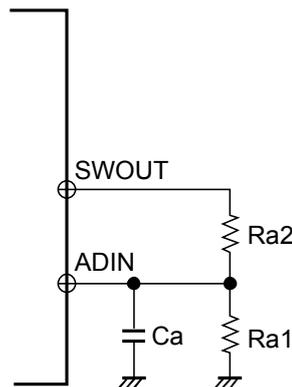


Figure25. ADIN filter circuit

LV8702V Application Note

(17) Output transistor operation mode

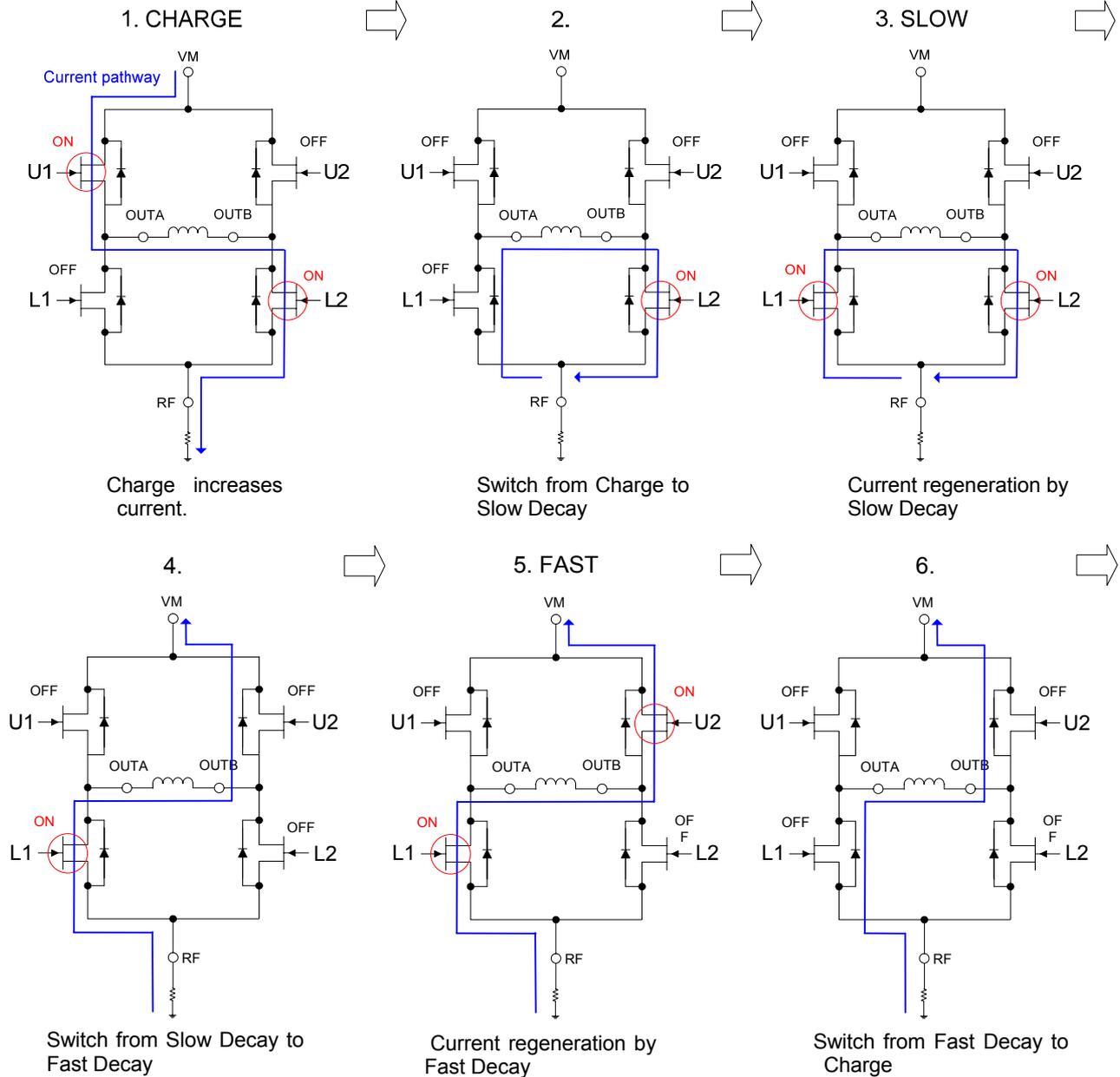


Figure 26. Switching operation

This IC controls constant current by performing chopping to output transistor.

As shown above, by repeating the process from 1 to 6, setting current is maintained.

Chopping consists of 3 modes: Charge/ Slow decay/ Fast decay. In this IC, for switching mode (No.2, 4, 6), there are “off period” in upper and lower transistor to prevent crossover current between the transistors. This off period is set to be constant ($\approx 0.375\mu\text{s}$) which is controlled by the internal logic. The diagrams show parasitic diode generated due to structure of MOS transistor. When the transistor is off, output current is regenerated through this parasitic diode.

Output Transistor Operation Function

OUTA→OUTB (CHARGE)

Output Tr	CHARGE	SLOW	FAST
U1	ON	OFF	OFF
U2	OFF	OFF	ON
L1	OFF	ON	ON
L2	ON	ON	OFF

OUTB→OUTA (CHARGE)

Output Tr	CHARGE	SLOW	FAST
U1	OFF	OFF	ON
U2	ON	OFF	OFF
L1	ON	ON	OFF
L2	OFF	ON	ON

LV8702V Application Note

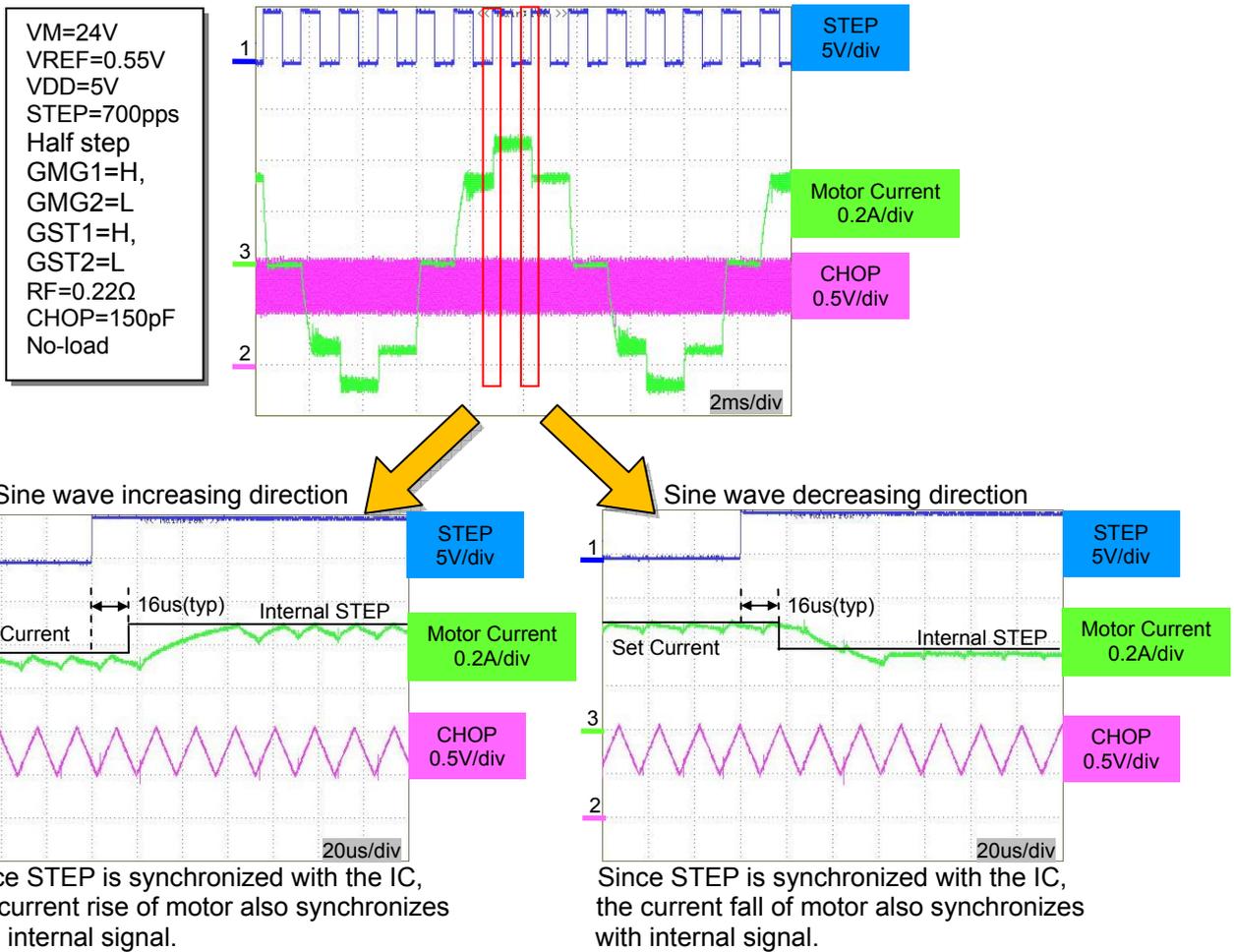


Figure 27. Current control operation waveform

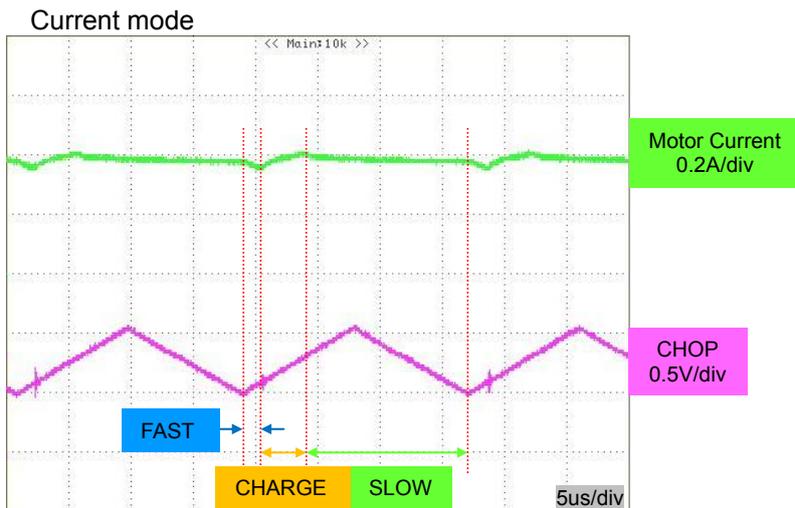


Figure 28. Chopping waveform

Motor current switches to Fast Decay mode when triangle wave (CHOP) switches from Discharge to Charge. Approximately after 1μs, the motor current switches to Charge mode. When the current reaches to the setting current, it is switched to Slow Decay mode which continues over the Discharge period of triangle wave.

LV8702V Application Note

High-efficient mode

When this driver shows GAD="H", it is in high efficient mode where drive current is adjusted automatically according to motor rotational speed and the change of load. By lowering the current, power consumption, heat generation, vibration and noise are reducible.

(1) The reduction of motor current

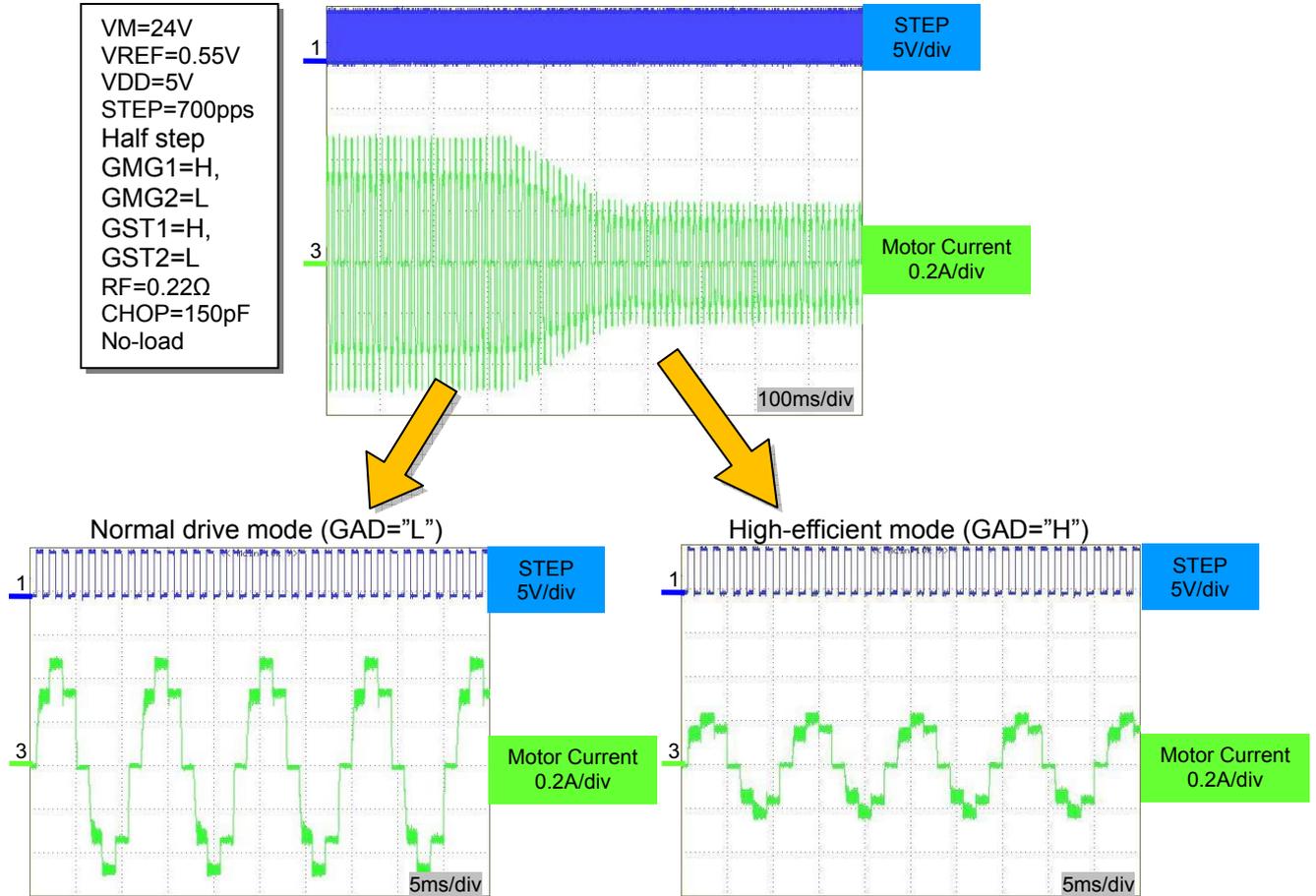


Figure 29. Normal drive mode -> High efficient mode Motor current waveform

Motor current is adjusted according to rotational speed and load by setting high efficiency mode (GAD="H"). The smaller the load is, the better the driving efficiency becomes.

LV8702V Application Note

(2) Motor current by different setting current.

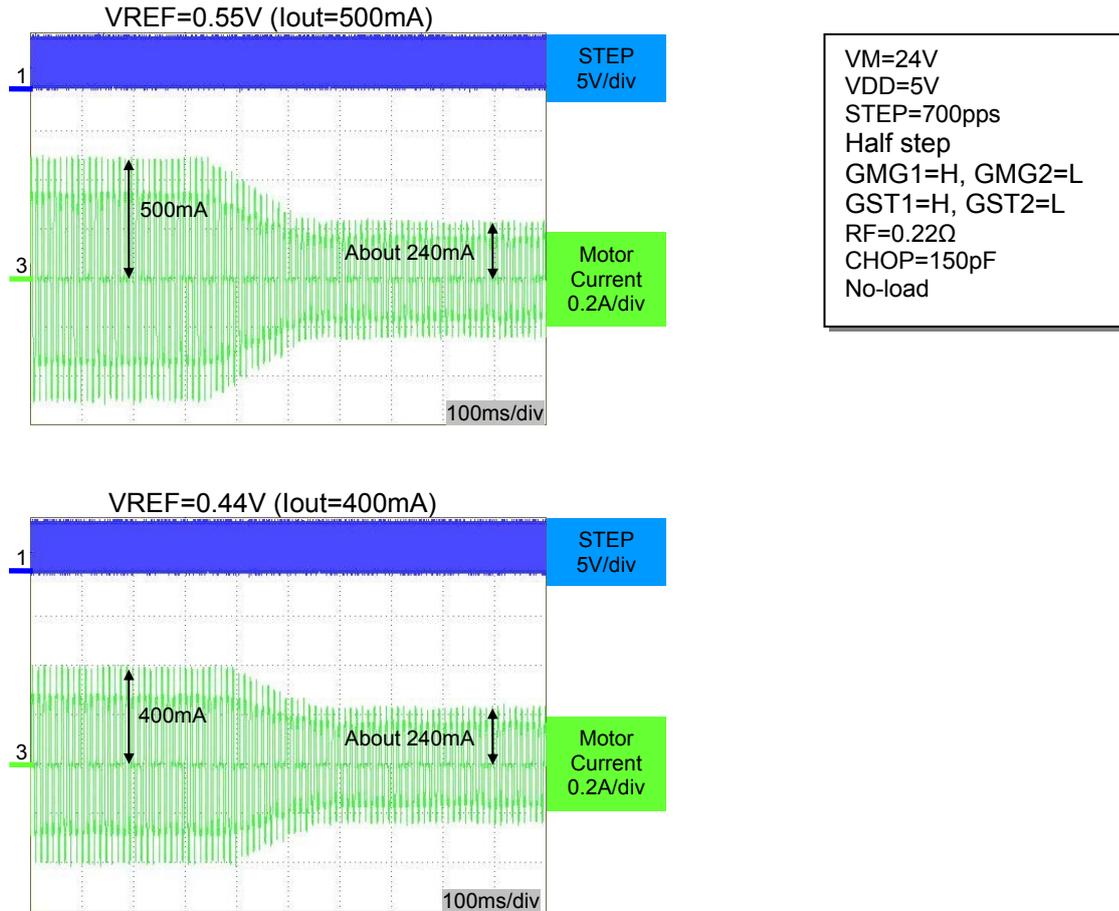


Figure 30. Motor current waveform by setting current

Whichever setting current is selected (Iout=500mA/ 400mA), after current adjustment the motor current will be the same according to rotational speed and load.

Taking the possibility of additional load into consideration, current should be set higher and reduce current consumption at light load by high efficiency mode.

LV8702V Application Note

(3) Difference in motor current by margin setting for high efficiency drive (GMG1,GMG2)

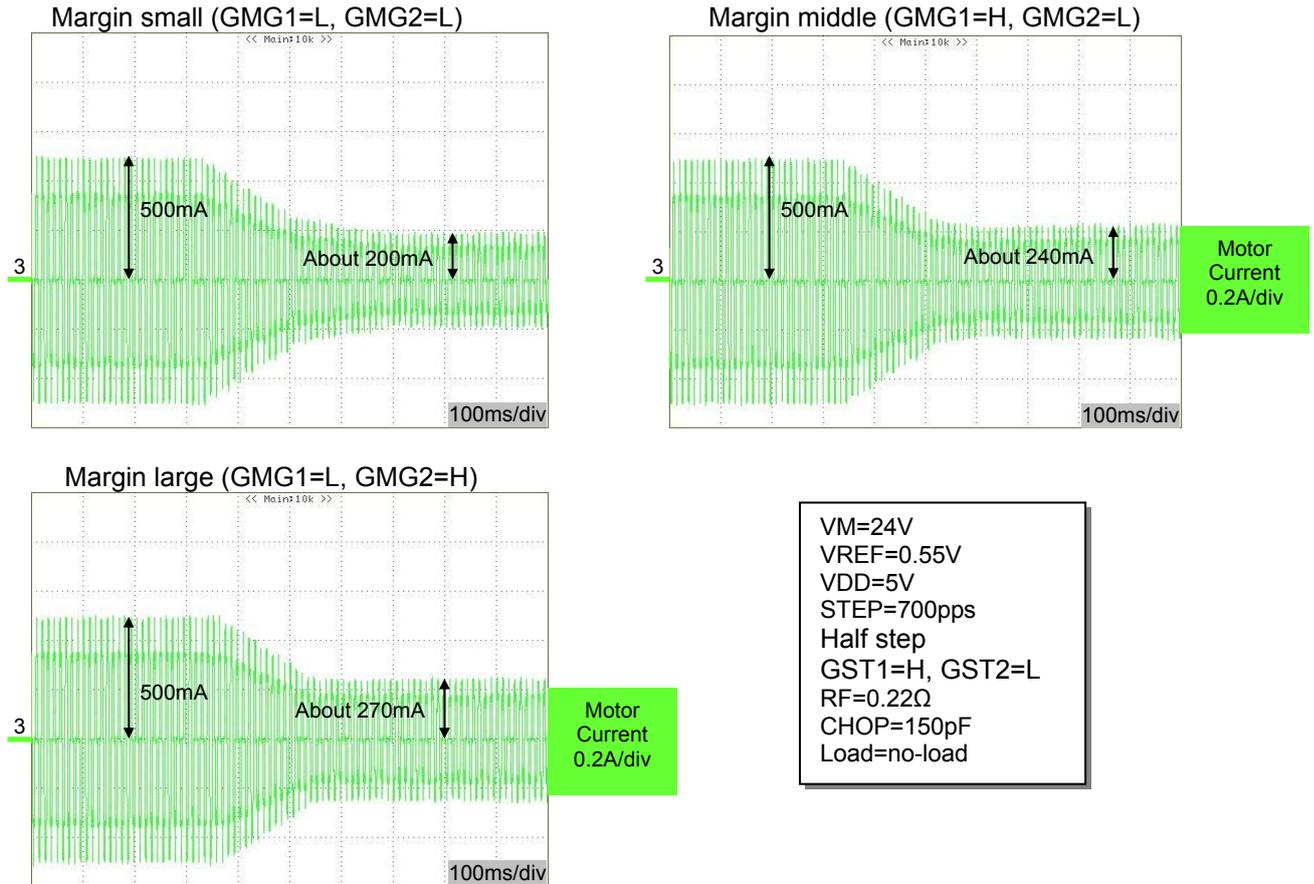


Figure 31. Motor current waveform by high efficiency margin setting

Motor driving capability at high efficiency mode is configurable by changing margin setting.

Margin setting enables to adjust the margin of rotor phase against a target phase. Therefore, driving current after the adjustment varies depends on motor type and load. Make sure to check the motor current at high efficiency mode using the actual application.

Driving capability is the lowest at "Margin small" (GMG1=L, GMG2=L) and the highest at "Margin large" (GMG1=L, GMG2=H).

When the driving capability is lower against the usage load, in some case, the number of boost-up process* may increase. In this case, increase the margin setting to adjust the driving capability.

In the application where load variation is excessive, you need to have a larger margin.

*: This is a function to increase I_{OUT} rapidly as soon as a possible stepping out is detected due to load variation during high efficiency drive.

LV8702V Application Note

(4) Difference in motor current by boost-up setting (GST1,GST2)

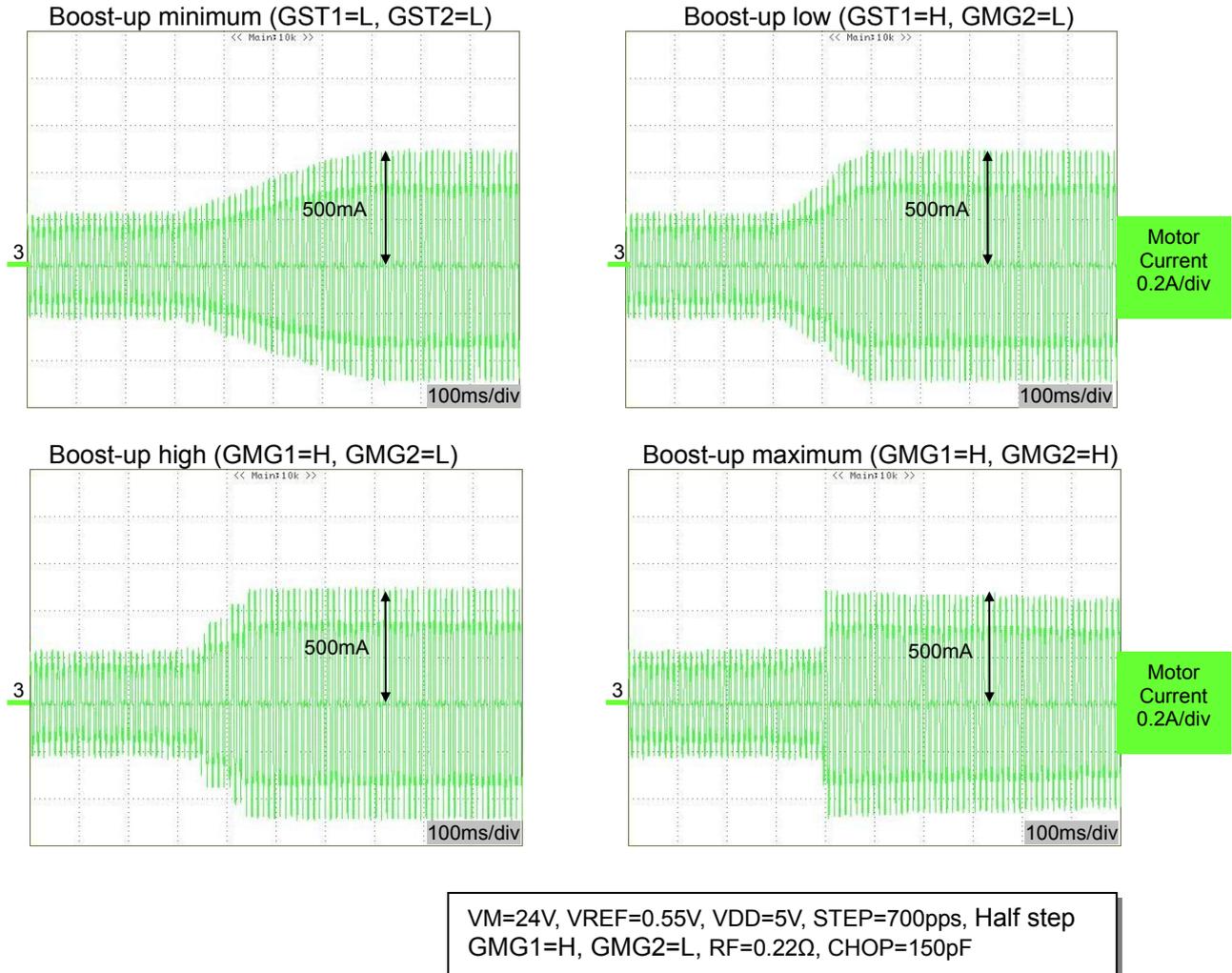


Figure 32. Motor current waveform by boost-up setting

When the rotor phase of motor delays due to the variation of load and the IC determined that more driving current is needed, boost-up process is operated to increase lout rapidly. See (16) – 3) Boost-up adjuster function for the level of lout increase by boost-up process. The motor current waveform by boost-up setting is as shown above.

The higher the boost-up level is, the more the IC becomes tolerant for abrupt load variation. However, caution is required for loosing stability in rotation by increasing lout rapidly.

LV8702V Application Note

(5) Step-out detection function

Step-out state is detectable only in high efficient mode. When step-out is detected, DTS1 pin is turned "L" for 1 STEP period. In some case step-out cannot be detected depends on motor type and rotational speed. Hence, make sure to check the operation using the actual usage application.

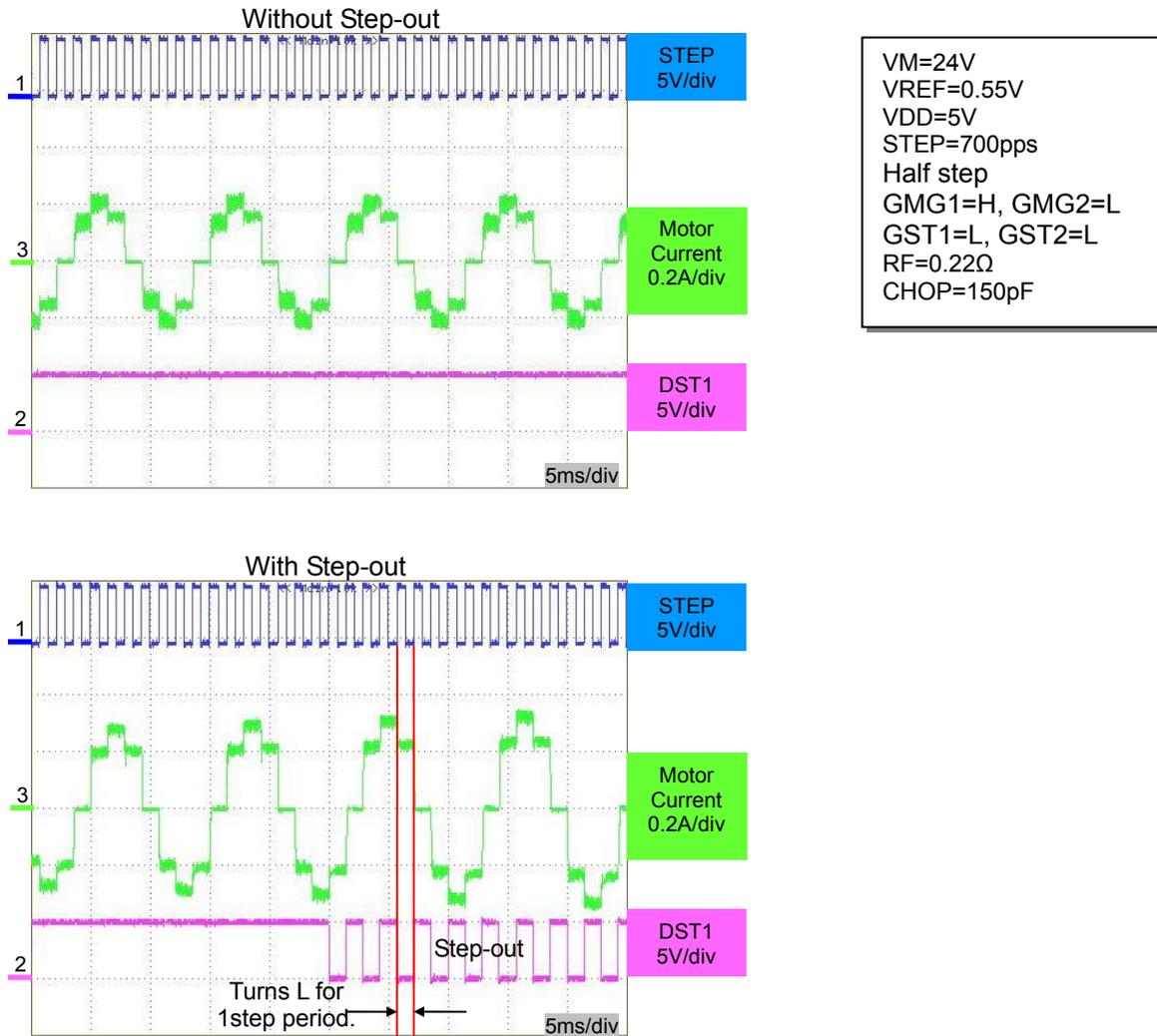


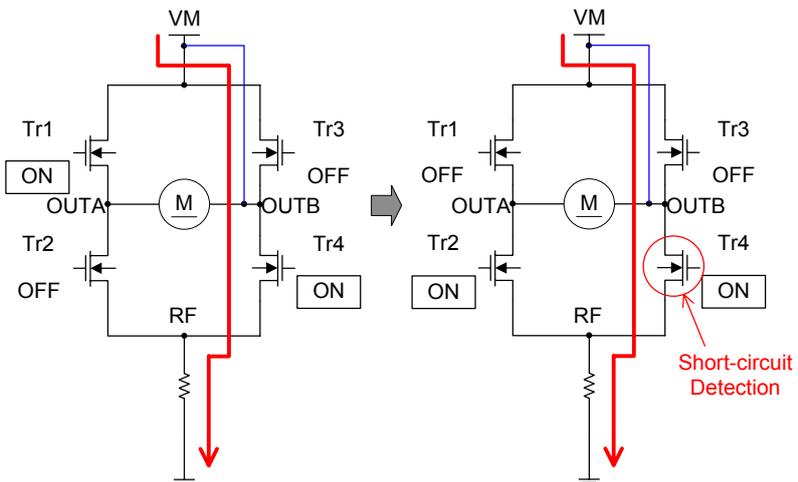
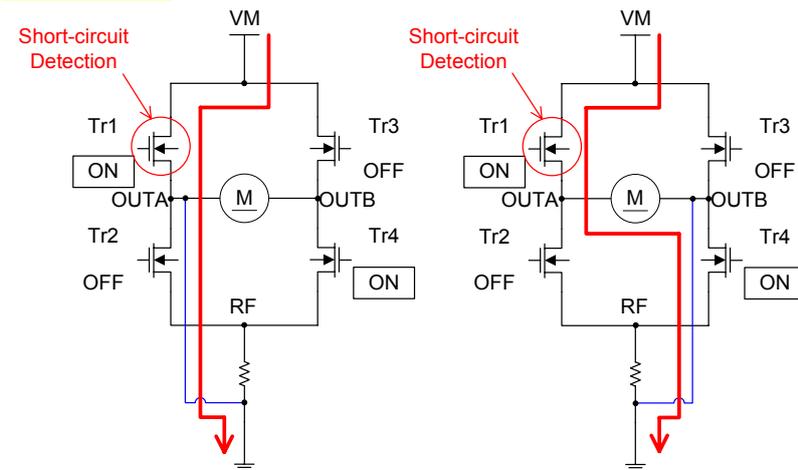
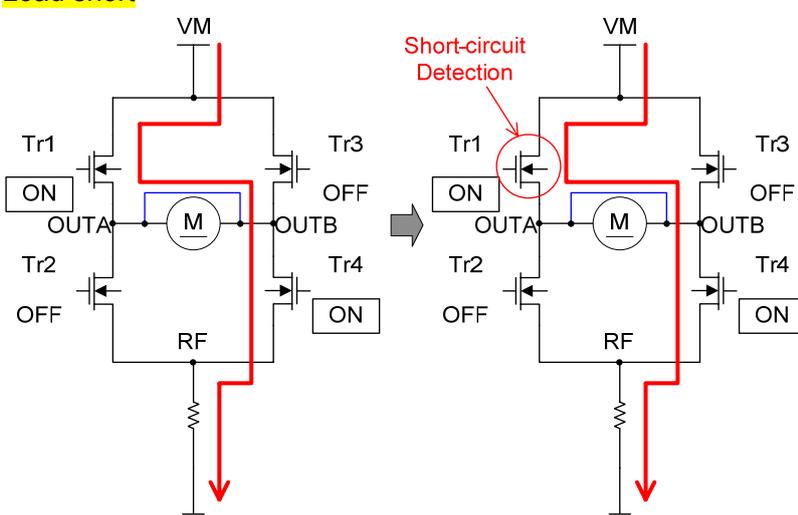
Figure 33. Step-out detection waveform

LV8702V Application Note

Output short-circuit protection function

This IC incorporates an output short-circuit protection circuit that, when the output has been shorted by an event such as shorting to power or shorting to ground, sets the output to the standby mode and turns on the warning output in order to prevent the IC from being damaged. In the stepper motor driver (STM) mode (DM = Low), this function sets the output to the standby mode for both channels by detecting the short-circuiting in one of the channels. In the DC motor driver mode (DM = High), channels 1 and 2 operate independently. (Even if the output of channel 1 has been short-circuited, channel 2 will operate normally.)

(1) Output short-circuit detection operation

<p>Short to Power</p> 	<ol style="list-style-type: none"> 1. High current flows if OUTB short to VM and Tr4 are ON. 2. If RF voltage > setting voltage, then the mode switches to SLOW decay. 3. If the voltage between Drain and Source of Tr4 exceeds the reference voltage for 2μs, short status is detected.
<p>Short to GND</p> 	<p>(left schematic)</p> <ol style="list-style-type: none"> 1. High current flows if OUTA short to GND and Tr1 are ON 2. If the voltage between Drain and Source of Tr1 exceeds the reference voltage for 2μs, short status is detected. <p>(right schematic)</p> <ol style="list-style-type: none"> 1. Without going through RF resistor, current control does not operate and current will continue to increase in CHARGE mode. 2. If the voltage between Drain and Source of Tr1 exceeds the reference voltage for 2μs, short status is detected.
<p>Load short</p> 	<ol style="list-style-type: none"> 1. Without L load, high current flows. 2. If RF voltage > setting voltage, then the mode switches to SLOW decay. 3. During load short stay in SLOW decay mode, current does not flow and over current state is not detected. Then the mode is switched to FAST decay according to chopping cycle. 4. Since FAST state is short (≈1μs), switches to CHARGE mode before short is detected. 5. If voltage between Drain and Source exceeds the reference voltage continuously during blanking time at the start of CHARGE mode (Tr1), CHARGE state is fixed (even if RF voltage exceeds the setting voltage, the mode is not switched to SLOW decay). After 2us or so, short is detected.

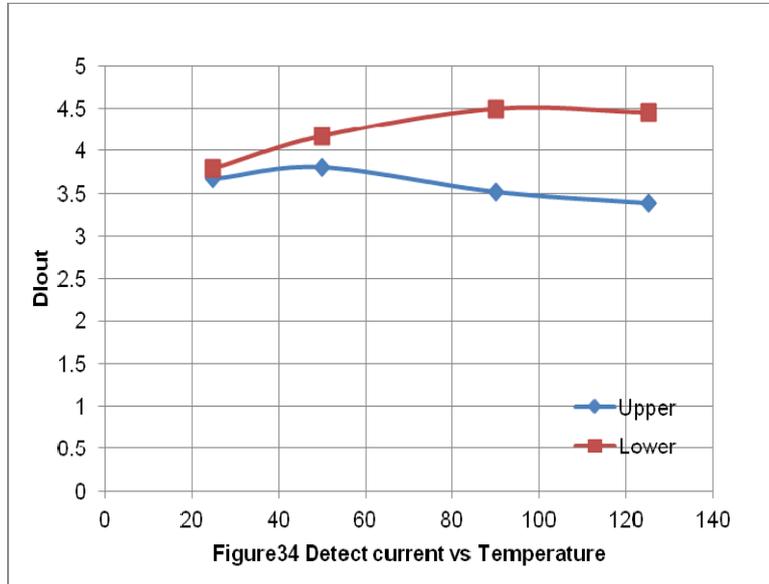
LV8702V Application Note

- (2) Output short-circuit protection detect current (Reference value)
Short protector operates when abnormal current flows into the output transistor.

Ta = 25°C (typ)

Output Transistor	LV8702V
Upper-side Transistor	3.7A
Lower-side Transistor	3.8A

*RF=GND



LV8702V Application Note

Charge Pump Circuit

When the ST pin is set High, the charge pump circuit operates and the VG pin voltage is boosted from the VM voltage to the VM + VREG5 voltage. If the VG pin voltage is not boosted to VM+4V or more, the output pin cannot be turned on. Therefore it is recommended that the drive of motor is started after the time has passed tONG or more.

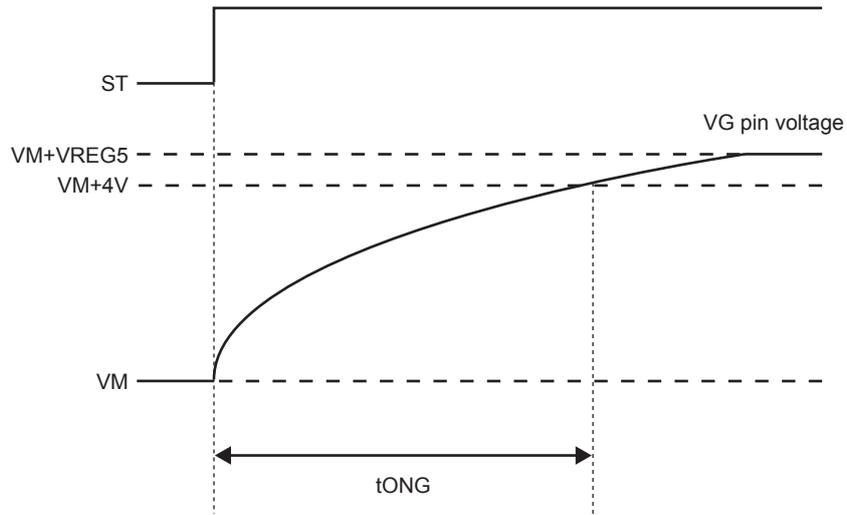


Figure 35. VG pin voltage schematic view

VG voltage is used to drive upper output FET and VREG5 voltage is used to drive lower output FET. Since VG voltage is equivalent to the addition of VM and VREG5 voltage, VG capacitor should allow higher voltage. The capacitor between CP1 and CP2 is used to boost charge pump. Since CP1 oscillates with 0V↔VREG5 and CP2 with VM↔VM+VREG5, make sure to allow enough capacitance between CP1 and CP2. Since the capacitance is variable depends on motor types and driving methods, please check with your application before you define constant to avoid ripple on VG voltage.

(Recommended value) VG: 0.1μF
CP1-CP2: 0.1μF

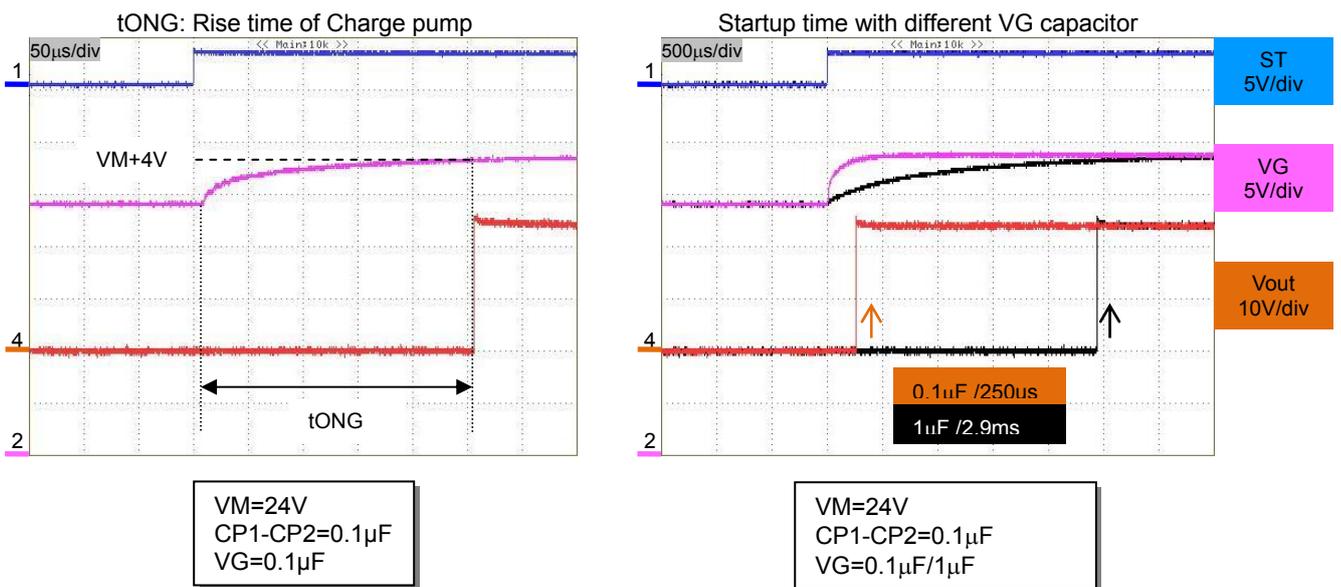


Figure 36. VG voltage pressure waveform

LV8702V Application Note

Thermal shutdown function

The thermal shutdown circuit is included, and the output is turned off when junction temperature T_j exceeds 180°C and the abnormal state warning output is turned on at the same time.

When the temperature falls hysteresis level, output is driven again (automatic restoration)

The thermal shutdown circuit doesn't guarantee protection of the set and the destruction prevention of IC, because it works at the temperature that is higher than rating ($T_{j\text{max}}=150^{\circ}\text{C}$) of the junction temperature

$T_{SD}=180^{\circ}\text{C}(\text{typ})$

$\Delta T_{SD}=40^{\circ}\text{C}(\text{typ})$

LV8702V Application Note

Application Circuit Example

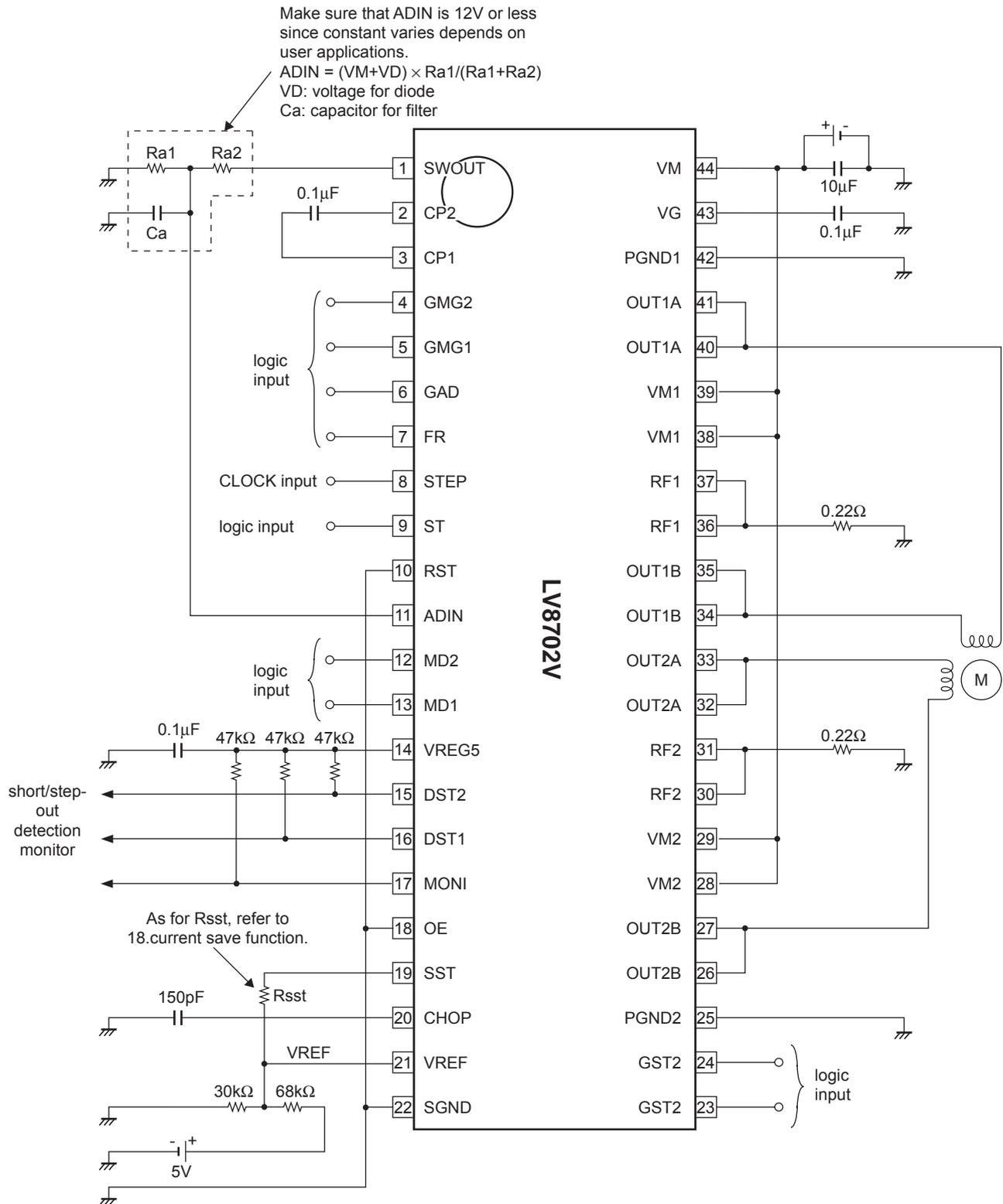


Figure 37. Application Circuit diagram

Calculation for each constant setting according to the above circuit diagram is as follows.

1) Constant current (100%) setting

$$VREF = 5V \times 30k\Omega / (68k\Omega + 30k\Omega) \approx 1.53V$$

When $VREF = 1.53V$:

$$I_{OUT} = VREF / 5 / 0.22\Omega \approx 1.39A$$

2) Chopping frequency setting

$$F_{chop} = I_{chop} / (C_{chop} \times V_{tchop} \times 2)$$

$$= 10\mu A / (150pF \times 0.5V \times 2)$$

$$\approx 66.7kHz$$

LV8702V Application Note

Allowable power dissipation

The pad on the backside of the IC functions as heatsink by soldering with the board. Since the heat-sink characteristics vary depends on board type, wiring and soldering, please perform evaluation with your board for confirmation.

Specified circuit board: 90mm x 90mm x 1.6mm, glass epoxy 4-layer board

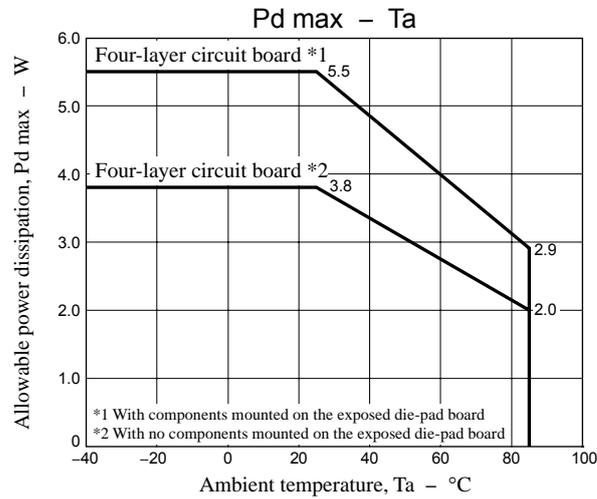
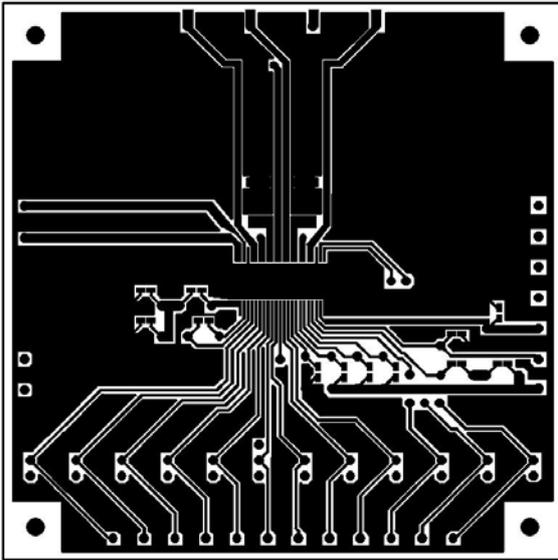


Figure 38. Pdmax – Ta Characteristic

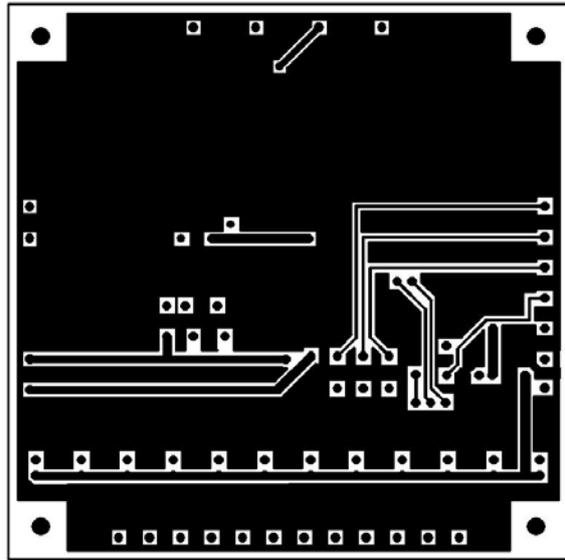
LV8702V Application Note

Substrate Specifications (Substrate recommended for operation of LV8702V)

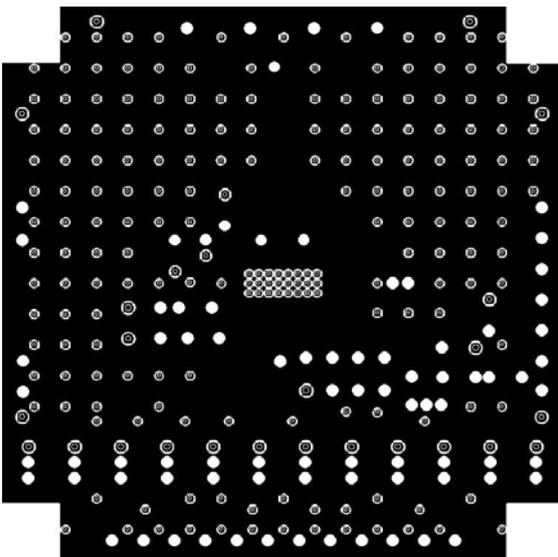
Size	: 90mm × 90mm × 1.6mm (Four-layer substrate)
Material	: Glass epoxy
Copper wiring density	: L1 = 85%, L2 = 90%



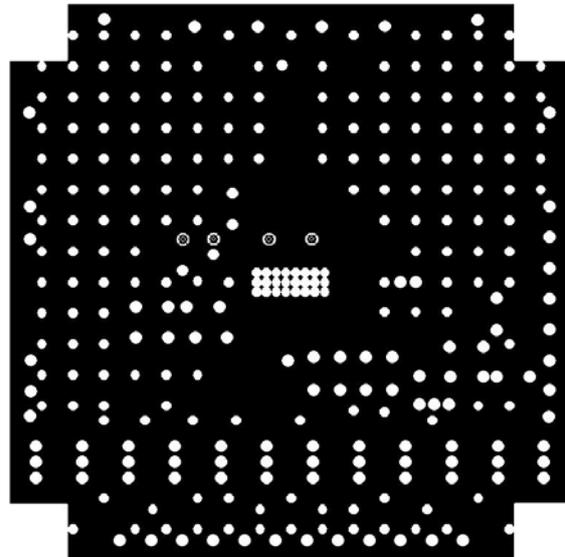
L1: Copper wiring pattern diagram



L2: Copper wiring pattern diagram



L3: GND layer



L4: Power supply layer

Figure 39. Substrate layout diagram

Cautions

- 1) The data for the case with the Exposed Die-Pad substrate mounted shows the values when 90% or more of the Exposed Die-Pad is wet.
- 2) For the set design, employ the derating design with sufficient margin.
Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stress such as vibration, impact, and tension.
Accordingly, the design must ensure these stresses to be as low or small as possible.
The guideline for ordinary derating is shown below:
 - (1) Maximum value 80% or less for the voltage rating
 - (2) Maximum value 80% or less for the current rating
(However this does not apply to high efficiency drive because operating current is lower than the setting current.)
 - (3) Maximum value 80% or less for the temperature rating
- 3) After the set design, be sure to verify the design with the actual product.
Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc.
Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal

LV8702V Application Note

conduction, possibly resulting in thermal destruction of IC.

LV8702V Application Note

Evaluation board

LV8702V (90.0mm×90.0mm×1.6mm, glass epoxy 4-layer board, with backside mounting)

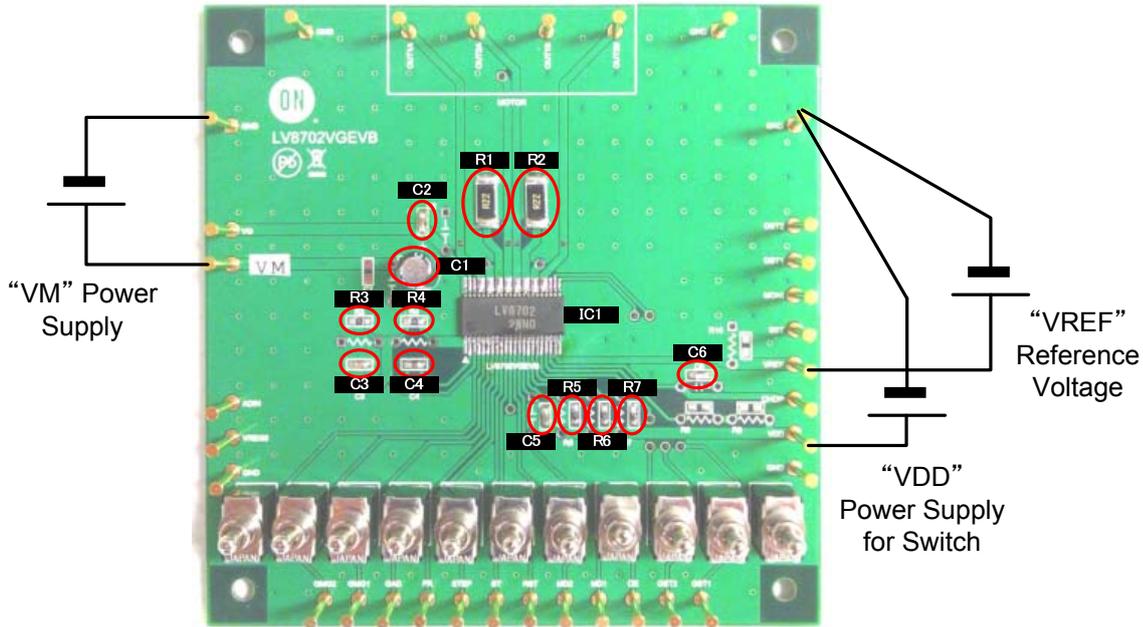


Figure 40. Evaluation board

Bill of Materials for LV8702V Evaluation Board

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free
C1	1	VM Bypass Capacitor	10 μ F, 50V	\pm 20%		SUN Electronic Industries	50ME10HC	Yes	Yes
C2	1	Capacitor for Charge pump	0.1 μ F, 100V	\pm 10%	1608 (0603Inch)	Murata	GRM188R72A 104KA35*	Yes	Yes
C3	1	Capacitor for filter of control signal	1000pF, 50V	\pm 5%	1608 (0603Inch)	Murata	GRM1882C1H 102JA01*	Yes	Yes
C4	1	Capacitor for Charge pump	0.1 μ F, 100V	\pm 10%	1608 (0603Inch)	Murata	GRM188R72A 104KA35*	Yes	Yes
C5	1	VREG5 stabilization Capacitor	0.1 μ F, 100V	\pm 10%	1608 (0603Inch)	Murata	GRM188R72A 104KA35*	Yes	Yes
C6	1	Capacitor to set chopping frequency	150pF, 50V	\pm 5%	1608 (0603Inch)	Murata	GRM1882C1H 151JA01*	Yes	Yes
R1	1	Channel 1 output current detective Resistor	0.22 Ω , 1W	\pm 5%	6432 (2512Inch)	ROHM	MCR100JZHJLR22	Yes	Yes
R2	1	Channel 2 output current detective Resistor	0.22 Ω , 1W	\pm 5%	6432 (2512Inch)	ROHM	MCR100JZHJLR22	Yes	Yes
R3	1	Resistor for filter of control signal	15k Ω , 1/10W	\pm 5%	1608 (0603Inch)	KOA	RK73B1JT**153J	Yes	Yes
R4	1	Resistor for filter of control signal	100k Ω , 1/10W	\pm 5%	1608 (0603Inch)	KOA	RK73B1JT**104J	Yes	Yes
R5	1	Pull-up Resistor for terminal DST2	47k Ω , 1/10W	\pm 5%	1608 (0603Inch)	KOA	RK73B1JT**473J	Yes	Yes
R6	1	Pull-up Resistor for terminal DST1	47k Ω , 1/10W	\pm 5%	1608 (0603Inch)	KOA	RK73B1JT**473J	Yes	Yes
R7	1	Pull-up Resistor for terminal MONI	47k Ω , 1/10W	\pm 5%	1608 (0603Inch)	KOA	RK73B1JT**473J	Yes	Yes
IC1	1	Motor Driver			SSOP44K (275mil)	ON semiconductor	LV8702V	No	Yes
SW1-SW11	11	Switch				MIYAMA	MS-621C-A01	Yes	Yes
TP1-TP29	33	Test Point				MAC8	ST-1-3	Yes	Yes

LV8702V Application Note

Evaluation board circuit

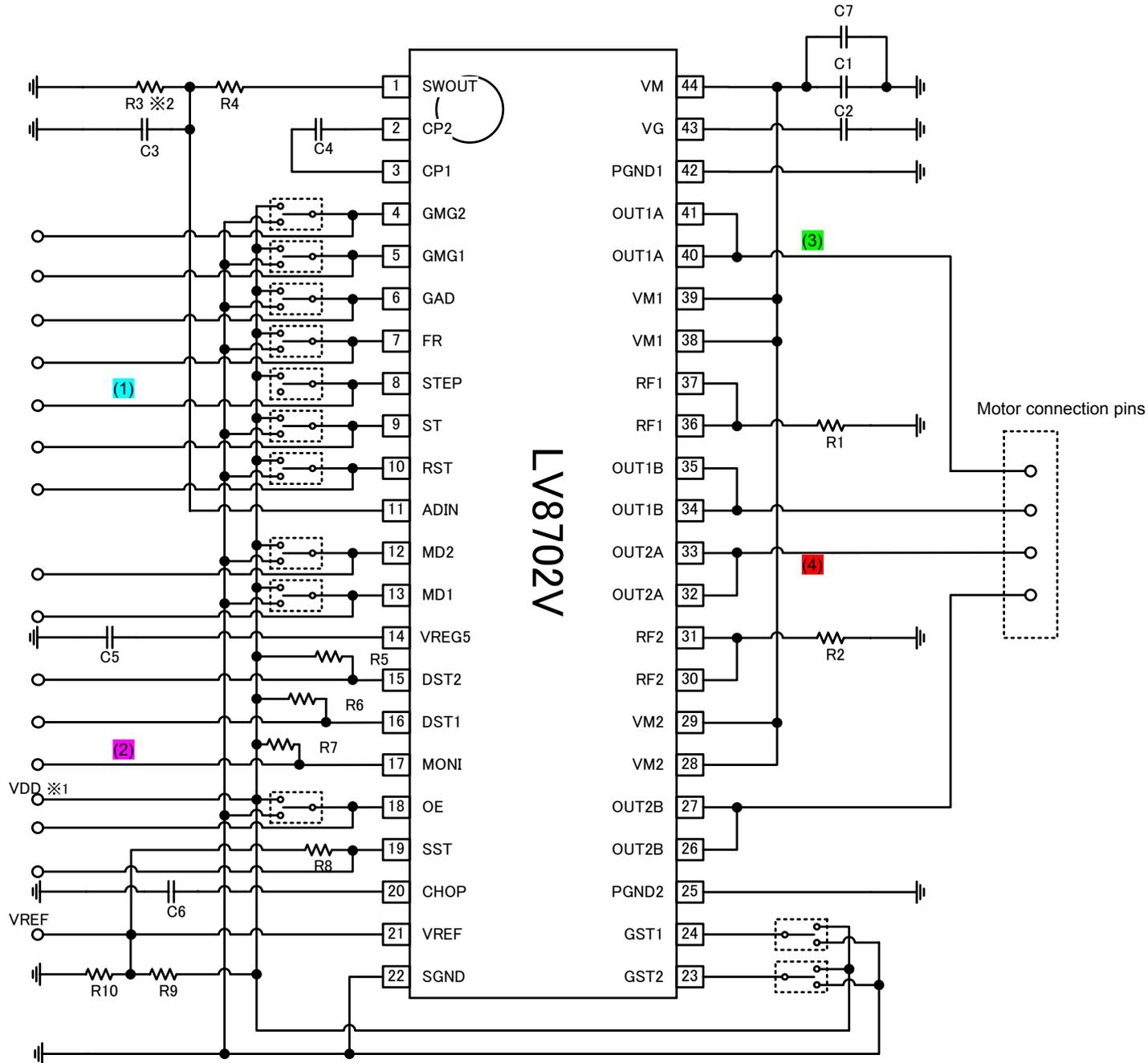


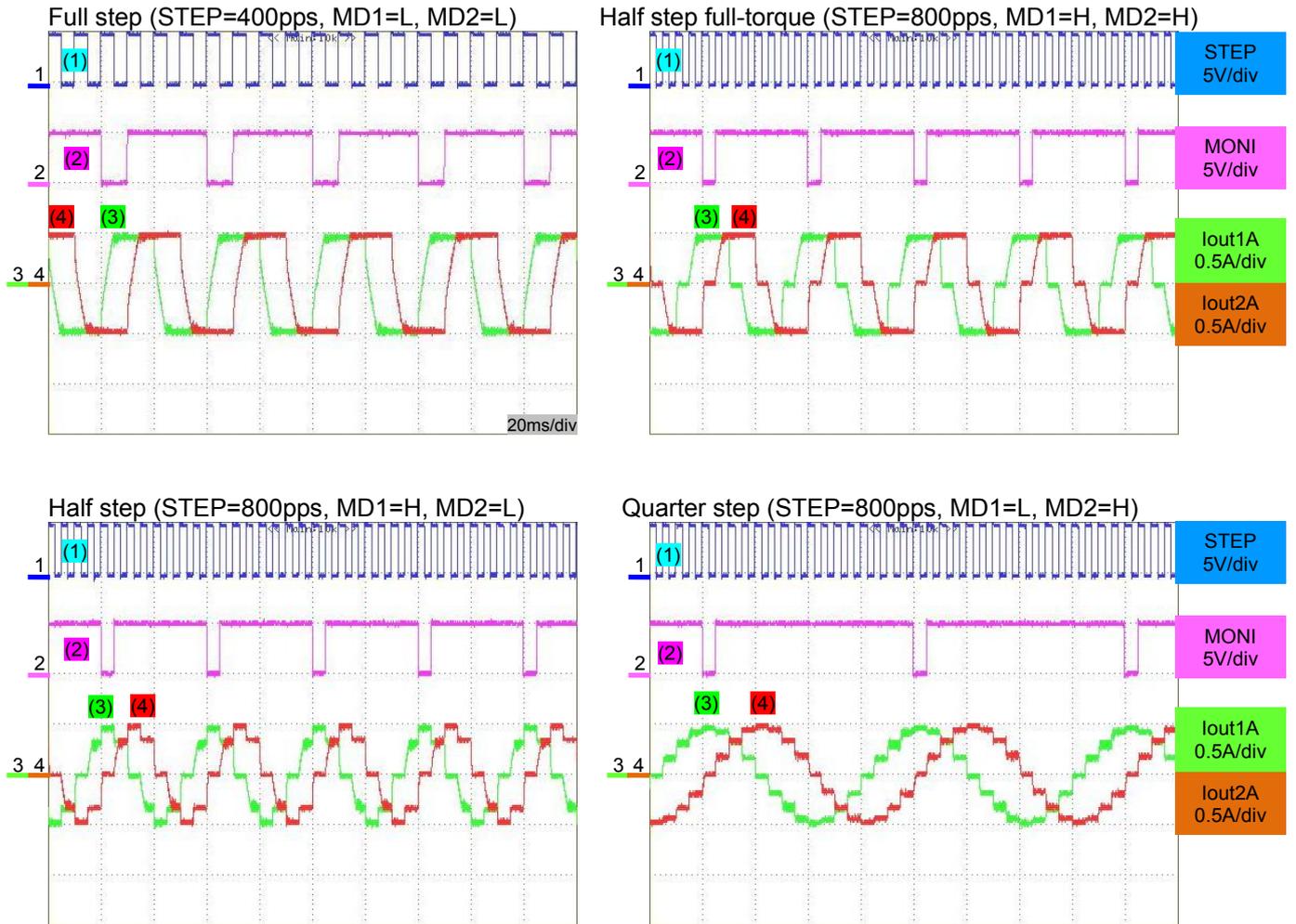
Figure 41. Evaluation board circuit diagram

*1 VDD is a power supply pin for SW/Nch open-drain. By supplying 3.3V or 5V, logic input setting is enabled. VDD is also the pull-up power supply for Nch open-drain.

*2 By increasing R3 resistor, high efficient operation is stabilized at low speed rotation (at 1/2 step: 1000pps or lower)
 Also by decreasing R3 resistor, high efficient operation is stabilized at high speed rotation (at 1/2 step: 10000pps or higher).
 (Frequency for stable operation varies depends on motor and load.)

LV8702V Application Note

Motor drive waveform



VM=24V, VDD=5V, VREF=0.55V
 GAD=L
 GMG1=H, GMG2=L
 GST1=H, GST2=L
 FR=L, RST=L, OE=L
 ST=H
 STEP, MD1 and MD2 are above conditions

Figure 42. Motor current waveform of each micro step

Evaluation Board Manual

[Supply Voltage] VM (9 to 32V) : Power Supply for LSI
 VREF (0 to 3V) : Const. Current Control for Reference Voltage
 VDD (2 to 5V) : Logic "High" voltage for toggle switch

[Toggle Switch State] Upper Side : High (VDD)
 Middle : Open, enable to external logic input
 Lower Side : Low (GND)

[Operation Guide]

1. Motor Connection: Connect the Motors between OUT1A and OUT1B, between OUT2A and OUT2B.
2. Initial Condition Setting: Set "Open" the toggle switch STEP, and "Open or Low" the other switches.
3. Power Supply: Supply DC voltage to VM, VREF and VDD.
4. Ready for Operation from Standby State: Turn "High" the ST terminal toggle switch. Channel 1 and 2 are into Full step initial position (100%, -100%).
5. Motor Operation: Input the clock signal into the terminal STEP.
6. Other Setting
 - i. GAD: High efficient drive enable.
 - ii. GMG1/GMG2 : High efficient drive margin setting.
 - iii. GST1/GST2: Boost-up level setting.
 - iv. FR: Motor rotation direction (CW / CCW) setting.
 - v. RST: Reset function setting.
 - vi. OE: Output enable.
 - vii. MD1, MD2: Excitation mode setting.

[Setting for External Component Value]

1. Constant Current (100%)
 At VREF =0.55V
 $I_{out} = VREF [V] / 5 / RF [\Omega]$
 $= 0.55 [V] / 5 / 0.22 [\Omega]$
 $= 0.5 [A]$
2. Chopping Frequency
 $F_{chop} = I_{chop} [\mu A] / (C_{chop} \times V_t \times 2)$
 $= 10 [\mu A] / (150 [pF] \times 0.5 [V] \times 2)$
 $= 67 [kHz]$

LV8702V Application Note

Notes in design:

●Power supply connection terminal (VM, VM1, VM2)

- ✓ Make sure to short-circuit VM, VM1 and VM2. For controller supply voltage, the internal regulator voltage of VREG5 (typ 5V) is used.
- ✓ Make sure that supply voltage does not exceed the absolute MAX ratings under no circumstance. Noncompliance can be the cause of IC destruction and degradation.
- ✓ Caution is required for supply voltage because this IC performs switching.
- ✓ The bypass capacitor of the power supply should be close to the IC as much as possible to stabilize voltage. Also if you intend to use high current or back EMF is high, please augment enough capacitance.

●GND terminal (GND, PGND, Exposed Die-Pad)

- ✓ Since GND is the reference of the IC internal operation, make sure to connect to stable and the lowest possible potential. Since high current flows into PGND, connect it to one-point GND.
- ✓ The exposed die-pad is connected to the board frame of the IC. Therefore, do not connect it other than GND. Independent layout is preferable. If such layout is not feasible, please connect it to signal GND. Or if the area of GND and PGND is larger, you may connect the exposed die pad to the GND.
(The independent connection of exposed die pad to PGND is not recommended.)

●Internal power supply regulator terminal (VREG5)

- ✓ VREG5 is the power supply for logic (typ 5V).
- ✓ When VM supply is powered and ST is "H", VREG5 operates.
- ✓ Please connect capacitor for stabilize VREG5. The recommendation value is 0.1 μ F.
- ✓ Since the voltage of VREG5 fluctuates, do not use it as reference voltage that requires accuracy.

●Input terminal

- ✓ The logic input pin incorporates pull-down resistor (100k Ω).
- ✓ When you set input pin to low voltage, please short it to GND because the input pin is vulnerable to noise.
- ✓ The input is TTL level (H: 2V or higher, L: 0.8V or lower).
- ✓ VREF pin is high impedance.

●OUT terminal (OUT1A, OUT1B, OUT2A, OUT2B)

- ✓ During chopping operation, the output voltage becomes equivalent to VM voltage, which can be the cause of noise. Caution is required for the pattern layout of output pin.
- ✓ The layout should be low impedance because driving current of motor flows into the output pin.
- ✓ Output voltage may boost due to back EMF. Make sure that the voltage does not exceed the absolute MAX ratings under no circumstance. Noncompliance can be the cause of IC destruction and degradation.

●Current sense resistor connection terminal (RF1, RF2)

- ✓ To perform constant current control, please connect resistor to RF pin.
- ✓ To perform saturation drive (without constant current control), please connect RF pin to GND.
- ✓ If RF pin is open, then short protector circuit operates. Therefore, please connect it to resistor or GND.
- ✓ The motor current flows into RF – GND line. Therefore, please connect it to common GND line and low impedance line.

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.