



ON Semiconductor®

<http://onsemi.com>

# LV8829LFQA

## Brushless Motor Drive PWM Driver Application Note

### Overview

The LV8829LFQA is a PWM-type driver IC designed for 3-phase brushless motors. The rotational speed can be controlled by inputting the PWM pulse from the outside, and changing Duty. The IC incorporates a latch-type constraint protection circuit.

### Function

- $I_O$  max = 1.5A (built-in output Tr)
- Speed control and synchronous rectification using direct PWM input (supports 3.3V inputs)
- 1-Hall FG output
- Latch type constraint protection circuit (the latch is released by S/S and F/R.)
- Forward/reverse switching circuit, Hall bias pin
- Power save circuit (Power save in stop mode)
- Current limiter circuit, Low-voltage protection circuit, Thermal Shutdown circuit
- Charge pump circuit, 5V regulator output.
- Start/stop circuit (short brake when motor is to be stopped)

### Typical Applications

- Laser Beam Printers
- Plain Paper Copiers
- Industrial Printers
- White Goods
- Security cameras

### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter                   | Symbol       | Conditions                    | Ratings     | Unit             |
|-----------------------------|--------------|-------------------------------|-------------|------------------|
| Supply voltage              | $V_{CC}$ max | $V_{CC}$ pin                  | 36          | V                |
|                             | $V_G$ max    | $V_G$ pin                     | 42          | V                |
| Output current              | $I_O$ max    | $t \leq 500\text{ms}$ *1      | 1.5         | A                |
| Allowable power dissipation | $P_d$ max    | Mounted on a circuit board.*2 | 1.35        | W                |
| Junction temperature        | $T_j$ max    |                               | 150         | $^\circ\text{C}$ |
| Operating temperature       | $T_{opr}$    |                               | -40 to +80  | $^\circ\text{C}$ |
| Storage temperature         | $T_{stg}$    |                               | -55 to +150 | $^\circ\text{C}$ |

\*1 :  $T_j$  cannot exceed  $T_j$  max =  $150^\circ\text{C}$

\*2 : Specified circuit board : 40mm × 50mm × 0.8mm, glass epoxy (four-layer board)

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

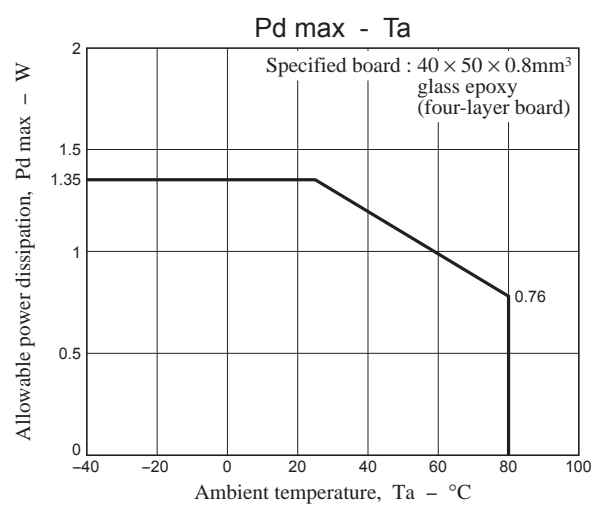
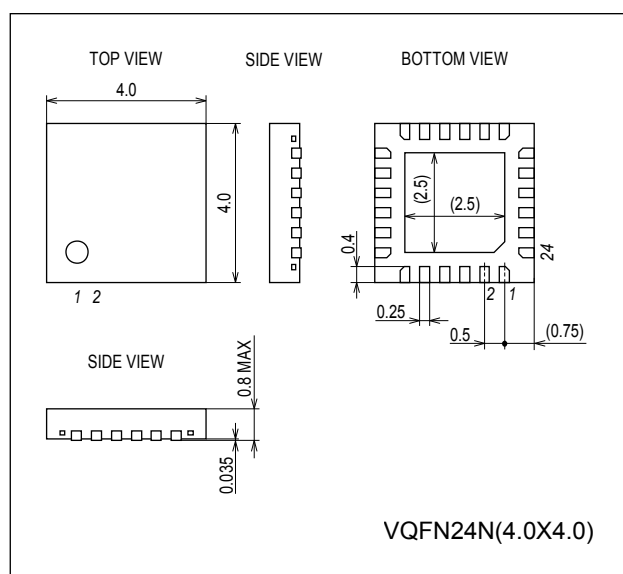
Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

# LV8829LFQA Application Note

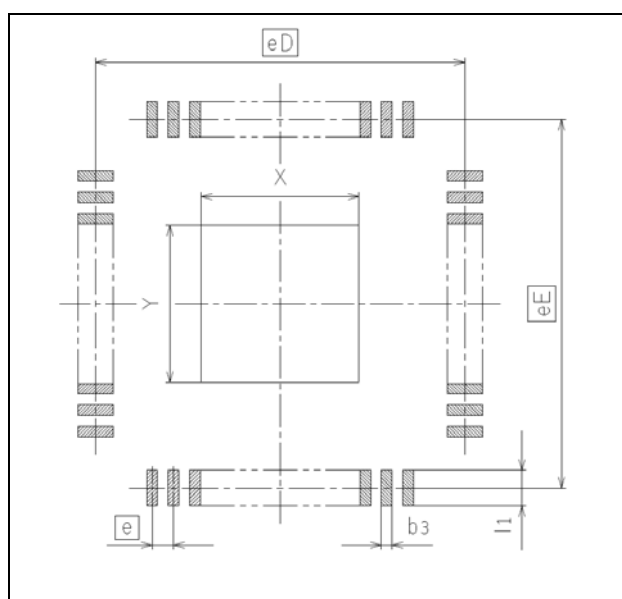
## Package Dimensions

Unit: mm(typ)



Caution: The package dimension is a reference value, which is not a guaranteed value.

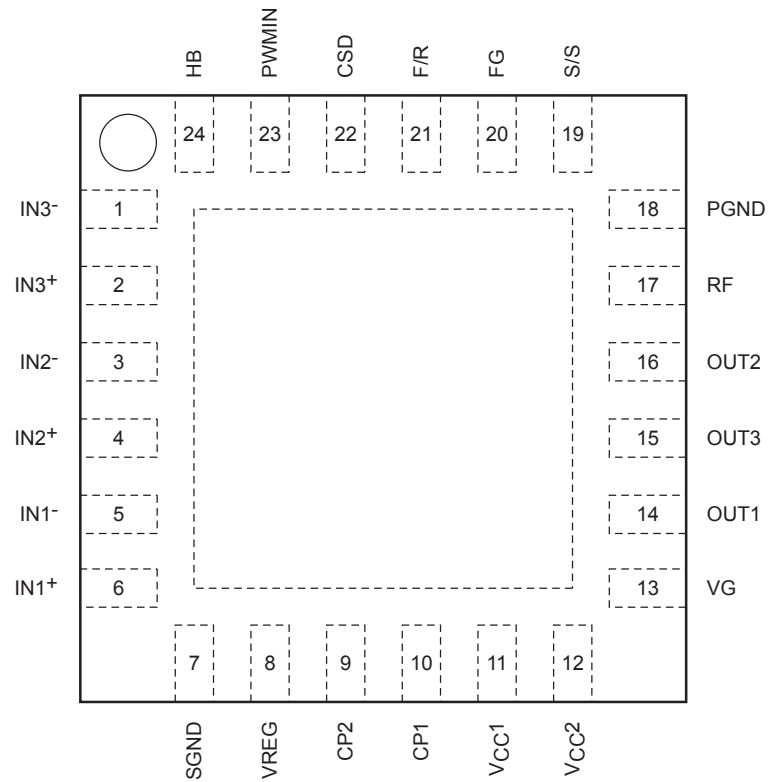
## Recommended Soldering Footprint



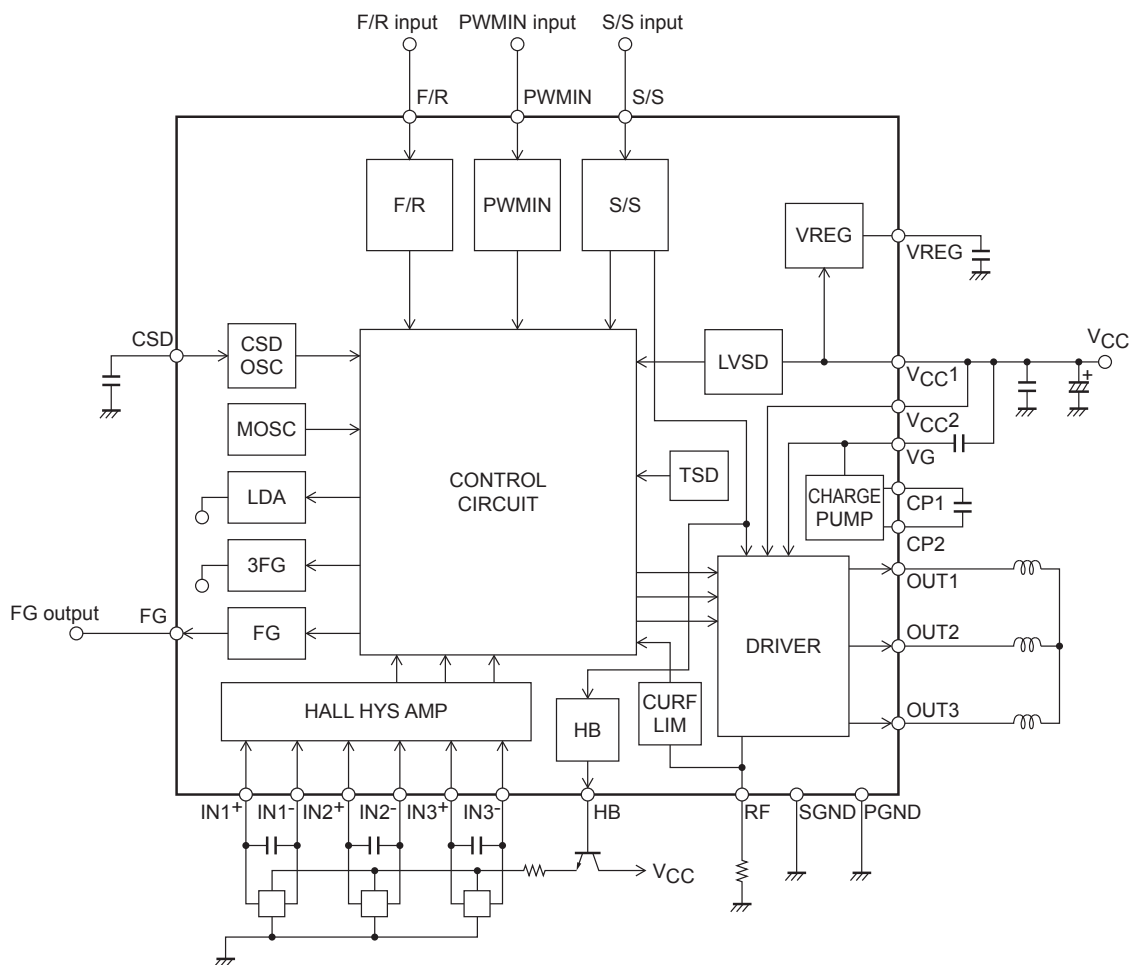
(unit: mm)

| Reference symbol | VQFN24N |
|------------------|---------|
| eD               | 3.7     |
| eE               | 3.7     |
| e                | 0.50    |
| b3               | 0.30    |
| l1               | 0.70    |
| X                | (2.5)   |
| Y                | (2.5)   |

# LV8829LFQA Application Note



**Figure1. Pin Assignment**



**Figure2. Block Diagram**

# LV8829LFQA Application Note

## Recommended Operating Conditions at Ta = 25°C

| Parameter                          | Symbol           | Conditions | Ratings |     |      | Unit |
|------------------------------------|------------------|------------|---------|-----|------|------|
|                                    |                  |            | min     | typ | max  |      |
| Supply voltage range               | V <sub>CC</sub>  |            | 8.0     |     | 35   | V    |
| 5V constant voltage output current | I <sub>REG</sub> |            | 0       |     | -10  | mA   |
| HB pin output current              | I <sub>HB</sub>  |            | 0       |     | -200 | μA   |
| FG pin applied voltage             | V <sub>FG</sub>  |            | 0       |     | 6    | V    |
| FG pin output current              | I <sub>FG</sub>  |            | 0       |     | 10   | mA   |

## Electrical Characteristics at Ta = 25°C, V<sub>CC</sub> = 24V

| Parameter                              | Symbol                  | Conditions  | Ratings |                      |                       | Unit  |
|--|-------------------------|---|---------|----------------------|-----------------------|-------|
|  |                         |   | min     | typ                  | max                   |       |
| Supply current 1                       | I <sub>CC1</sub>        |   |         | 3.3                  | 4.0                   | mA    |
| Supply current 2                       | I <sub>CC2</sub>        | At stop   |         | 0.7                  | 0.8                   | mA    |
| <b>Output block</b>                    |                         |   |         |                      |                       |       |
| Low-side output ON resistance          | R <sub>ON</sub> (L1)    | I <sub>O</sub> = 1.0A                             |         | 0.47                 | 0.65                  | Ω     |
| High-side output ON resistance         | R <sub>ON</sub> (H1)    | I <sub>O</sub> = -1.0A                            |         | 0.67                 | 0.9                   | Ω     |
| Low-side output leak current           | I <sub>L</sub> (L)      |   |         |                      | 50                    | μA    |
| High-side output leak current          | I <sub>L</sub> (H)      |   | -50     |                      |                       | μA    |
| Low-side diode forward voltage         | V <sub>D</sub> (L1)     | I <sub>D</sub> = -1.0A                            |         | 1.0                  | 1.2                   | V     |
| High-side diode forward voltage        | V <sub>D</sub> (H1)     | I <sub>D</sub> = 1.0A                             |         | 1.1                  | 1.3                   | V     |
| <b>5V Constant-voltage Output</b>      |                         |   |         |                      |                       |       |
| Output voltage                         | V <sub>REG</sub>        | I <sub>O</sub> = -5mA                             | 4.8     | 5.1                  | 5.4                   | V     |
| Line regulation                        | ΔV (REG1)               | V <sub>CC</sub> = 8 to 35V, I <sub>O</sub> = -5mA |         |                      | 50                    | mV    |
| Load regulation                        | ΔV (REG2)               | I <sub>O</sub> = -5m to -10mA                     |         |                      | 100                   | mV    |
| <b>Hall Amplifier</b>                  |                         |   |         |                      |                       |       |
| Input bias current                     | I <sub>B</sub> (HA)     |   | -2      |                      |                       | μA    |
| Common-mode input voltage range 1      | V <sub>ICM1</sub>       | When using Hall elements                          | 0.3     |                      | V <sub>REG</sub> -1.7 | V     |
| Common-mode input voltage range 2      | V <sub>ICM2</sub>       | At one-side input bias (Hall IC application)      | 0       |                      | V <sub>REG</sub>      | V     |
| Hall input sensitivity                 | V <sub>HIN</sub>        | SIN wave  | 80      |                      |                       | mVp-p |
| Hysteresis width                       | ΔV <sub>IN</sub> (HA)   |   | 9       | 20                   | 35                    | mV    |
| Input voltage Low → High               | V <sub>SLH</sub>        |   | 3       | 9                    | 16                    | mV    |
| Input voltage High → Low               | V <sub>SHL</sub>        |   | -19     | -11                  | -5                    | mV    |
| <b>CSD oscillator circuit</b>          |                         |   |         |                      |                       |       |
| High level output voltage              | V <sub>OH</sub> (CSD)   |   | 2.7     | 3.0                  | 3.3                   | V     |
| Low level output voltage               | V <sub>OL</sub> (CSD)   |   | 0.9     | 1.1                  | 1.3                   | V     |
| Amplitude                              | V (CSD)                 |   | 1.6     | 1.9                  | 2.2                   | Vp-p  |
| External capacitor charge current      | I <sub>CHG1</sub> (CSD) | V <sub>CHG1</sub> = 2.0V                          | -14     | -11.5                | -9                    | μA    |
| External capacitor discharge current   | I <sub>CHG2</sub> (CSD) | V <sub>CHG2</sub> = 2.0V                          | 9.5     | 12                   | 14.5                  | μA    |
| Oscillation frequency                  | f (CSD)                 | C = 0.022μF (Design target value)                 |         | 130                  |                       | Hz    |
| <b>Charge pump output (VG pin)</b>     |                         |   |         |                      |                       |       |
| Output voltage                         | V <sub>GOUT</sub>       |   |         | V <sub>CC</sub> +4.5 |                       | V     |
| <b>CP1 pin</b>                         |                         |   |         |                      |                       |       |
| Output ON resistance (High level)      | V <sub>OH</sub> (CP1)   | I <sub>CP1</sub> = -2mA                           |         | 500                  | 700                   | Ω     |
| Output ON resistance (Low level)       | V <sub>OL</sub> (CP1)   | I <sub>CP1</sub> = 2mA                            |         | 350                  | 500                   | Ω     |
| Charge pump frequency                  | f (CP)                  |   | 82      | 103                  | 124                   | kHz   |
| <b>Internal PWM frequency</b>          |                         |   |         |                      |                       |       |
| Oscillation frequency                  | f (PWM)                 |   | 41      | 51.5                 | 62                    | kHz   |
| <b>Current limiter operation</b>       |                         |   |         |                      |                       |       |
| Limiter voltage                        | V <sub>RF</sub>         |   | 0.19    | 0.21                 | 0.23                  | V     |
| <b>Thermal shutdown operation</b>      |                         |   |         |                      |                       |       |
| Thermal shutdown operation temperature | T <sub>SD</sub>         | *Design target value (junction temperature)       | 150     | 165                  | 180                   | °C    |
| Hysteresis width                       | ΔT <sub>SD</sub>        | *Design target value (junction temperature)       |         | 30                   |                       | °C    |

Continued on next page.

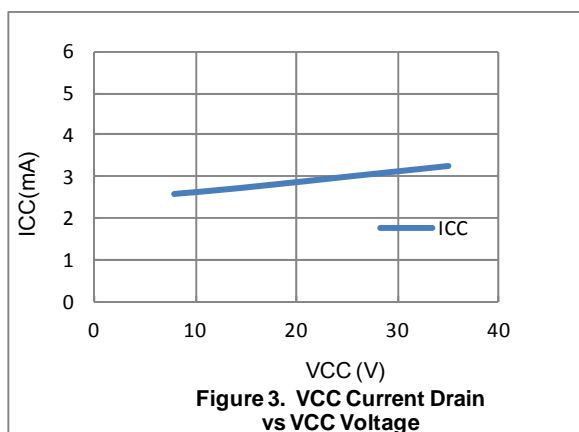
# LV8829LFQA Application Note

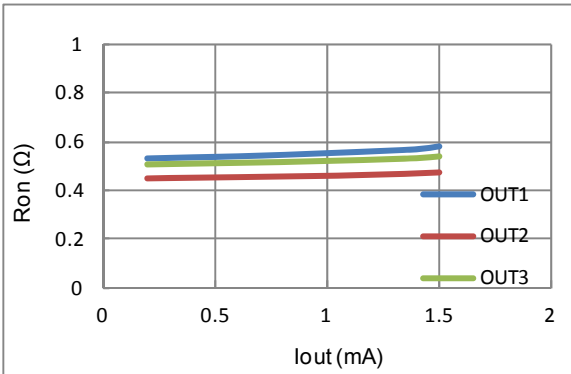
Continued from preceding page.

Continued from preceding page.

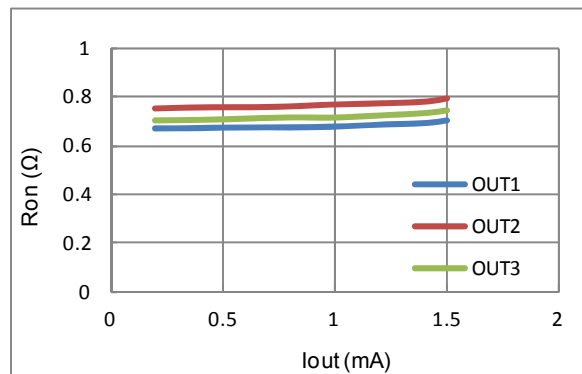
| Parameter  | Symbol     | Conditions           | Ratings  |          |          | Unit |
|--|------------|----------------------|----------|----------|----------|------|
|  |            |                      | min      | typ      | max      |      |
| <b>HB pin</b>  |            |                      |          |          |          |      |
| Output voltage   | VHB        | IHB = -100μA         | 3.4      | 3.6      | 3.8      | V    |
| <b>Low-voltage protection</b> (5V constant-voltage output detection) |            |                      |          |          |          |      |
| Operation voltage  | VSD        |                      | 3.95     | 4.15     | 4.35     | V    |
| Hysteresis width   | ΔVSD       |                      | 0.2      | 0.3      | 0.4      | V    |
| <b>FG pin</b> (3FG pin)  |            |                      |          |          |          |      |
| Output ON resistance   | VOL (FG)   | IFG = 5mA            |          | 40       | 60       | Ω    |
| Output leak current  | IL (FG)    | VO = 5V              |          |          | 10       | μA   |
| <b>S/S pin</b>   |            |                      |          |          |          |      |
| High level input voltage   | VIH (SS)   |                      | 2.0      |          | VREG     | V    |
| Low level input voltage  | VIL (SS)   |                      | 0        |          | 1.0      | V    |
| Input open voltage   | VO (SS)    |                      | VREG-2.2 | VREG-2.0 | VREG-1.8 | V    |
| Hysteresis width   | VIS (SS)   |                      | 0.25     | 0.33     | 0.4      | V    |
| High level input current   | IIH (SS)   | VSS = VREG           | 45       | 60       | 75       | μA   |
| Low level input current  | IIL (SS)   | VSS = 0V             | -115     | -90      | -65      | μA   |
| <b>PWMIN pin</b>   |            |                      |          |          |          |      |
| Recommended input frequency  | f(PWIN)    |                      | 0.5      |          | 60       | kHz  |
| High level input voltage   | VIH (PWIN) |                      | 2.0      |          | VREG     | V    |
| Low level input voltage  | VIL (PWIN) |                      | 0        |          | 1.0      | V    |
| Input open voltage   | VO (PWIN)  |                      | VREG-2.2 | VREG-2.0 | VREG-1.8 | V    |
| Hysteresis width   | VIS (PWIN) |                      | 0.25     | 0.33     | 0.4      | V    |
| High level input current   | IIH (PWIN) | VPWIN = VREG         | 45       | 60       | 75       | μA   |
| Low level input current  | IIL (PWIN) | VPWIN = 0V           | -115     | -90      | -65      | μA   |
| <b>F/R pin</b>   |            |                      |          |          |          |      |
| High level input voltage   | VIH (FR)   | *Design target value | 2.0      |          | VREG     | V    |
| Low level input voltage  | VIL (FR)   | *Design target value | 0        |          | 1.0      | V    |
| Input open voltage   | VO (FR)    |                      | VREG-2.2 | VREG-2.0 | VREG-1.8 | V    |
| Hysteresis width   | VIS (FR)   | *Design target value | 0.25     | 0.33     | 0.4      | V    |
| High level input current   | IIH (FR)   | VF/R = VREG          | 45       | 60       | 75       | μA   |
| Low level input current  | IIL (FR)   | VF/R = 0V            | -115     | -90      | -65      | μA   |

\* : Design target value and no measurement is made.

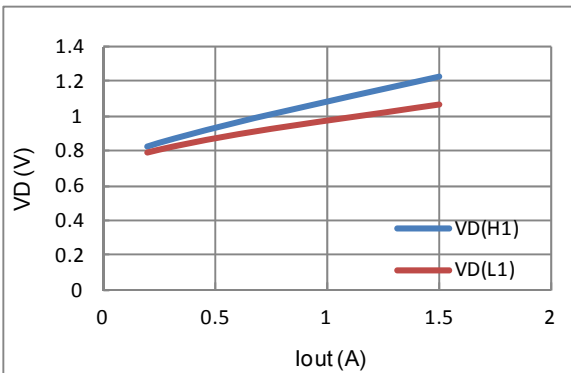




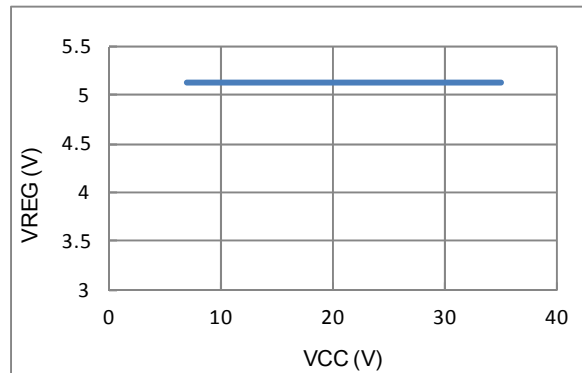
**Figure 4. Low-side Output on Resistance vs Output Current (VM=24V)**



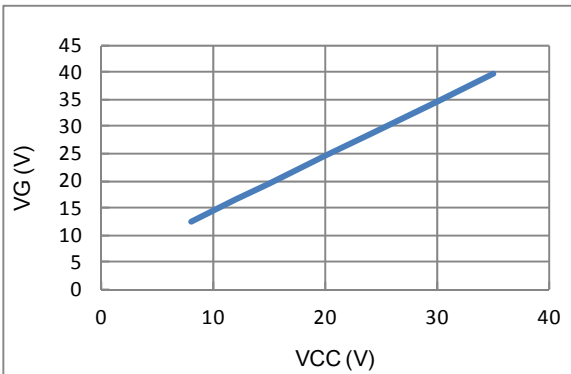
**Figure 5. High-side Output on Resistance vs Output Current (VM=24V)**



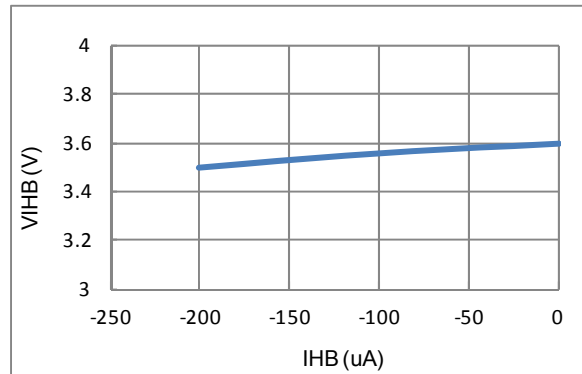
**Figure 6. Diode Forward Voltage vs Output Current**



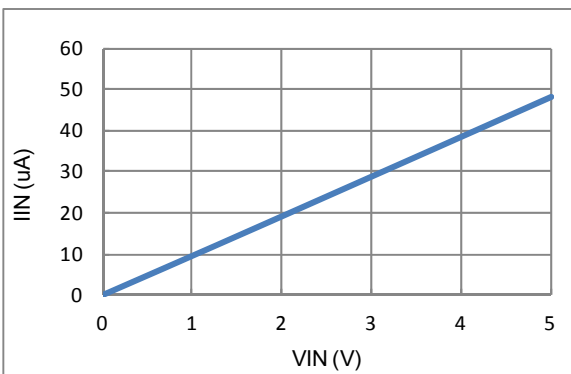
**Figure 7. VREG Output Voltage vs VCC Voltage (Io=5mA)**



**Figure 8. VG Output Voltage vs VCC Voltage**



**Figure 9. HB pin output Voltage vs HB current**



**Figure 10. Logic Pin Input Current vs Input Voltage**

# LV8829LFQA Application Note

## Pin Functions

| Pin No.                    | Pin Name   | Pin function   | Equivalent Circuit |
|----------------------------|--|--|--------------------|
| 1<br>2<br>3<br>4<br>5<br>6 | IN3 <sup>-</sup><br>IN3 <sup>+</sup><br>IN2 <sup>-</sup><br>IN2 <sup>+</sup><br>IN1 <sup>-</sup><br>IN1 <sup>+</sup> | Hall input pin.<br>•High when IN <sup>+</sup> > IN <sup>-</sup> .<br>Low in reverse relationship.<br>The input amplitude of over 100mVp-p (differential) is desirable in the Hall inputs. Insert a capacitor between the IN <sup>+</sup> and IN <sup>-</sup> pins if the noise on the Hall signal is a problem.<br>Please refer to P.11-12 for detail. |                    |
| 7                          | SGND   | Control circuit block ground pin.  |                    |
| 8                          | VREG   | 5V regulator output pin (control circuit power supply).<br>Insert a capacitor between this pin and ground for stabilization.<br>About 0.1μF is necessary.<br>(Refer to P.11 "5" is Low-voltage Protection Circuit, P.12 "10" is VREG Stabilization.)   |                    |
| 9<br>10                    | CP2<br>CP1   | Charge pump capacitor connection pin.<br>Insert capacitor between CP1 and CP2.   |                    |
| 11<br>12                   | VCC1<br>VCC2   | For Control (Pin 11) and for output (Pin 12) power pin.<br>Insert a capacitor between this pin and ground to prevent the influence of noise, etc.<br>(Refer to P.12 "9" is Power Supply Stabilization.)  |                    |
| 13                         | VG   | Charge pump output pin.<br>(Upper-side FET gate power supply)<br>Insert a capacitor between this pin and VCC.<br>(Refer to P.12 "11" is Charge pump Circuit.)  |                    |

Continued on next page.

# LV8829LFQA Application Note

Continued from preceding page.

| Pin No.        | Pin Name             | Pin function   | Equivalent Circuit |
|----------------|----------------------|--|--------------------|
| 14<br>15<br>16 | OUT1<br>OUT3<br>OUT2 | Output pin.<br>PWM is controlled by the upper-side FET.  |                    |
| 17             | RF                   | Output current detection pin.<br>Insert a low resistance resistor (Rf) between this pin and ground.<br>(Refer to P.10 "2" is Current Limiter Circuit.) |                    |
| 18             | PGND                 | Out circuit block ground pin.  |                    |
| 19             | S/S                  | Pin to select the start/stop type.<br>Stop = High or open<br>Start = Low<br>(Refer to P.12 "8" is Power Saving Circuit.)                               |                    |
| 20             | FG                   | 1-Hall FG signal output pin.<br>Open drain output.   |                    |

Continued on next page.

# LV8829LFQA Application Note

Continued from preceding page.

| Pin No. | Pin Name | Pin function  | Equivalent Circuit |
|---------|----------|---|--------------------|
| 21      | F/R      | Pin to select the forward/reverse type.<br>This pin goes to the high level when open.   |                    |
| 22      | CSD      | Pin to set the constraint protection circuit operating time and initial reset pulse.<br>Insert a capacitor between this pin and ground.<br>Insert a resistor in parallel with the capacitor if the protection circuit is not to be used.<br>(Refer to P.11 "4" is Constraint Protection Circuit.) |                    |
| 23      | PWMIN    | External PWM input pin.<br>Apply an external PWM input signal to this pin.<br>(Input frequency range is from 0.5 to 60kHz.)<br>PWM ON = Low<br>PWM OFF = High or open<br>(Refer to P.11 "3" is Speed control method.)   |                    |
| 24      | HB       | HALL bias pin (3.6V output).<br>Connect an NPN transistor.<br>(Refer to P.11 "7" Hall Input Signal.)  |                    |

## LV8829LFQA Application Note

**Three-phase logic truth table** (IN = "High" indicates the state where  $IN^+ > IN^-$ .)

("H" = SOURCE, "L" = SINK, and "M" = output OFF are shown with OUT1 to 3.)

| F/R = [H] |     |     | F/R = [L] |     |     | Output |      |      |
|-----------|-----|-----|-----------|-----|-----|--------|------|------|
| IN1       | IN2 | IN3 | IN1       | IN2 | IN3 | OUT1   | OUT2 | OUT3 |
| H         | L   | H   | L         | H   | L   | L      | H    | M    |
| H         | L   | L   | L         | H   | H   | L      | M    | H    |
| H         | H   | L   | L         | L   | H   | M      | L    | H    |
| L         | H   | L   | H         | L   | H   | H      | L    | M    |
| L         | H   | H   | H         | L   | L   | H      | M    | L    |
| L         | L   | H   | H         | H   | L   | M      | H    | L    |

| FG output |     |     |    |
|-----------|-----|-----|----|
| IN1       | IN2 | IN3 | FG |
| H         | L   | H   | L  |
| H         | L   | L   | L  |
| H         | H   | L   | L  |
| L         | H   | L   | H  |
| L         | H   | H   | H  |
| L         | L   | H   | H  |

### S/S pin, PWMIN pin

| Input state  | S/S pin            | PWMIN pin  |
|--------------|--------------------|------------|
| High or Open | Stop (short brake) | Output OFF |
| Low          | Start              | Output ON  |

### CSD function

- When the S/S pin is in a STOP state → Protection released and count reset (Initial reset)
- When the F/R pin is switched → Protection released and count reset
- When 0% duty is detected at the PWMIN pin input → Protection released and count reset
- When low-voltage condition is detected → Protection released and count reset (Initial reset)
- When TSD condition is detected → Stop counting

## Description of LV8829LFQA

### 1. Output Drive Circuit

This IC adopts a direct PWM drive method to reduce power loss in the output. It regulates the drive force of the motor by changing the output on duty. The output PWM switching is performed by the upper-side output transistor.

The current regeneration route during the normal PWMOFF passes through the parasitic diode of the output DMOS. This IC performs synchronous rectification, and is intended to reduce heat generation compared to diode regeneration.

### 2. Current Limiter Circuit

The current limiter circuit limits the output current peak value to a level determined by the equation  $I = V_{RF}/R_f$  ( $V_{RF} = 0.21V$  (typical),  $R_f$ : current detection resistor). This circuit suppresses the output current by reducing the output on duty.

The current limiter circuit has an operation delay (approx. 700ns) to detect reverse recovery current flowing in the diode due to the PWM operation, and prevent a malfunction of the current limiting operation. If the coil resistance of the motor is small, or the inductance is low, the current at startup (the state in which there is no back electromotive force generated in the motor) will change rapidly. As a result, the operation delay may sometimes cause the current limiting operation to take place at a value above the set current. In such a case, it is necessary to set the current limit value while taking into consideration the increase in current due to the delay.

\* Regarding the PWM frequency in the current limiter circuit

The PWM frequency in the current limiter circuit is determined by the internal reference oscillator, and is approximately 50 kHz.

### 3. Speed control method

Pulses are input to the PWMIN pin, and the output can be controlled by varying the duty cycle of these pulses.

When a low-level input voltage is applied to the PWMIN pin, the output at the PWM side (upper side) is set to ON.

When a high-level input voltage is applied to the PWMIN pin, the output at the PWM side (upper side) is set to OFF.

If it is necessary to input pulses using inverted logic, this can be done by adding an external transistor (NPN).

When the input to the PWMIN pin remains high-level for a certain period, the IC judges that the duty is 0%, causing the CSD circuit count to be reset and the output from the HB pin to become low level.

### 4. Constraint Protection Circuit

The LV8829LFQA includes a constraint protection circuit for protecting the IC and the motor in a motor constraint mode.

This circuit operates when the motor is in an operation condition and the Hall signal does not switch over for a certain period. Note that while this constraint protection is operating, the upper-side output transistor will be OFF.

Time setting is performed according to the capacitance of the capacitor connected to the CSD pin.

$$\text{Set time (s)} \approx 90 \times C (\mu\text{F})$$

When a 0.022 $\mu\text{F}$  capacitor is connected, the protection time becomes approximately 2.0 seconds. The set time must be selected to a value that provides adequate margin with respect to the motor startup time.

Conditions for releasing the constraint protection state:

- When the S/S pin is in a STOP state → Protection released and count reset (Initial reset)
- When the F/R pin is switched → Protection released and count reset
- When 0% duty is detected at the PWMIN pin input → Protection released and count reset
- When low-voltage condition is detected → Protection released and count reset (Initial reset)
- (• When TSD condition is detected → Stop counting)

The CSD pin also functions as the initial reset pulse generation pin. If it is connected to ground, the logic circuit will go into a reset state, preventing speed control from taking place. Consequently, when not using constraint protection, connect a resistor of approximately 220k $\Omega$  and a capacitor of about 4700pF in parallel to ground.

### 5. Low-voltage Protection Circuit

The LV8829LFQA incorporates a comparator that uses the band gap voltage as the reference. The circuit monitors the voltage at the VREG pin (5V) while the S/S pin is low and activates the protection circuit when the voltage at the VREG pin falls below 4.15V (typ.).

When this happens, the state of the output transistors for all phases set to OFF.

In order to ensure that the IC does not exhibit any unstable behavior when the VREG voltage has increased or decreased around 4.15V, a hysteresis of 0.3V (typ.) is provided. As a result, when the VREG voltage recovers to 4.45V (typ.) after the low-voltage protection circuit has been activated, all output transistors return to their operating state.

### 6. Thermal shutdown Circuit

When the IC junction temperature exceeds 165°C (design target value), the thermal shutdown circuit is activated, and all the output transistors are set to OFF.

When the IC junction temperature goes below the hysteresis temperature of 30°C (design target value) or more, all the output transistors return to their operating state.

However, as the thermal shutdown circuit is activated only when the junction temperature of the IC has exceeded the rating, its activation does not constitute a guarantee that the product that incorporates this circuit will be protected from damage or destruction.

### 7. Hall Input Signal

A pulse input with the amplitude in excess of the hysteresis (35mV maximum) is required for the Hall inputs. It is desirable that the amplitude of the Hall input signal be 100mVp-p or more in consideration of the effect of noise and phase displacement.

If disturbances to the output waveform (during phase switching) occur due to noise, connect a capacitor between the Hall input pins to prevent such disturbances. In the constraint protection circuit, the Hall input is utilized as a judgment signal. Although the circuit ignores a certain amount of noise, caution is necessary.

If all three phases of the Hall input signal go to the same input state (HHH or LLL), the outputs are all set to the OFF state.

## LV8829LFQA Application Note

If the Hall IC is used, fixing one side of the inputs (either the + or – side) at a voltage within the common-mode input voltage range (between 0.3V and VREG-1.7V) allows the other input side to be used as an input over the 0V to VREG range.

- Method of connecting Hall elements

Type (1) connection (three Hall elements connected in series)

Advantages

- Because the current flowing in Hall elements can be shared by connecting the Hall elements in series, the current consumption is less than that of a parallel-connected arrangement.
- The use of a current limiting resistor can be eliminated.
- Fluctuations of amplitude with temperature are reduced.

Disadvantages

- Because only 1V can be applied to one Hall device, there is a possibility that adequate amplitude cannot be obtained.
- The current flowing in the Hall elements varies with temperature.
- HALL element unevenness (input resistance in particular) is easy to influence the amplitude.

Type (2) connection (three Hall elements connected in parallel)

Advantages

- The current flowing in the Hall elements can be determined by the current limiting resistor.
- The voltage applied to the Hall elements can be varied, enabling adequate amplitude to be obtained.

Disadvantages

- Because it is necessary to supply current separately to each Hall element, the current consumption becomes large.
- A current limiting resistor is necessary.
- The amplitude varies with temperature.

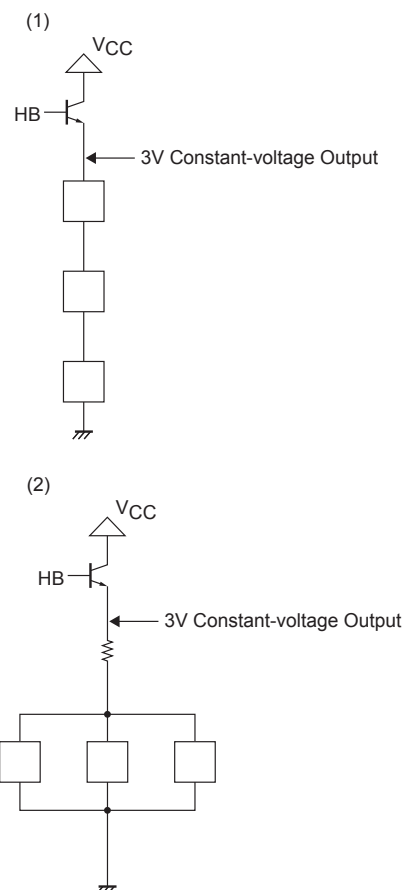


Figure11. Method of connecting Hall elements

- HB pin

The HB pin is used for cutting off the current flowing in the Hall elements during standby (for saving electricity).

The output from the HB pin is set to OFF in the following cases.

- When the S/S pin is in a STOP state
- When 0% duty is detected at the PWMIN pin input

### 8. Power Saving Circuit (Start/Stop circuit)

To save power when the LV8829LFQA is in the stop state, most of the circuit is stopped, aiming at reducing current consumption. If the Hall bias pin is used, the current consumption in the power-saving mode will be approximately 700μA. Even in the power-saving mode, a 5V regulator voltage is output. Also, in the power-saving mode, the IC is in a short break state. (lower-side shorted)

### 9. Power Supply Stabilization

This IC generates a large output current, and employs a switching drive method, so the power supply line level can be disturbed easily. For this reason, it is necessary to connect a capacitor (electrolytic) of sufficient capacitance between the VCC pin and ground to ensure a stable voltage. Connect the ground side of the capacitor to the PGND pin, which is the power ground, as close as possible to the pin. If it is not possible to connect a capacitor of sufficiently large capacitance close to the pin, connect a ceramic capacitor of approximately 0.1μF to the vicinity of the pin.

If diodes are inserted in the power supply line to prevent IC destruction resulting from reverse-connecting the power supply, the power supply lines are even more easily disrupted. And even larger capacitor is required.

### 10. VREG Stabilization

To stabilize the VREG voltage, which is the power supply for the control circuit, connect a capacitor of 0.1μF or larger.

Connect the ground of this capacitor as close as possible to the control block ground (SGND pin) of the IC.

## 11. Charge pump Circuit

The voltage is stepped-up by the charge pump circuit, causing the gate voltage of the upper-side output FET to be generated. The voltage is stepped-up by capacitor CP connected between pins CP1 and CP2, causing charge to accumulate in capacitor CG connected between pins VG and V<sub>CC</sub>. The capacitance of CP and CG must always satisfy the following relationship.

$$CG \geq 4 \times CP$$

Charging and discharging of capacitor CP take place based on a frequency of 100k Hz. When the capacitance of capacitor CP is large, the current supply capability of power supply VG will increase. However, if the capacitance is too large, the charging and discharging operations will be insufficient. The larger the capacitance of capacitor CG, the more stable voltage VG will become. However, if the capacitance is made too large, the period during which voltage VG is generated when the power is switched ON will become long, so caution is necessary.

The capacitance settings of CP and CG should be the following.

$$CP = 0.01\mu F$$

$$CG = 0.1\mu F$$

## 12. Difference point of LV8829LFQA and LV8827LFQA

This difference that IC is the more following compared with LV8827LFQA exists.

|  | LV8829LFQA  | LV8827LFQA                        |
|--|---|-----------------------------------|
| When Duty=0% of PWM input is detected  | Synchronous rectification OFF<br>(Free run)               | Short brake                       |
| At the low frequency number of PWM input<br>(About 7.5kHz under)             | Synchronous rectification OFF                             | Like synchronous rectification ON |
| At low ON Duty of the PWM input<br>(ex. frequency: 20kHz, ON Duty: 3% under) | Synchronous rectification OFF                             | Like synchronous rectification ON |
| Backflow current detecting function  | It is.<br>(At detection -> Synchronous rectification OFF) | non                               |

## 13. Metal part at the rear of the IC

The metal part at the rear of the IC (exposed die-pad) constitutes the sub ground of the IC, so connect it to the control ground (SGND pin) and power ground pin (PGND) at points close to the IC.

## 14. Notes on Using the IC

This IC performs synchronous rectification in order to achieve high-efficiency drive.

The synchronous rectification operation reduces the output transistor loss so it has the effect of reducing heat generation and improving efficiency.

However, the synchronous rectification operation may cause the supply voltage to rise depending on the conditions under which the IC is used, such as:

- When the output duty ratio has suddenly decreased
- When the PWM input frequency is low, etc.

Protective measures must be taken to ensure that the maximum ratings are not exceeded even when the supply voltage has risen. These measures include:

- Appropriate selection of the capacitance of the capacitor inserted between the power supply and the ground
- Insertion of a zener diode between the power supply and the ground

# LV8829LFQA Application Note

## Typical Application Circuit (Hall IC)

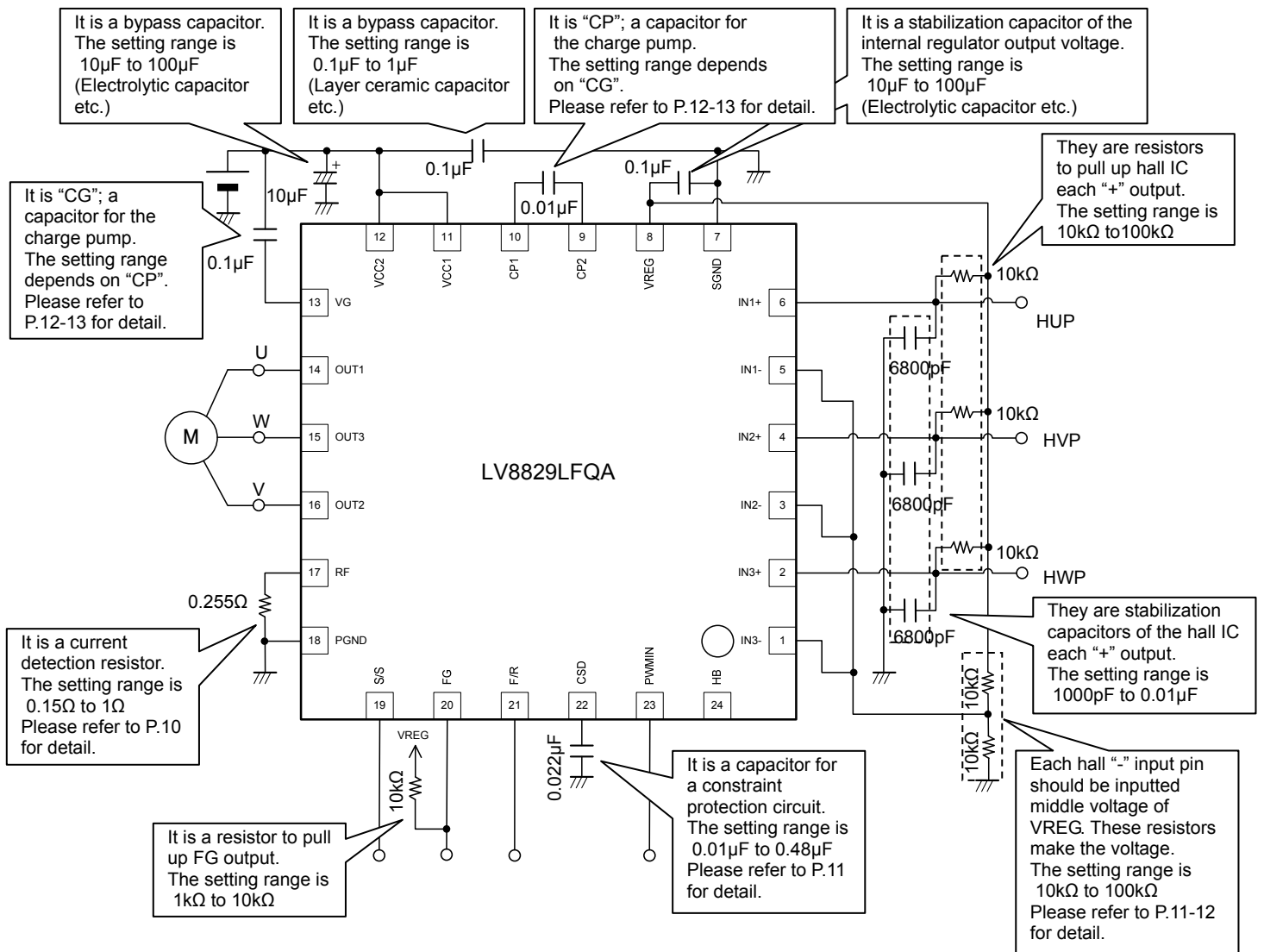


Figure12. Typical application Circuit for a motor with Hall ICs

# LV8829LFQA Application Note

## (Hall Elements)

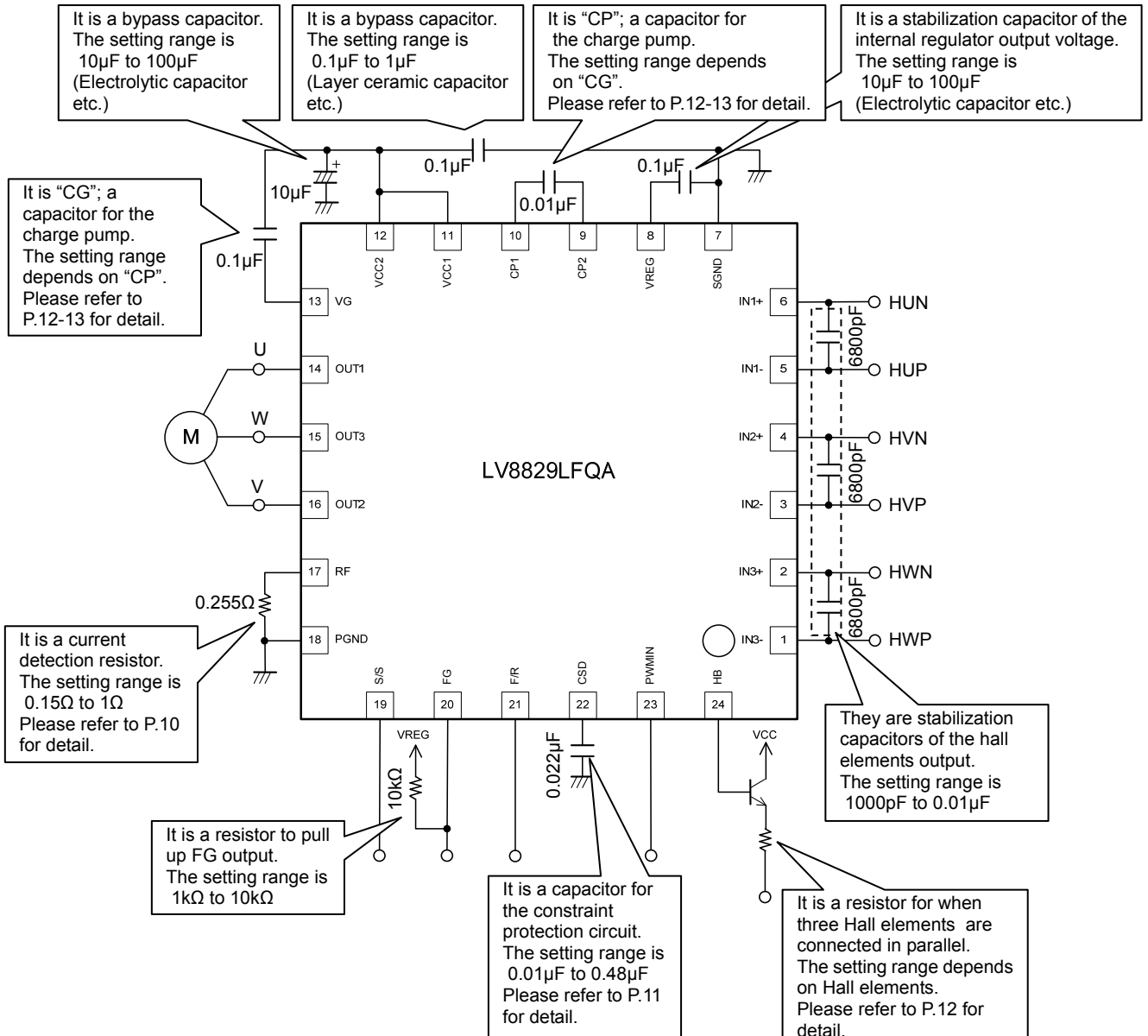


Figure13. Typical application Circuit for a motor with Hall elements

# LV8829LFQA Application Note

**Evaluation Board** ("M-DrAGON means Motor-Driver And GUI produced by ON semiconductor)

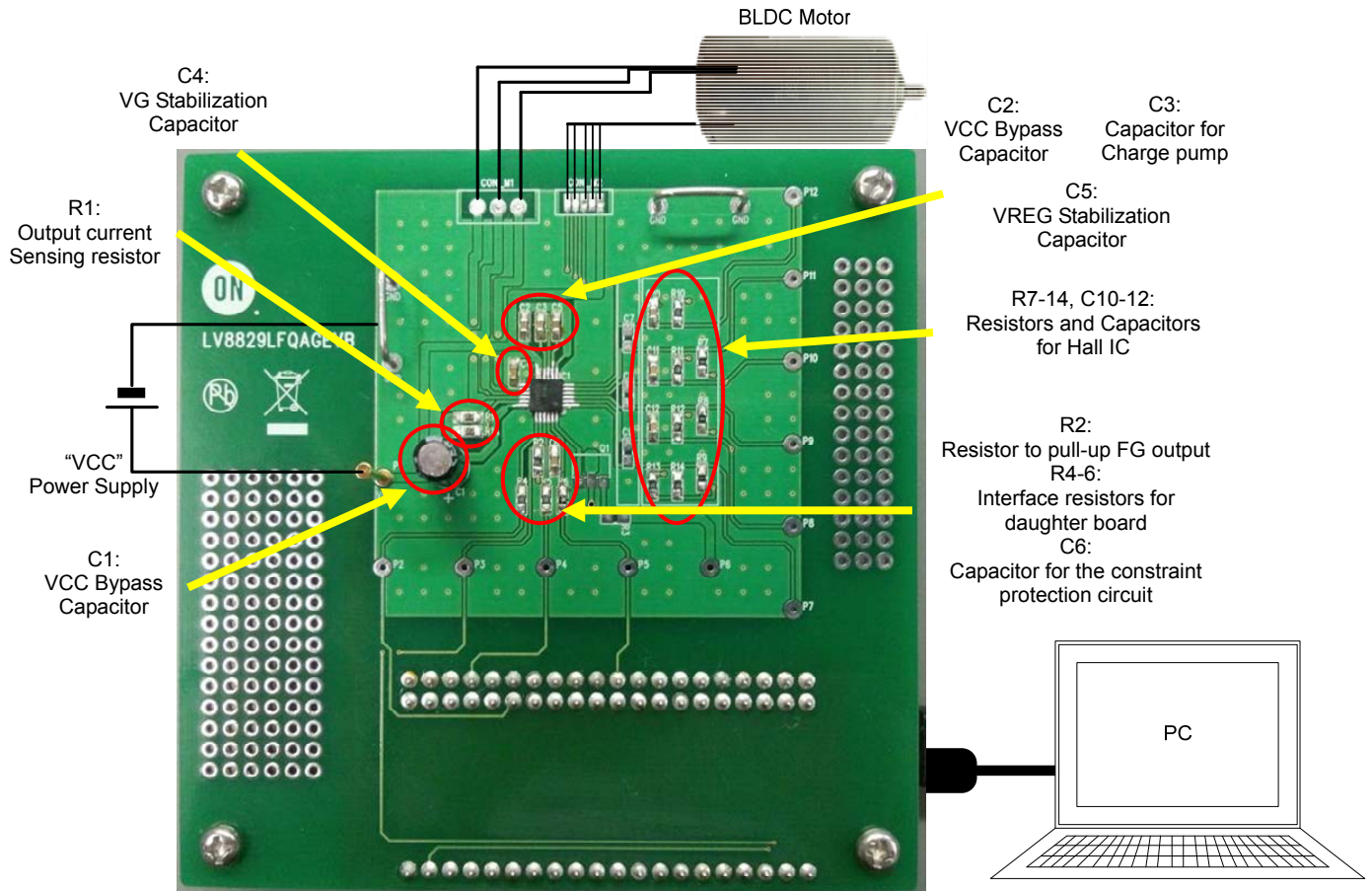


Figure14. "M-DrAGON" overview (Top view)

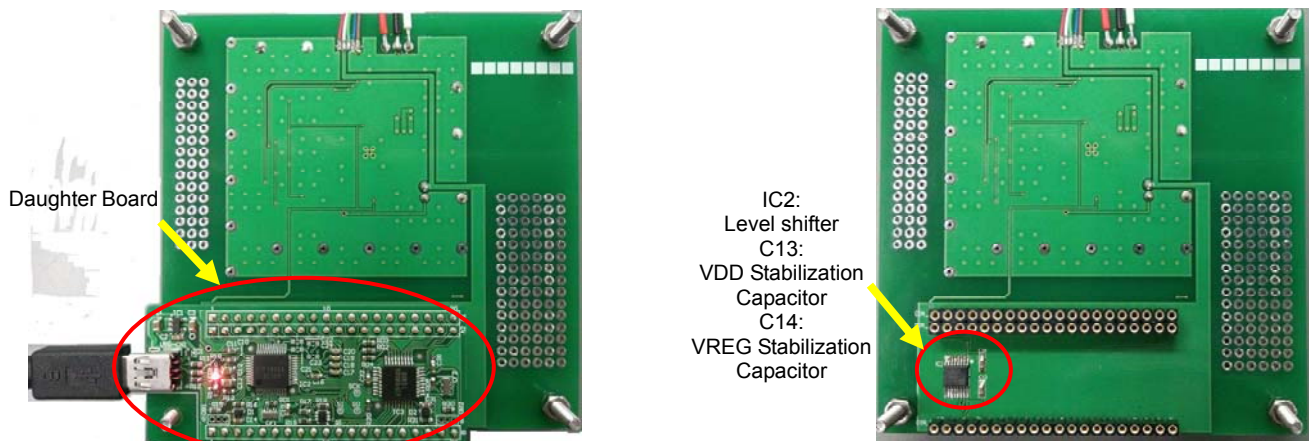


Figure15. "M-DrAGON" overview (Bottom view)

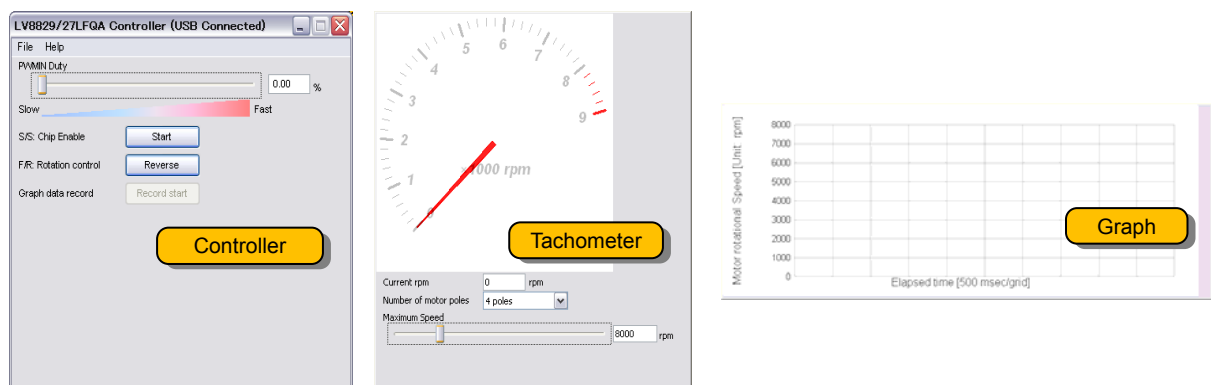


Figure16. Images of GUI

# LV8829LFQA Application Note

## Bill of Materials for LV8829LFQA Evaluation Board

| Designator     | Quantity | Description                  | Value        | Tolerance | Footprint      | Manufacturer              | Manufacturer Part Number | Substitution Allowed | Lead Free |
|----------------|----------|------------------------------|--------------|-----------|----------------|---------------------------|--------------------------|----------------------|-----------|
| IC1            | 1        | Motor Driver                 | -            | -         | VQFN24N        | ON Semiconductor          | LV8829LFQA               | No                   | Yes       |
| IC2            | 1        | Level Shifter                | -            | -         | TSSOP16        | ON Semiconductor          | MC14504B                 | No                   | Yes       |
| R1             | 2        | Thick film Resistor          | 0.51Ω,0.25W  | ±5%       | 2012(0805Inch) | Rohm                      | MCR10EZHLR51             | Yes                  | Yes       |
| R2             | 1        | Thick film Resistor          | 10kΩ,0.1W    | ±5%       | 1608(0603Inch) | Rohm                      | MCR03ERTJ103             | Yes                  | Yes       |
| R4-6           | 3        | Thick film Resistor          | 200Ω,0.1W    | ±5%       | 1608(0603Inch) | Rohm                      | MCR03ERTJ201             | Yes                  | Yes       |
| R7-9           | 3        | Jumper                       | 0Ω,0.1W      | ±5%       | 1608(0603Inch) | Rohm                      | MCR03ERTJ000             | Yes                  | Yes       |
| R10-14         | 5        | Thick film Resistor          | 10kΩ,0.1W    | ±5%       | 1608(0603Inch) | Rohm                      | MCR03ERTJ103             | Yes                  | Yes       |
| C1             | 1        | Electrolytic Capacitor       | 10μF, 50V    | ±20%      | F2.0-5         | SUN Electronic Industries | 50ME10HC                 | Yes                  | Yes       |
| C2             | 1        | Ceramic multilayer Capacitor | 0.1μF, 100V  | ±10%      | 1608(0603Inch) | Murata                    | GRM188R72A104KA35*       | Yes                  | Yes       |
| C3             | 1        | Ceramic multilayer Capacitor | 0.01μF, 50V  | ±10%      | 1608(0603Inch) | Murata                    | GRM188B11H103KA01*       | Yes                  | Yes       |
| C4             | 1        | Ceramic multilayer Capacitor | 0.1μF, 100V  | ±10%      | 1608(0603Inch) | Murata                    | GRM188R72A104KA35*       | Yes                  | Yes       |
| C5             | 1        | Ceramic multilayer Capacitor | 0.1μF, 100V  | ±10%      | 1608(0603Inch) | Murata                    | GRM188R72A104KA35*       | Yes                  | Yes       |
| C6             | 1        | Ceramic multilayer Capacitor | 0.022μF, 50V | ±10%      | 1608(0603Inch) | Murata                    | GRM188B11H223KA01*       | Yes                  | Yes       |
| C10-12         | 3        | Ceramic multilayer Capacitor | 6800pF, 50V  | ±10%      | 1608(0603Inch) | Murata                    | GRM188B11H682KA01*       | Yes                  | Yes       |
| C13,14         | 2        | Ceramic multilayer Capacitor | 0.1μF, 100V  | ±10%      | 1608(0603Inch) | Murata                    | GRM188R72A104KA35*       | Yes                  | Yes       |
| Daughter Board | 1        | Interface board              | -            | -         | -              | ON Semiconductor          | -                        | No                   | Yes       |
| CN-A1,A2,B     | 3        | Female Socket                | -            | -         | -              | MAC8                      | PM-61                    | Yes                  | Yes       |
| CON_M1         | 1        | Socket to Motor              | -            | -         | -              | JST                       | B3B-EH                   | No                   | Yes       |
| CON_M2         | 1        | Socket to Motor              | -            | -         | -              | JST                       | BM05B-SRSS-TB            | No                   | Yes       |
| P1             | 1        | Test Point                   | -            | -         | -              | MAC8                      | ST-1-3                   | Yes                  | Yes       |
| USB cable      | 1        | A-MiniB                      | -            | -         | -              | -                         | -                        | Yes                  | Yes       |
| Ref Motor      | 1        | BLDC motor                   | 18V-1A       | -         | -              | Minebea                   | BLIM2430H-A01            | Yes                  | Yes       |

# LV8829LFQA Application Note

## Evaluation Board circuit

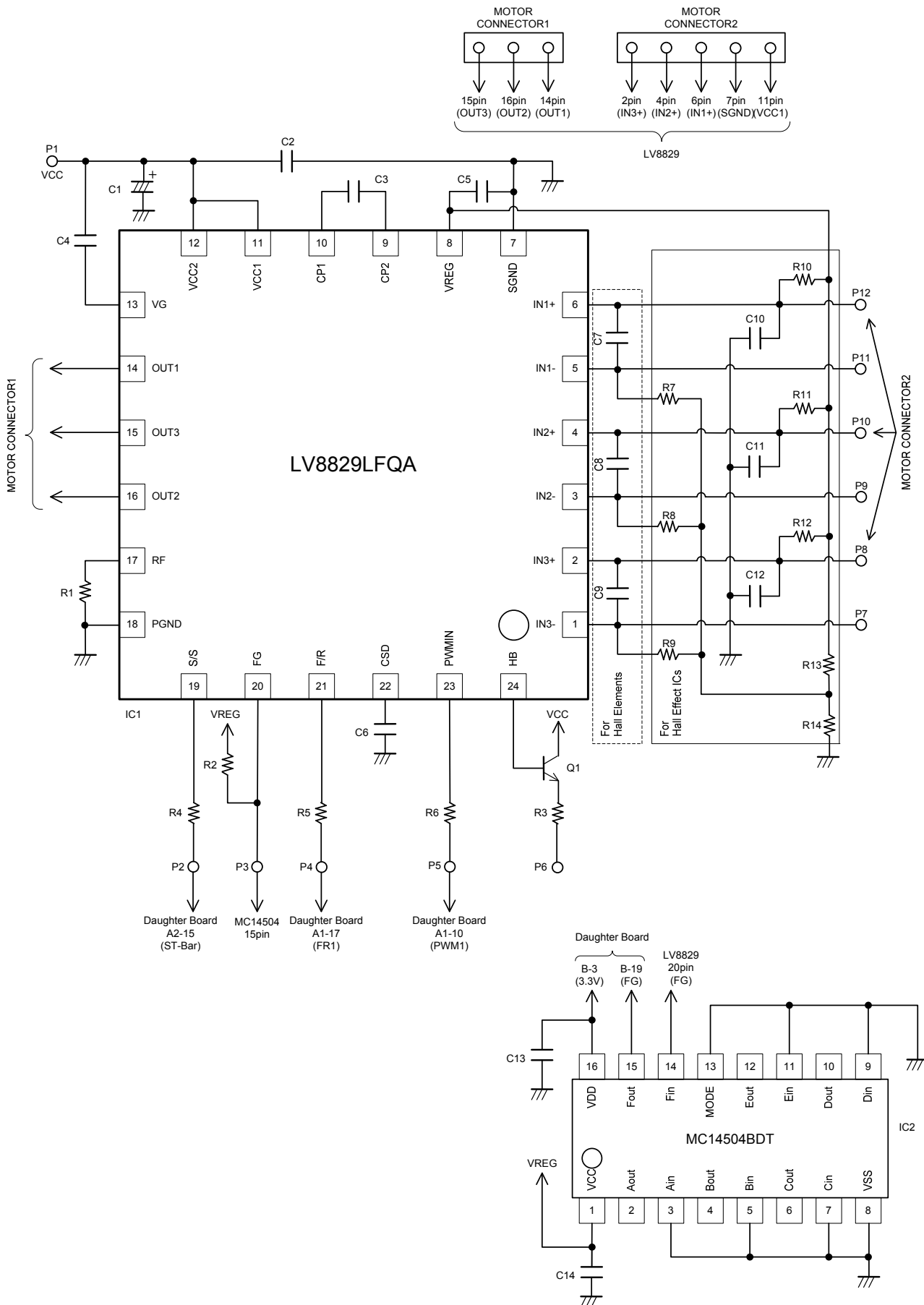


Figure17. Evaluation Board Circuit Schematic

## LV8829LFQA Application Note

---

### Operation Guide

- Connect a 3-phase Brushless DC motor with MOTOR CONNECTOR1 and MOTOR CONNECTOR2 or P7-12.  
(When we provide the Evaluation Board, it is mounted peripheral parts for Hall ICs.  
Because the BLDC motor that we provide is built-in Hall ICs.  
When you drive the BLDC with Hall elements, please remove R7-14, C10-12 and mount R3, C7-9, connect + terminal of the Hall elements to P6. Refer to P.11-12 for detail.  
When you control LV8829LFQA by your DSP, please remove the Daughter Board and input signals to P2-5.)
- Please start up the system in following procedure.
  1. Plug an USB cable into the Daughter Board.
  2. Start up the GUI for LV8829LFQA.
  3. Apply input voltage to the terminal P1 "VCC".  
Don't apply voltage before plugging USB into the Daughter Board and starting the GUI.
  4. Input drive signals by GUI.
- When you unplug the daughter board, turn "VCC" off at first.

### The points of attention to design applications

- Do not exceed the absolute maximum ratings under no circumstance.
- VCC, and each OUT, where large current flows should be laid out as fat and short as possible.
- The metal part at the rear of the IC (exposed die-pad) constitutes the sub ground of the IC, so connect it to the control ground (SGND pin) and power ground pin (PGND) at points close to the IC.
- VCC bypass capacitor, especially Ceramic multilayer Capacitor should be mounted as near as possible to VCC pin of LV8829LFQA.
- VREG should be used in the IC as reference voltage. Capacitor should be connected between VREG pin and GND to stabilize VREG. Therefore, the capacitor should be mounted as near as possible to VREG pin.
- The impedance of the island of GND needs to be as low as possible by making through-holes, for example.
- We recommend that the GND lines to connect a motor and the GND area of MCUs are laid out independently and single-point-grounded at VM bypass capacitor
- VREG can not be recommended to use for peripheral circuits because their output voltage are not so high in precision.

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.