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AN-9017

Manufacturing Technology of a Small Capacity Inverter Using a Fairchild IGBT

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2.1 Selection of the Resistance Value Considering the Gate Drive IC Drive Capability

The value of the gate resistance, R_G , connected to the gate drive IC output is determined based on the peak current (I_{ON} , $I_{OFF,PEAK}$) which is charged and discharged between the gate and the emitter. The maximum current which can electrically charge the gate oxide between the gate and the emitter is determined based on the maximum source current of the gate drive IC. On the other hand, the maximum current which can discharge the gate oxide is determined based on the maximum sink current of the gate drive IC. The minimum gate resistance value, R_G , is, in turn, determined based on these determined maximum charge and discharge currents.

Determination of the Minimum R_G Based on the Maximum Drive Capability of the Gate Drive IC

If we assume that the equivalent capacitance (C_{GE}) between the IGBT emitter and gate has discharged to the gate drive turn off voltage (V_{OL}) to obtain the minimum value of the turn on resistance R_{ON} and that the capacitance has charged to the gate drive turn on voltage (V_{OH}) to obtain the minimum value of the turn off resistance R_{OFF} , the following relationships can be derived from Ohm's Law. .

$$R_{ON}^{MIN} = \frac{V_{OH} - V_{OL}}{I_{SOURCE}^{MAX}} \quad \text{and} \quad R_{OFF}^{MIN} = \frac{V_{OH} - V_{OL}}{I_{SINK}^{MAX}} \quad (1)$$

Where,

R_{ON}^{MIN} = Minimum value of the turn on resistance,

R_{OFF}^{MIN} = Minimum value of the turn off resistance,

V_{OH} = Turn on output maximum voltage of the gate drive IC

V_{OL} = Turn off output minimum voltage of the gate drive IC

I_{SOURCE}^{MAX} = Maximum output source current of the gate drive IC

I_{SINK}^{MAX} = Maximum output sink current of the gate drive IC

Because the maximum sink current is generally greater than the source current in the gate drive IC output ($I_{SOURCE}^{MAX} < I_{SINK}^{MAX}$), the selected gate resistance must be greater than R_{ON}^{MIN} if the turn on and turn off resistances are not separated and used as one.

Calculation of the Power Loss in the Gate Drive IC

The total power loss (P_T) in the gate drive can be calculated from the following equation. .

$$\begin{aligned} P_T &= P_{BIAS} + P_{SWITCH} \\ &= I_{CC} V_{CC} + I_{EE} V_{EE} + E_{SWITCH} f_{SWITCH} \end{aligned} \quad (2)$$

where,

P_{BIAS} : Power consumed to bias the elements in the IC in normal state

P_{SWITCH} : Switching loss associated with turning on and off the IGBT gate

E_{SWITCH} : Average loss ($\mu J/cycle$) in the IC during one cycle of turning on and off.

f_{SWITCH} : Average turn off frequency

V_{CC} : + power supply voltage

V_{EE} : - power supply voltage

I_{CC} : Average + power supply current in normal state

I_{EE} : Average - power supply current in normal state

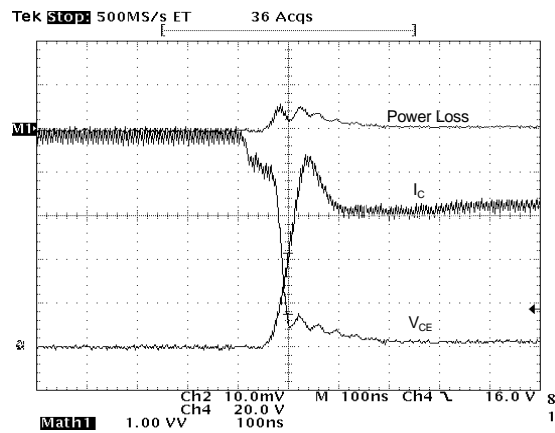
If the gate resistance is lowered, the E_{SWITCH} value decreases, and switching speed increase. If the switching speed is increased, P_{SWITCH} value decreases. The total power loss calculated from the above equation should not exceed the maximum value identified in the data book.

2.2 Selection of the Resistance value considering the IGBT Drive Conditions

The relationship between the switching loss and the gate resistance

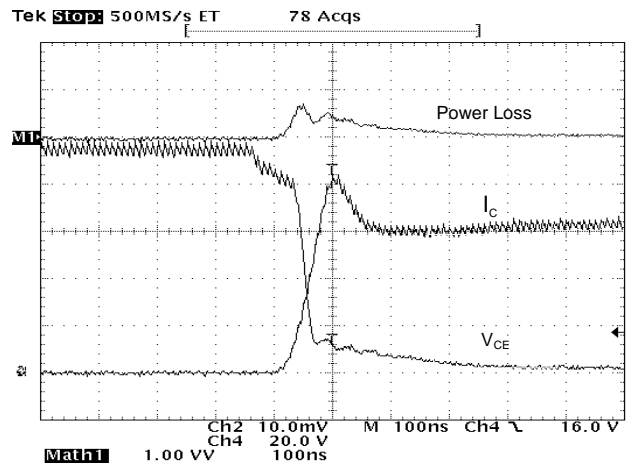
The IGBT is designed such that the MOSFET driven by the gate turns on the output bipolar TR. Because the determined maximum current between the drain and source of the MOSFET is proportional to the gate voltage, the IGBT turn on characteristic is affected by the magnitude of the voltage and current applied to the gate. This turn on characteristic significantly affects the IGBT turn on loss. Therefore, if the magnitude of the turn on resistance is reduced, the internal MOSFET turns on quickly, and as a result, the switching loss also reduces. The following figure shows each of the waveforms which are turned on when the gate resistance is changed in the Fairchild IGBT SGP5N60RUFD.

Test Condition: $L = 78[\mu\text{H}]$, $R = 21.2[\Omega]$, $T = 25[^\circ\text{C}]$, $V_{\text{OH}} = 15[\text{V}]$
 $V_{\text{CC}} = 80[\text{V}]$ (20V/DIV), $I_{\text{C}} = 3[\text{A}]$ (1A/DIV)



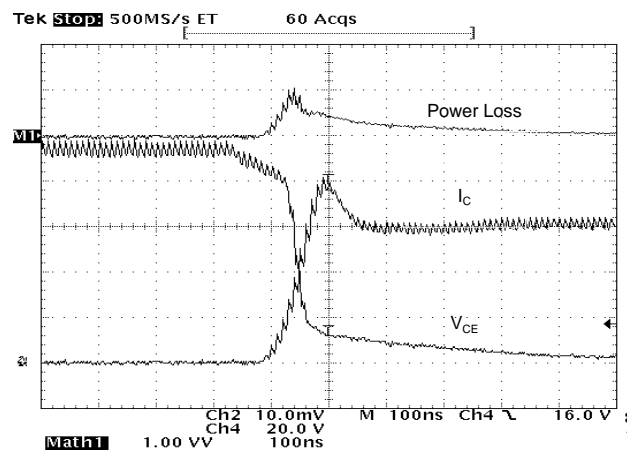
$$R_{\text{ON}} = 40[\Omega]$$

Figure 2.2.1



$$R_{ON} = 80[\Omega]$$

Figure 2.2.2



$$R_{ON} = 120[\Omega]$$

Figure 2.2.3

Figure 2.2 Turn on waveforms of SGP5N60RUF D when the gate resistance is changed.

The following table summarizes the turn on losses measured from the above tests. The areas of the waveforms for the consumed power above were converted to the power loss values used in the table.

SGP5N60RUFD

$R_{ON}(\Omega)$	40	60	80	100	120
Loss(μ J)	4.22	5.62	7.93	11.04	12.63

SGP10N60RUFD

$R_{ON}(\Omega)$	40	60	80	100	120
Loss(μ J)	3.16	3.58	4.73	5.31	6.44

Table 2.1 Relationship between the Turn on Loss and Gate Resistance

The figures and tables above reveal that the turn on losses increase as the gate resistance is increased. The turn off speed is affected more by the minority carrier recombination mechanism, an inherent feature of the IGBT output bipolar TR, than by the MOSFET turn off speed. Therefore, there is a relatively small relationship between the magnitude of the gate resistance and the turn off speed. However, if the gate resistance increases above a specific value, the turn off speed becomes affected more by the internal MOSFET turn off time than by the minority carrier recombination time. This reduces the IGBT turn off speed and, in turn, increases the turn off loss. Hence, the turn-off resistance must be maintained below an appropriate value. The following table summarizes the turn off loss under the same test conditions as the turn on test.

SGP5N60RUFD

$R_{ON}(\Omega)$	40	60	80	100	120
Loss(μ J)	65.9	65.9	66.2	66.4	67.2

SGP10N60RUFD

$R_{ON}(\Omega)$	40	60	80	100	120
Loss(μ J)	45.9	45.9	47.3	47.3	49.8

Table 2.2 Relationship between the Turn off Loss and Gate Resistance

There is almost no change in the turn off loss with the change in the gate resistance.

Relationship between the Gate Resistance and dv/dt Sensitivity

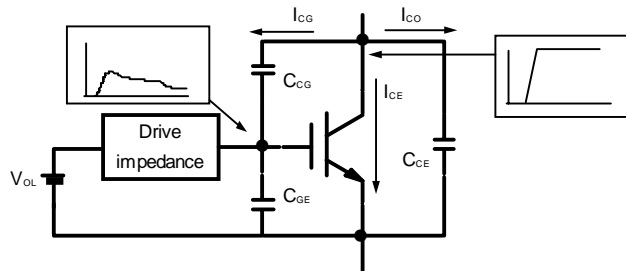


Figure 2.3 Equivalent Circuit Depicting a Gate which Turns on by the dv/dt

IGBTs, as shown in Figure 2.3, have individual capacitances between the emitter and the gate and between the gate and the collector. The capacitance C_{ge} between the emitter and the gate, and the capacitance C_{gc} called the Miller capacitance between the gate and the collector play important roles. Not only does the Miller capacitance, like the Miller effect, delay the IGBT turn on time, but it also allows the current of $C_{gc} \times dv/dt$ to flow in when there is a sudden change in the voltage between the emitter and collector. Thus, producing a voltage of $R_{OFF} \times C_{gc} \times dv/dt + V_{OL}$ at the gate. The moment that this voltage becomes greater than the minimum voltage needed to turn on the gate, V_{TH} , the IGBT turns on causing a situation similar to a short circuit. Accordingly, the maximum gate off resistance value can be obtained from the following equation.

$$R_{OFF} \leq \frac{V_{TH} - V_{OL}}{C_{gc} \times dv/dt} \quad (3)$$

If the gate turn off voltage V_{OL} is negative or V_{TH} is large, R_{OFF} can become sufficiently large.

Relationship between the Gate Resistance and the Peak Recovery Current of and the Freewheel Diode and Diode Inrush Current

The following figure shows the stray inductance which always exists in the circuit.

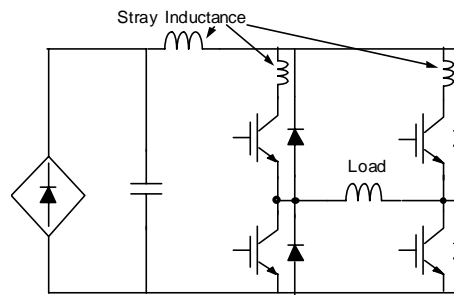


Figure 2.4 Figure Showing the Stray Inductance in the Circuit

The above circuit is simplified in the diagrams below to explain the peak recovery voltage of the freewheel diode.

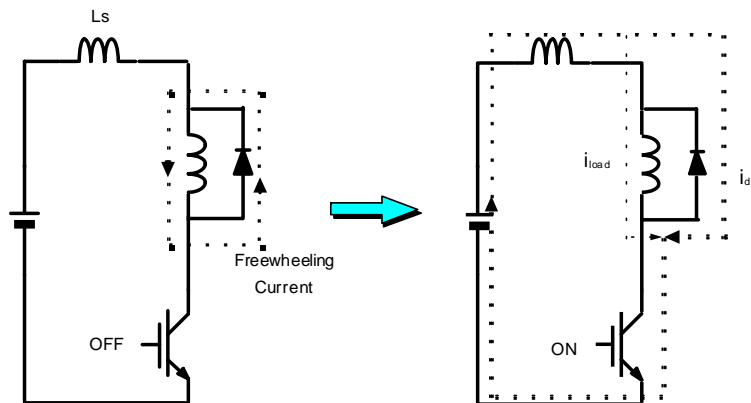


Figure 2.5 Figure Showing the Recovery Current Flow in the Diode

When an IGBT is turned on abruptly while the diode is operating in one way, an instantaneous current flows in the opposite direction through the diode until the diode PN junction voltage is recovered. This is shown in the figure above.

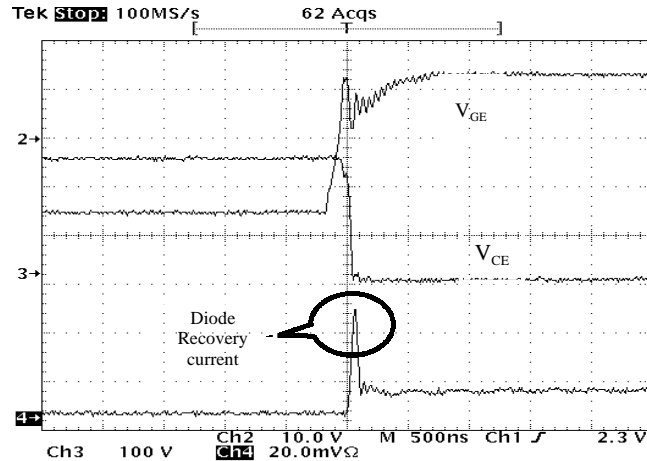


Figure 2.6 Figure Showing the Diode Recovery Current Flow ($R_{ON}=0[W]$, $L=48[mH]$)

Though the current amount is not large enough to destroy the IGBT, the instantaneous current slope becomes steep. This type of an abrupt slope generates a voltage of $L_S \times di_{do}/dt$ in the stray inductance in the circuit of Figure 2.5. This voltage resonates with the stray capacitance in the circuit to produce an oscillation similar to the V_{GE} waveform in Figure 2.6 or to cause EMI problems. If the gate resistance is increased at this time, the diode recovery current slope of di_{do}/dt reduces the occurrence of these phenomena, making them less frequent. Because the peak voltage, generated by the diode recovery current, is different depending on the stray inductance, it is very difficult to correctly calculate its value through an equation.

Hence, it would be better to determine its minimum value based on the gate resistance through repeated testing.

3. Design Technique of a Protection Circuit

Because an inverter is a circuit which delivers power, the entire circuit becomes damaged due to the large current that flows when accidents such as a short circuit occur. This can lead to a fire, which can be prevented with the insertion of a current protection circuit. Though general household electronic devices can block an over current or short circuit current through a current fuse or something similar, they do not protect the IGBT or similar semiconductor switching components. This is because they deteriorate faster than the time required by the fuse to cut off the current. The Fairchild IGBT must cut off the current within $1.5[\mu sec]$ after a short circuit has occurred for a product without short circuit protection measures, and within $10 [\mu sec]$ for a product with protection measures to protect the IGBT. This section reviews the method of designing a protection circuit which can safely protect the IGBT against an over-current or short circuit situation.

3.1 Current Sensing Method

Of the many methods for sensing the current flow in IGBTs (not the sense IGBT for current sensing), a detection resistance inserted at the DC link terminal is the most widely used method, as shown in the figure below.

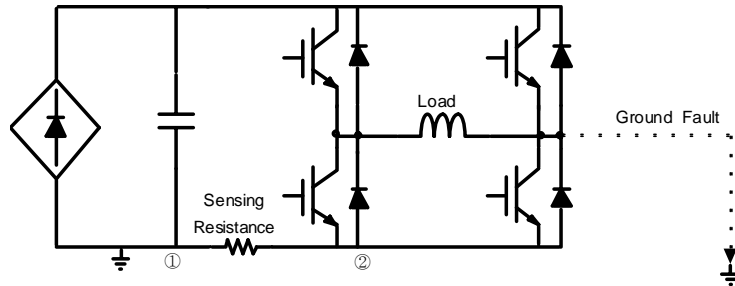


Figure 3.1 Current Sensing Resistance Inserted at the DC Link Terminal

As shown in the above figure, the sensing resistance must be inserted after the smoothing capacitor. Because power is consumed through this resistance even at normal conditions, it cannot be used in the inverters which use large amounts of current. It is used widely in common small capacity inverters. The resistance insertion method senses the entire current at one place and thus, one protection circuit can protect the entire IGBT. Though this feature, which reduces the inverter production cost, is an advantage, the fact that the protection circuit can fail when a large current ground accident occurs, in which the current does not flow through the resistance as depicted in figure 3.1, is a disadvantage.

Furthermore, when there is large amount of current flowing, a differential potential appears across the resistance due to the current. This increases the potential at (1) the ground shown in figure 3.1 and at (2) the emitter terminal of the lower IGBT and the gate drive circuit ground. Therefore, the gate drive circuit should be designed considering this increase in the potential. For example, if the potential at (2) increases 2V when using a gate drive IC with an input threshold of 2V, a voltage over 4V must be applied at the input to exceed the threshold voltage. For this reason, a protection circuit is inserted in all IGBT gate drive blocks in most large capacity inverters. By sensing each of the V_{CE} saturation voltage of the IGBT, the protection circuit operates individually when the V_{CE} saturation voltage exceeds a specific voltage.

The value of the sensing resistance inserted at the DC link terminal is selected according to the mechanism using the inverter. For example, a low inductance resistor with a capacity of about 0.2[W] is usually used for a 1~2[A] capacity inverter, and a low inductance resistor with a capacity of about 0.1[W] is used for a 3~4[A] capacity inverter. However, for inverters with capacities over 10[A], it is best not to use this method because accuracy falls for lower resistance levels. Noise, similar to the operating frequency, appears on the detection signal in normal inverter operation. In this case, the amplitude of noise is relatively large because the voltage across the sensing resistance is quite low. A low pass filter circuit should be added to the over-current detection circuit with a low detection level for noise immunity. The low pass filter is reviewed in Section 3.2. It has a close relationship with the operation of the over-current protection circuit.

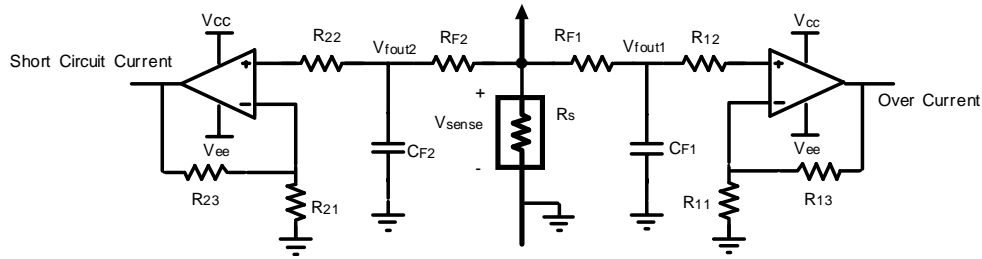


Figure 3.2 The Example Circuit that Amplifies the Detection Voltage

The relationship between the input voltage V_{SENSE} and output voltage V_{FOUT} of the low pass filter is presented in the following equation.

$$V_{FOUT} = \frac{\frac{1}{R_F \times C_F}}{S + \frac{1}{R_F \times C_F}} \times V_{SENSE} \quad (4)$$

The filter constant, $1/R_F C_F$, required for over-current sensing must be smaller than the filter constant, $1/R_F C_F$, required for short current detection. In other words, the filter response speed needed for short current detection must be fast.

The amplification gain of the amplifier and resistance calculation of R_{i2} ($i=1, 2$) is shown below.

$$V_{CO} = \frac{R_{i1} + R_\beta}{R_{i1}} \times V_{FOUT}, \quad R_{i2} = \frac{R_{i1} \times R_\beta}{R_{i1} + R_\beta}, \quad (i = 1, 2) \quad (5)$$

A non-inverting amplifier was used to amplify the input impedance. Therefore, the output of the amplifier V_{CO} is usually positive, but it can be negative when regenerating to the voltage source during freewheeling. If the output absolutely needs to be positive in such a case, a rectified circuit must be added at the output. There is no negative V_{CO} without the regenerative freewheeling to the source. A rectified circuit does not need to be considered in that case. Because the IGBT must be turned off within $10[\mu\text{sec}]$ after a short circuit, the gate cutoff signal must leave the filter input within $10[\mu\text{sec}]$. However, there are many instances when this $10[\mu\text{sec}]$ cannot be met due to the differences in the LPF design. In such instances, the detection must be done before the $10[\mu\text{sec}]$ by controlling the amplifier gain and comparator detection level. The filter design will be reviewed in detail in the actual inverter design in Section 5.

3.2 Over-Current Protection Circuit

There are many over-current protection methods depending on the mechanism to which the inverter is applied. This application note describes the design of a smoothly operating over-current protection circuit for an inverter applied to a BLDC motor. The diagram of the over-current protection circuit is shown below.

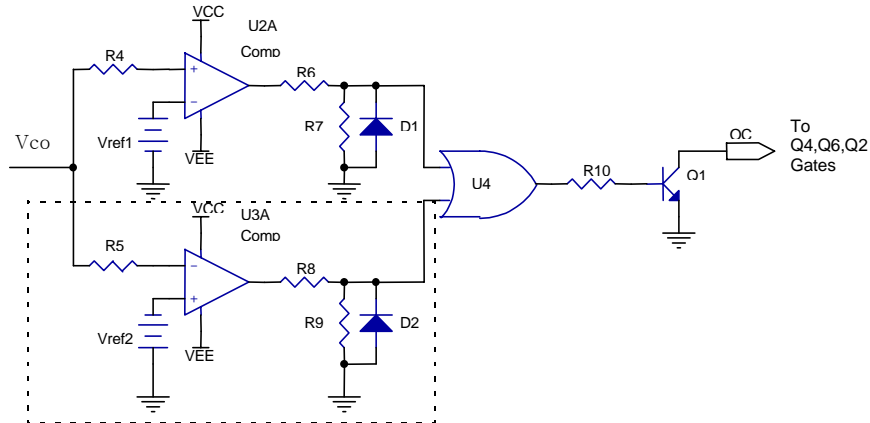


Figure 3.3 Over-current Protection Circuit

When a specific level of over-current is detected initially, the above over-current protection circuit is designed to physically cutoff the bottom gate, but recover the gate completely after a specific delay time. Furthermore, it was designed with the consideration of the negative current during the regenerative braking of the motor and designed to have diodes (D1, D2) inserted at the comparator output terminal to block the comparator output from becoming negative. When an over-current is detected, it operates from the OR gate through R_{10} to drive the TR. The base current, i_B , is determined based on the value of resistance R_{10} , and the maximum current.

$I = H_{FE} \times i_B$ flows through TR. At this time, the potential of the IGBT gate is determined based on the voltage of the gate drive IC output, the value of the resistance, R_{10} , and the value of the turn off resistance, R_{OFF} . The following figure shows the relationship between the IGBT emitter gate voltage V_{GE} , and the maximum current that can flow in the IGBT.

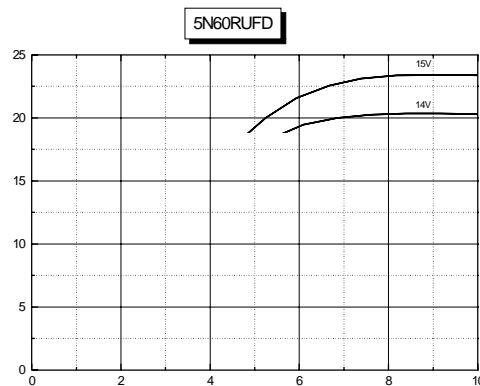


Figure 3.4.1 The Relationship between V_{GE} and the Maximum Current that can flow in the IGBT (5N60RUFD)

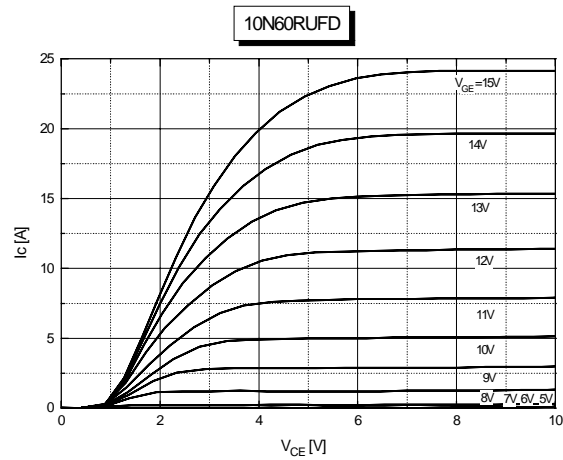


Figure 3.4.2 The Relationship between V_{GE} and the Maximum Current that can flow in the IGBT (10N60RUFD)

As shown in the figure above, if the gate voltage is not dropped completely to 0[V] but to an appropriate level of (6-7[V]), the IGBT current is reduced to 2-3[A]. Furthermore, if the cutoff TR gate resistance R10 is selected appropriately, a comparatively smooth cutoff waveform can be obtained. The following figure shows the operation of the protection circuit when an over-current flows in the inverter.

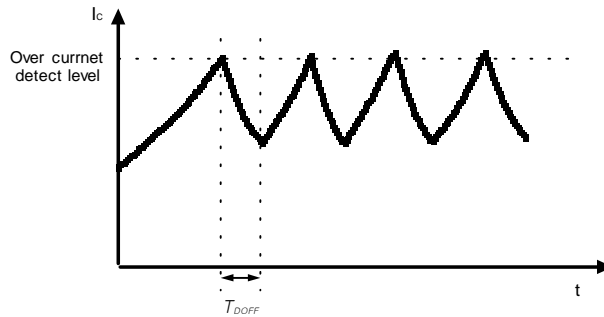


Figure 3.5 Over-current Protection Circuit Operation

The turn off interval T_{DOFF} shown in the above figure is the most important constant in the actual operation of the over-current protection circuit. If T_{DOFF} is too short, high speed switching can occur during an over-current situation, and the IGBT can be thermally destroyed. If it is too long, an interval where the current is discontinuous can arise, and this enlarges the current ripple which appears as the motor torque ripple.

Hence, T_{DOFF} is determined depending on the current reduction slope at turn off. Most motors have inductive elements inside, and all inverter circuits have freewheeling paths to make the current flow continuously in these inductive elements. The current reduction slope at turn off varies with the size of the inductance in the motor and with the freewheeling method. There are two freewheeling methods. One method turns off both the top and lower terminals of the IGBT. The other method turns off either the top or bottom terminal. The following figure shows the current path of the former method, which turns off both the top and bottom IGBT.

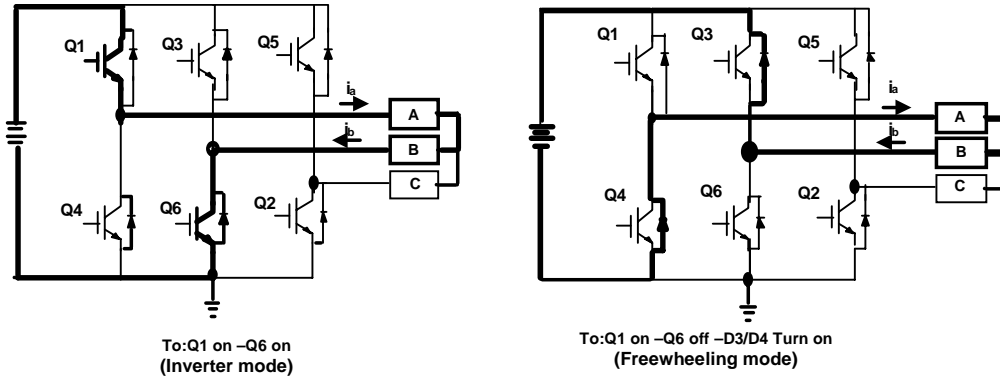


Figure 3.6 The Current Path of the Freewheeling Method which turns off both the top and bottom parts of the IGBT

As shown in Fig. 3.6, the freewheeling current flows in reverse through the diode opposite to the IGBT, which was just turned on in the same arms. The equation for freewheeling in the circuit is shown below:

$$L_a \times \frac{di_f}{dt} + R_a \times i_f = -E \quad (6)$$

Here, L_a is sum of all the inductance; R_a is the sum of all the resistances in the circuit; i_f is the freewheeling current; and E is the power source voltage. If the initial current when the turn off starts is i_o , the freewheeling current can be obtained from the following equation.

$$i_f(t) = i_o \times e^{-\frac{R_a}{L_a} \times t} - \frac{E}{R} \times \left(1 \times e^{-\frac{R_a}{L_a} \times t} \right), \quad i_f(t) \geq 0 \quad (7)$$

If we note the direction of the freewheeling current as +, the current continues to reduce until it becomes zero, and when it becomes negative the diode stops the current. The fact that the current is reduced quickly as the power source voltage E increases is described in the above equation. The following figure graphs the current when the power voltage is 200[V], the resistance is 5[Ω], the inductive components are rated at 300[mH] and the initial current is 20[A].

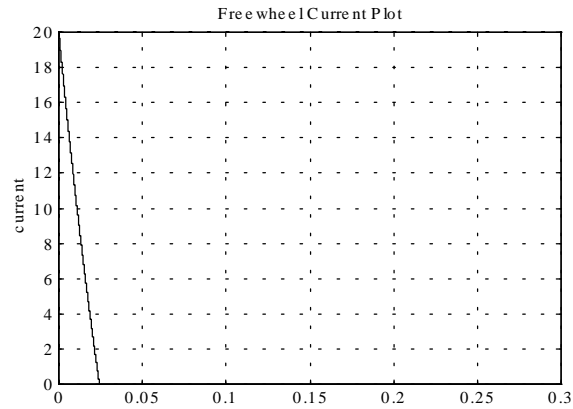


Figure 3.7 Waveform of the Freewheeling Current of the Method which turns off Both the Top and Bottom Parts of the IGBT

The figure above shows the abrupt drop of the current.

The figure below shows the freewheeling path when only the bottom part of the IGBT is turned off.

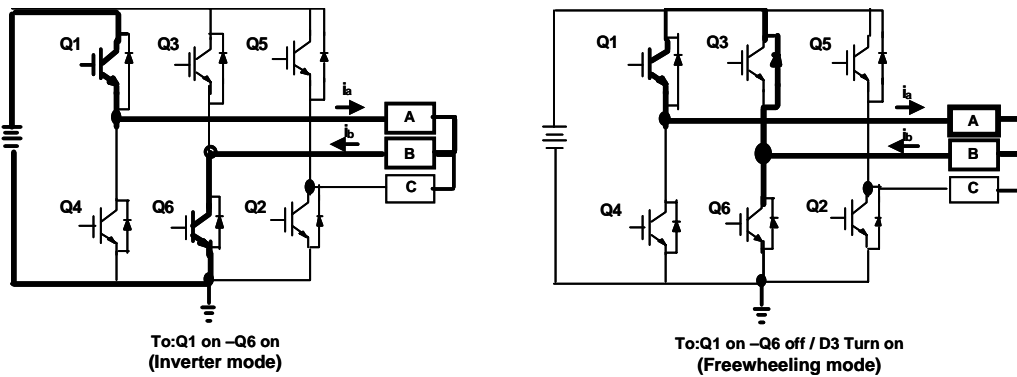


Figure 3.8 Freewheeling Current Path of the Method which turns off only the Bottom Part of the IGBT

The freewheeling current flows through the diode opposite to the bottom part of the IGBT which was on, and the top part of the IGBT. The equation for the freewheeling in the circuit is presented below.

$$L_a \times \frac{di_f}{dt} + R_a \times i_f = 0 \quad (8)$$

If the initial current at the start of the turn off is i_o , the current can be obtained as follows:

$$i_f(t) = i_o \times e^{-\frac{R_a}{L_a} \times t} \quad (9)$$

The current waveform of a circuit with the above freewheeling path and coefficient in Figure 3.7 is presented below.

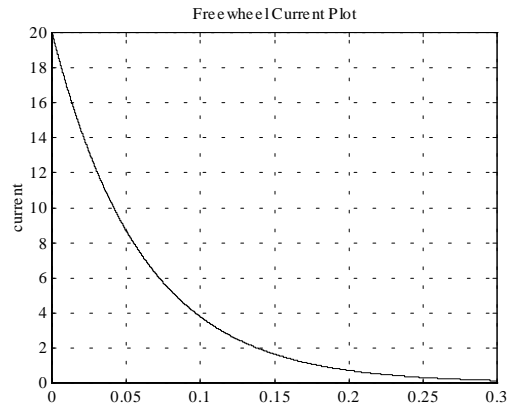


Figure 3.9 Freewheeling Current Waveform of the Method which turns off the Entire Bottom Part of the IGBT

Comparison of Figure 3.7 with 3.8 reveals that turning off both the top and bottom brings about a much faster decrease. TDOFF must be shortened to reduce the ripple of the current with the fast decrease. But switching the component too quickly can heat the component severely when the current is becoming an over-current, and has a negative effect on the component's dynamic characteristics. Hence, this application note recommends the method which reduces the current by switching only the bottom part of the IGBT.

3.3 Short Circuit Current Protection Circuit

When an accident such as an inverter Arm Short or Shoot Through is generated, the current suddenly increases at a sharp slope, saturating the IGBT with the maximum allowable current as shown in Figure 3.4. The Fairchild IGBT (Short Circuit Rated IGBT) which is designed for short circuit currents, can withstand such an accident for 10[μsec]. If the IGBT is turned off within this time, the IGBT is protected from damage. In a 5 [A] IGBT the short circuit current protection normally operates around 10[A]. If the current increases gradually, the over-current protection circuit set at 7[A] starts to operate first. This prevents the current from reaching the specified value for the short circuit current. However, because the current increases with a sharp slope in a short circuit, the short circuit current protection circuit operates before the LPF output of the over-current detection circuit, with a relatively slow response speed, initiates the over-current protection circuit. A current that can destroy the IGBT instantly flows through the circuit when there is a short circuit current. Therefore, if it cuts off the current instantaneously and repeats the operation like the over-current protection circuit, the IGBT heats up instantaneously. This results in a thermal latch-up state. Even if the IGBT cuts off the gate signal, working like a thyristor in this situation, the IGBT is unable to turn off and is damaged. Hence, the short circuit current protection must cut off the gate when a short circuit is detected until the reset signal enters from outside.

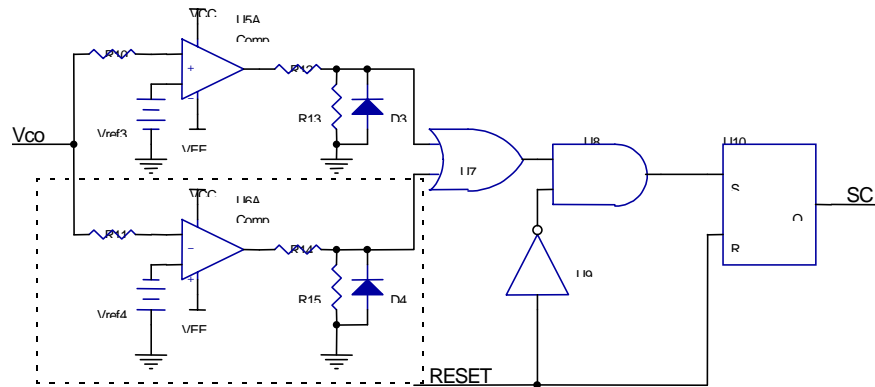


Figure 3.10 Short Circuit Current Protection Circuit

The RS F/F operation used as the latch circuit in the above circuit is presented in the following table.

R	S	Q_n
0	0	Q_{n-1}
0	1	1
1	0	0
1	1	0

Table 3.1 F/F Operation Truth Table

The turn off speed must be considered in the short circuit current protection circuit. As mentioned in section 2.2, the current slope generates the circuit surge voltage depending on the stray inductance in the circuit. Unlike the slope of the diode recovery current which can not generate a large voltage, the short circuit current falls from a large current value to 0. For this reason, if the gate voltage is eliminated suddenly at short circuit, the current will have a large slope. If the stray inductance in the circuit is large, a high voltage is generated. This generated voltage will instantaneously exceed the breakdown voltage of IGBT depending on the circumstances and will destroy the IGBT. The two types of short circuits are explained below.

Type I: Short Circuit that occurs when the IGBT is on-state and the current is flowing

This is a situation when a short circuit occurs for any reason while a current is flowing in IGBT. At this time, the IGBT is on-state and the voltage across the IGBT collector and emitter is maintained at about 2[V], as shown in the figure below. If a short circuit occurs, the current abruptly increases to reach the maximum value. If the gate is cutoff at this time, V_{CE} increases and becomes the same as the power source voltage while the current gradually decreases.

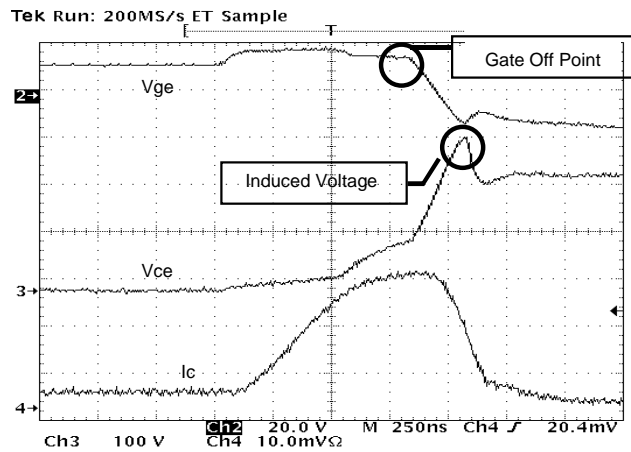


Figure 3.11 Type I Short Circuit

IGBT: SGH30N60RUFD, DC link voltage: 240[V], Peak Current: 140[A],
Stray Inductance: 150[nH]

Type II: The turn on signal is applied to the gate when the IGBT is off and a short circuit has occurred in the load

In this case the V_{CE} is the same as the power source voltage because the IGBT is off initially. Because the current starts to flow with a sharp slope, the current reaches its maximum before the voltage across the IGBT drops, as shown in the figure below.

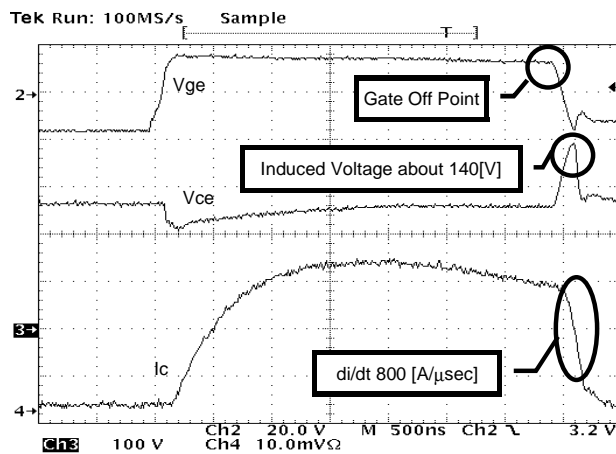


Figure 3.12 Type II Short Circuit

IGBT: SGH30N60RUFD, DC link voltage: 240[V], Peak Current: 140[A],
Stray Inductance: 150[nH]

If the current is cutoff in this situation and a surge voltage is generated, the voltage across the component increases sharply because the V_{CE} is already large. If this voltage across the component exceeds the breakdown voltage, it will destroy the IGBT. If the IGBT is destroyed, the gate, emitter and collector all become short circuited and a large current leaks into the drive circuit through the gate. This destroys the gate drive IC and damages its connected power source. Hence, the inverter should be designed for the type II accident. Because the design of the inverter with stray inductance is dealt with in Section 5, the rules for designing a low turn off slope for the short circuit current will be explained here.

A large capacity inverter cuts off the gate drive voltage by dividing it into 2-step potentials. When turning off the short circuit current, it drops the gate voltage at a slope lower than normal to prevent sudden current changes. However, because the short circuit current itself is small in a small capacity inverter, the slope is also small. Therefore, the turn off slope is controlled by appropriately controlling the gate turn off resistance rather than through this type of gate operation. Essentially, if the gate turn off resistance is made large, the peak current increases because the charge at the gate can not be quickly extracted, and the slope of the decreasing current decreases. If the resistance is made small, the peak current can be reduced, but the current slope increases. The Fairchild IGBT, which takes into consideration the short circuit current, can withstand up to 10 [μ sec]. The gate resistance does not need to be decreased to reduce the peak current because it is limited by the inherent characteristics of the IGBT. Hence, if the stray inductance in the circuit is large, a comparatively large turn off resistance should be selected, and if small, a small resistance should be selected.

The following table summarizes the gate resistance selection method of Section 2, and the rules for deciding on the gate resistance presented in this paragraph.

Condition	Increase R_{on}	Condition	Increase R_{off}
Turn-on di/dt	Decrease	Turn-off Loss	Limited Increase
Turn-off Loss	Increase	Turn-off Delay	Increase
Turn-on Time	Increase	Voltage Rise Time	Increase
Diode Recovery Current	Decrease	Current Fall Time	Limited Increase
Diode Recovery Voltage	Decrease	S/C Time	Decrease
EMI	Decrease	S/C Current Peak	Increase
S/C Time	Not Applicable	S/C Voltage Peak	Decrease
S/C Peak	Not Applicable	dv/dt Sensitivity	Increase

Table 3. 2 IGBT Operation according to the gate resistance

4. Usage of the Gate Drive IC with a Boot Strap Circuit

A bootstrap circuit uses its own signals etc. to operate the circuit. It is also a circuit which controls the impedance by applying a positive feedback in the general OP amp circuit. In this application note, it supplies the IC power to drive the top IGBT gate by using a diode, capacitor and IGBT switching without making a separate power source on the outside.

4.1 Principle of the Bootstrap Circuit

The following figure represents a bootstrap circuit which uses a diode and a capacitor.

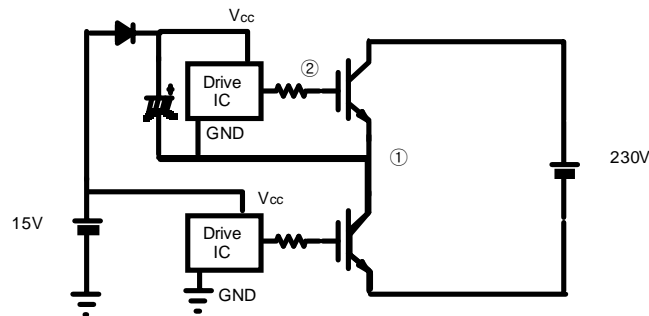


Figure 4.1 An example of a Bootstrap Circuit

When the IGBT arm as shown in Figure 4.1 is driven, the potential of the inverter output (1) varies from the ground voltage to the DC link voltage 230[V]. Essentially, this means that if the upper IGBT turns on and the lower IGBT turns off, the potential at (1) increases to 230[V], but if the lower IGBT turns on and the upper IGBT turns off, the potential at (1), falls to the ground potential. However, to turn on the upper IGBT, the potential at (2) must be 15[V] higher than the potential at (1). The potential difference between (1) and (2) must be maintained above 15[V], regardless of the absolute potential at (1). For this, the bootstrap circuit (Level Shifter) is used. The bootstrap circuit uses the switching of the lower IGBT to supply 15V to the upper gate drive IC through the diode and capacitor.

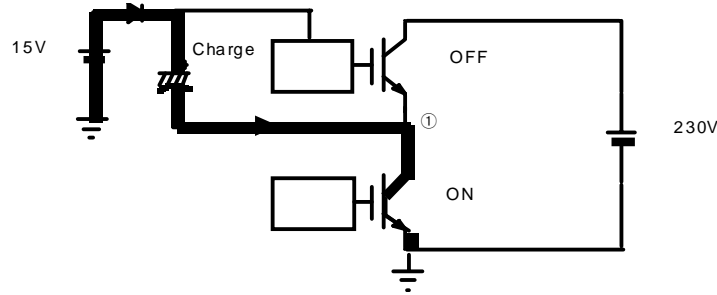


Figure 4.2.1 Bootstrap Circuit Operation (Capacitor Charging Mode)

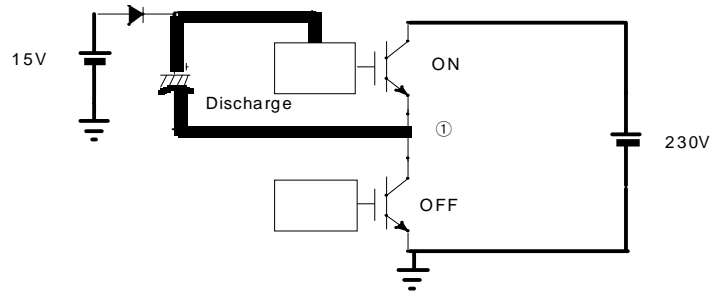


Figure 4.2.2 Bootstrap Circuit Operation (Power Supply Mode)

In Figure 4.2.1, the lower IGBT turns on first and the potential at (1) drops to ground. This turns on the boot strap diode in one direction to charge the capacitor to 15[V]. In Figure 4.2.2, the lower IGBT turns off and the upper IC operates with the voltage charged in previous step as shown in the operation in figure 4.2.1. This turns on the upper IGBT and, as a result, the potential at (1) becomes 230[V]. Then the diode turns off in the reverse direction and the capacitor supplies the power to keep the top part of the gate on.

As shown in Figures 4.2.1 and 4.2.2, the gate drive system with the bootstrap configuration must turn on the bottom IGBT first, and then turn on the upper IGBT to charge the energy to drive the top gate drive in the capacitor.

4.2 Bootstrap Circuit Capacitor Value Determination Method

In a bootstrap circuit, the capacitor supplies the gate energy to turn on the upper IGBT. Therefore, a comparatively small capacitor can be used with higher frequency because the charging frequency of the capacitor increases as much as the the top and bottom alternate switching speed. On the other hand, if the switching speed is slow, a larger capacitor must be used. The size of this type of a capacitor is closely related to the IGBT switching frequency and the voltage applied to the capacitor. The equation below calculates the minimum charge the bootstrap capacitor must supply.

$$Q_{bs} = 2Q + [I_{qbs(max)} + I_{cbs(leak)} + I_{dbs(leak)} + I_{c(max)}] \times t_{on} \quad (10)$$

where,

Q_g : Charge amount of the gate at the top part of the IGBT

t_{on} : Turn on time

$I_{qbs(max)}$: Current required to keep the IGBT on

$I_{cbs(leak)}$: Capacitor leakage current

$I_{dbs(leak)}$: Diode reverse leakage current

$I_{c(max)}$: Maximum current

The bootstrap capacitor capacity selected should be such that it supplies sufficient charge to the upper IGBT even if IGBT keep their on-state relatively for a long time. The capacitance of the bootstrap capacitor is calculated as follows:

$$C \geq \frac{20Q_{bs}}{V_{CC} - V_f - V_{IS} - V_{MIN}} \quad (11)$$

where,

V_f : Bootstrap diode forward voltage drop

V_{IS} : The lower IGBT forward voltage drop

V_{MIN} : Minimum voltage required to turn on the IGBT

In the Fairchild IGBT, the leakage current between the gate and source or the reverse leakage current of the diode is lower than 100 [nA] and can be ignored. Furthermore, the following equation calculates only the charge to turn on the IGBT and the current to keep the IGBT on.

$$C \geq \frac{2(2Q_g + I_{qbs} \times t_{on} + i_{c(max)})}{V_{CC} - V_f - V_{IS} - V_{MIN}} \quad (12)$$

If the recommended minimum capacitance calculated in equation (12) is used in an actual application circuit to keep the IGBT on, the generated voltage ripple has a negative effect on the inverter operation. Hence, the higher the capacitance, the better it is. However, a capacitor of about 15~20 times the value calculated in equation (12) can be selected.

4.3 Bootstrap Circuit Diode Selection Method

When the upper IGBT is on, almost all the DC link voltage is applied across the bootstrap diode. Therefore, the breakdown voltage of the diode must at least exceed the minimum DC link voltage. It should also have fast reverse recovery speed to block the emission of the capacitor charge. A component which minimizes the diode reverse leakage current must be chosen for an application circuit with a comparatively long turn on time. The absolute rating of the diode, which satisfies these characteristics is presented in the following equation.

$$V_{RMS} \geq \text{DC Link voltage} \quad (13)$$

$$t_{m(MAX)} \leq 100[\text{ns}] \text{ (typically)}$$

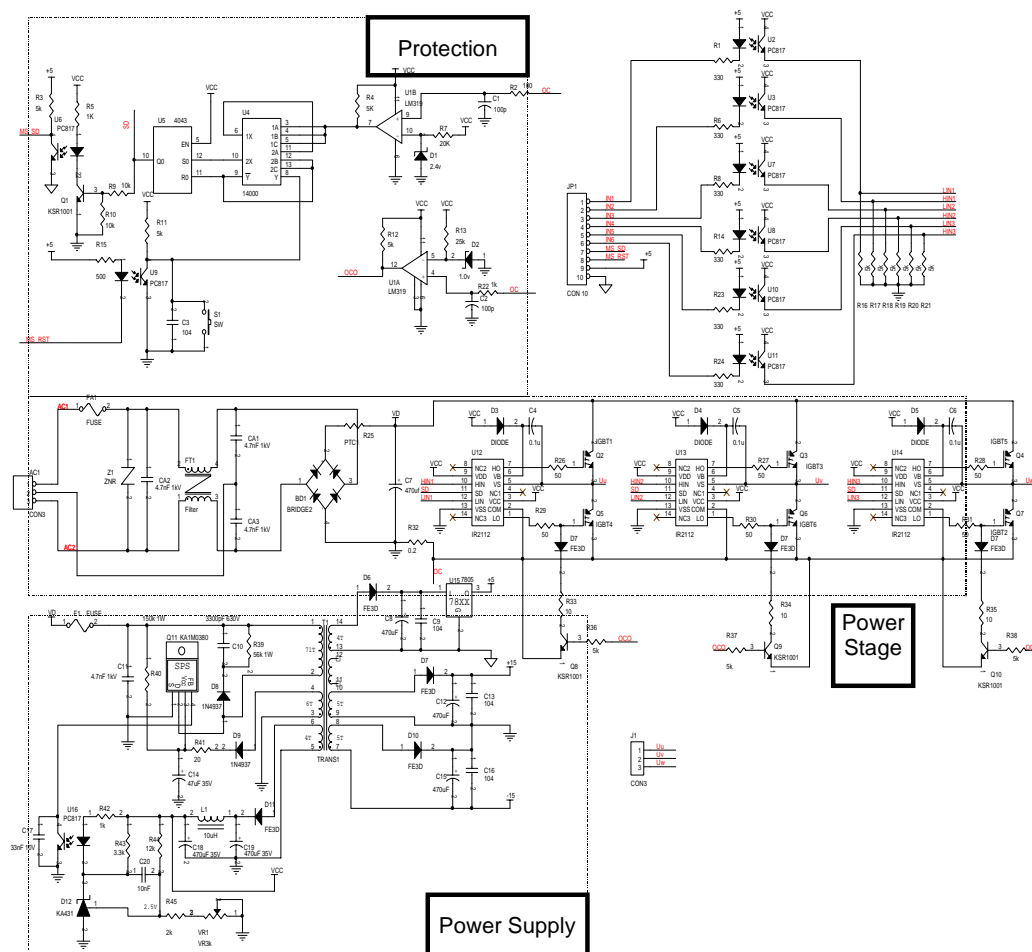
$$I_F = Q_{bs} \times f, \text{ where } f \text{ is the operating frequency}$$

5. An Example of an Inverter design with SGP5N60RUF

A design for a three-phase inverter with short-circuit rated COPAK IGBT with the rating of 600V 5A in motor applications is described in this chapter.

5.1 Circuit Diagram of the Entire System

The circuit diagram of the actual design of the system is shown as follows:



The inverter design can be divided into the power supply block, power drive block and the protection circuit block. Firstly, the power supply block makes the isolated power source with SMPS(Switch Mode Power Supply) and provides its power to the inverter circuit including gate drive ICs. In the diagram above, the power supply uses the SPS (Smart Power Switch), a Fairchild IC, appropriate for the SMPS. Generally, a large capacity three-phase inverter must have a power supply to supply power to 3 lower IGBTs and their surrounding circuits, and 3 independent power supplies to drive 3 upper IGBTs. However, in a small capacity inverter, one power supply can satisfy all the power needs by using a bootstrap circuit.

The gate drive in the inverter, herein, does not need a separate photo-coupler or similar level shift circuit. However, if a general gate drive is used, a photo-coupler or similar level shift circuit must be used to provide a signal to the upper gate drive.

5.2 Gate Resistance Calculation

It is assumed that the inverter operates with a 10[kHz] basic PWM frequency, 300[V] for the DC link voltage,

2[A] for operating current, 200[mA]/420[mA] for source/sink current for maximum drive capacity of the gate drive output used, and 15[V] for the maximum gate drive voltage. The stray inductance, which increased slightly due to the DC link current detection resistance in the actual inverter, was measured at 200[nH]. Considering the worst case conditions, the inverter did not use a low-inductance resistor for the detection resistor so the stray inductance became much larger than normal. Stray inductance is normally measured below 90[nH] in the normal inverter. The stray inductance in the circuit can be roughly estimated by measuring the short circuit current slope and the voltage across the device. The minimum gate resistance can be calculated based on equation (1) and the above conditions.

$$R_{ON}^{MIN} = \frac{15}{0.2} = 75[\Omega] \quad \text{and} \quad R_{OFF}^{MIN} = \frac{15}{0.42} = 35.71[\Omega] \quad (14)$$

The turn on and off resistances are both lower than 100[W] accounting for the turn on loss. The following maximum turn off current can be selected if the surge voltage due to the stray inductance is set to lower than 200[V], while taking into account that the IGBT has a blocking voltage of 600[V].

$$200 \times 10^{-9} \times \frac{dt}{di} \leq 200$$

$$\frac{dt}{di} \leq 1[A/ns] \quad (15)$$

The maximum turn off resistance based on the maximum voltage slope from equation (3) and test waveforms from the Fairchild IGBT data book is presented below.

$$R_{OFF} \leq \frac{5[V]}{13 \times 10^{-12} \times 3 \times 10^9[V/sec]} = 128[\Omega] \quad (16)$$

90[Ω] of turn on resistance and 75[Ω] of turn off resistance will be appropriate value according to the above calculation. In the actual circuit, the gate resistance was set to 90[Ω] because it was not separated into turn on and off resistances.

5.3 Parameter Calculation of the Current Detection LPF

The most noise from the power source is in the band of 10[kHz] because the basic frequency of the PWM is 10[kHz]. Therefore, the short circuit current detection filter or the over-current detection filter in figure 3.2 must have stop bands of less than 10[kHz]. If the filter pass band is too narrow, all the noise is eliminated, but the filter quick response characteristic falls, which has a negative effect on the circuit operation. If the -3[dB] frequency of the short circuit current detection circuit is changed to 1[kHz], the noise reduces from 10[kHz] to -20[dB] and can be effectively eliminated. However, it may not be possible to protect the IGBT if there is a short circuit current because the response is too slow. Therefore, to make the filter respond faster, its performance must be sacrificed. By changing the -3[dB] frequency from 10[kHz] to 6[kHz], the appropriate response and filter effect were obtained. The over-current detection circuit must be slower than the short circuit current filter speed, which is determined by the slope of the overall current. When the inverter is attached with a motor, an actual load, and tested, the slope of the current becomes about 2.3[A/ms] with only the lower part turned off. It takes about 3[ms] to drop from 7[A] to 0. To reduce the current ripple, the IGBT should be turned on again before the current becomes 0, and the filter frequency of -3[dB] should be set to 400[Hz]. The following equation can be derived using the results from above.

$$\frac{1}{R_{F1} \times C_{F1}} = 800\pi [\text{Rad/s}] \quad (17)$$

$$\frac{1}{R_{F2} \times C_{F2}} = 12000\pi [\text{Rad/s}] \quad (18)$$

If $C_{F1} = C_{F2} = 0.1[\mu\text{F}]$ is set, $R_{F1} \cong 4[\text{k}\Omega]$, $R_{F2} \cong 260[\Omega]$

5.4 Calculation of the Parameters for the Short Circuit Current Detection Circuit

10V is detected when the maximum short circuit current of 20[A] at the 15[V] gate voltage flows because a 0.2[Ω] detection resistance was used. The figure below shows the operating waveform of the short circuit current filter when the starting current of the short circuit current circuit operation is set to 10[A].

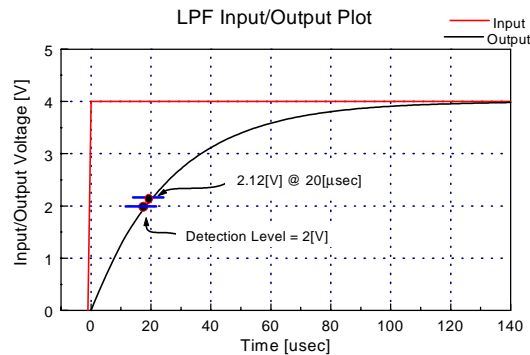


Figure 5.2 Input and Output Waveform of the LPF for Short-current Protection

The voltage across the detection resistance with a short circuit current increases as a step wave as shown in the figure above. The short circuit protection must start before the output voltage of the LPF, which is shown in Section 5.3, reaches approximately 2.12[V] if the maximum short circuit withstand time is set to 20[usec]. Furthermore, if the amplifier gain is set to 1 and the cutoff operation is executed when the amplifier output becomes 2[V], the IGBT can be protected without any damage. Even if the IGBT current was to increase slowly and exceed 10[A], the IGBT can be protected because the protection starts at 10[A].

5.5 Parameter Calculation for the Over-current Detection Circuit

Most over-currents in the inverter, which drives the motor, flow through the motor. Therefore, mostly depending on the load conditions, the slopes of the current change and can be calculated through the circuit equation or through direct testing. The rising slope of the load current is obtained through testing in this application note. The test consists of applying a single short pulse to the motor initially and examining the voltage and current waveforms. At this time, the motor must not be operating and the width of the applied pulse should be as small as possible, so that motor demagnetizing due to an large current does not occur. The maximum slope of the current obtained from testing is 5[A/msec]. Consequently, the slope of the voltage across the detection resistance is 1[V/msec], and the output waveform from the filter with this slope as input is shown in the figure below.

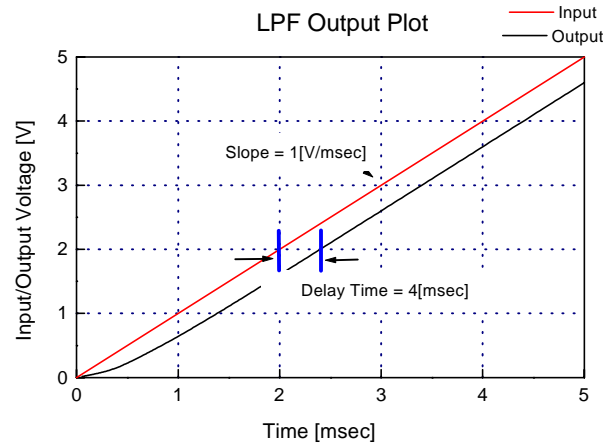


Figure 5.3 Input and Output Waveform of the LPF for Over-current Protection

The filter delay time is about 0.3[msec] so T_{DOFF} is set to about 0.3[msec]. However, T_{DOFF} becomes much longer because the gate voltage is not dropped to 0[V] immediately but maintained at an appropriate voltage of 5~6[V]. Consequently, we know that it is designed well because the IGBT turns on and off repeatedly at lower than 3[kHz] without straining the IGBT excessively. Therefore, if the amplifier gain is 3 times and the comparison level of the over-current comparator is set to 4.0[V], the current can be limited to around the load current of 7[A].

5.6 PCB Design Cautions

Though the circuit design is important in the inverter design, what is more important is the artwork which moves the circuit to the actual PCB. Though the circuit design may be perfect but if it was designed without giving special attention to the art work, the circuit could malfunction during actual operation due to an unforeseen noise. The artwork must be carefully designed to prevent the circuit from being damaged due to large amounts of power when the circuit malfunctions. There is not much theoretical information regarding artwork production, but it does require a lot of experience. General items for caution while producing the artwork and the steps that must be executed in inverter design are listed in this section.

- 1) If possible, separate the gate drive IC's GND from the general analog IC's GND. If this is not possible, do not mix these two lines and use them carelessly.
- 2) Good 0.1[F] capacitors must be attached in parallel between the IC power supply V_{CC} containing the gate drive IC and the GND.
- 3) The lower gate drive should be separated from the circuit power supply GND using a photo-coupler etc. If not, it should be directly connected to each of the IGBT emitters.
- 4) The closed loop design of the line must be avoided to the extent possible.
- 5) The high voltage point and the signal line should be kept far apart whenever possible. If this is difficult, they should be appropriately isolated.
- 6) The signal line with little current should be kept far apart from the power line. The IC power supply with this signal as input and output should be directly connected to the voltage source.
- 7) When winding the transformer which isolates the power source, the area where the windings overlap should be minimized in order to reduce the capacitance. If the secondary side of the transformer has capacitance, the surge current can pass through due to the sudden voltage change via the transformer.
- 8) The stray inductance should be minimized at the block connecting the DC link capacitor to the IGBT. Therefore, the connection line in this block should make a strong connection and not be bent over 45° .
- 9) When inserting the current detection resistor, the connection of the resistor legs should be short to minimize the stray inductance in this resistor.

The figure below outlines the items for caution when transferring the circuit diagram in Figure 5.1 to the PCB.

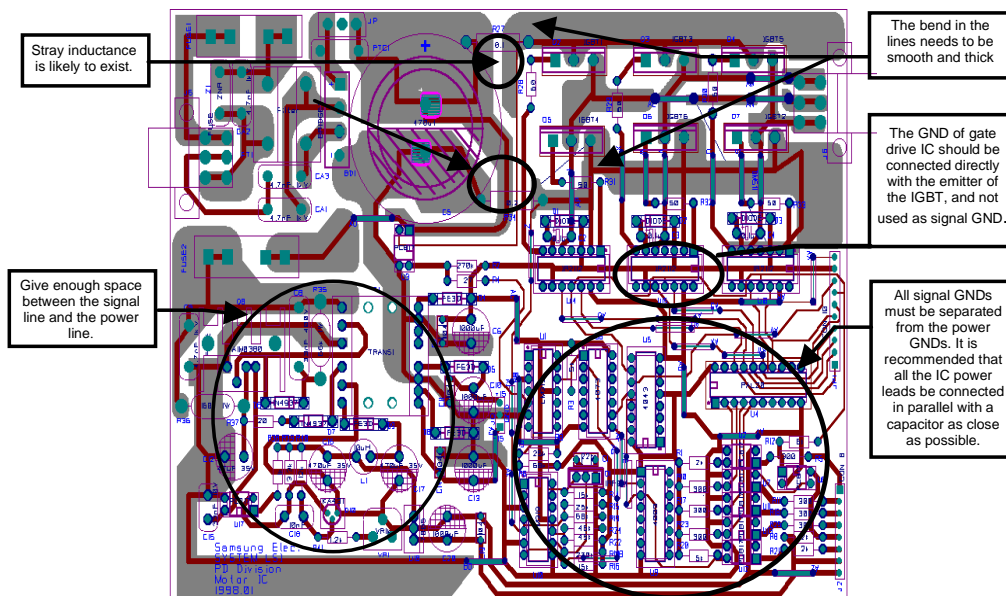


Figure 5.4 The PCB of an actual inverter circuit and the areas for caution

6. Conclusion

As IGBTs with the advantages of MOSFET and TR are becoming prevalent, they are being used in large and small capacity inverters. Fairchild IGBTs have the world's best features in many aspects. This application note details a method of designing an inverter at low cost by using the Fairchild IGBT as an output component. To promote the superior features of the Fairchild IGBT, which is not widely known, an inverter design appropriate for this IGBT's inherent features is presented. Furthermore, everything from design to artwork is covered in detail so that anyone can design the inverter using this application note.

Though this application note deals with a small capacity inverter design, the gate selection method in Section 2 or the protection circuit configuration method in Section 3, which is common to all inverter designs, can be used as valuable reference material.



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