AND8140/D

Current Limit Function

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APPLICATION NOTE

GENERAL DESCRIPTION

The ON Semiconductor family of hot swap devices uses a SENSEFET® for the power transistor. This is a very efficient method of sensing current as it does not require a low resistance, high power sense resistor. This circuit has two modes of operation, and will give a different current limit level in each mode. When the device encounters a short circuit condition, including initial charging of the input cap, the current will be limited to a predetermined level. This level is lower than the current limit level that will occur when the device encounters an overload condition. This application note will discuss these modes and give equations.

CIRCUIT DESCRIPTION

SENSEFET Operation

It is important to understand that a power MOSFET is made up of thousands of paralleled FETs or cells. By operating many cells in parallel very low values of R_{DSon} may be achieved.

A SENSEFET is made by separating a small portion of the cells from the main FET, which are used for the sense device. The ratio of cells from the main to sense FET determines the ratio of R_{DSon} of the two devices.

If all three terminals (gate, drain and source) are tied together, the two devices will share current based on the ratio of the cells. If a small resistor is added between the source of the sense FET and the source of the main FET (ground), this ratio will have a small error, but will still be close to the ratio of the cells.

By only allowing a fraction of the main current to flow in the sense FET, the current sensing resistor can be a more reasonable value in terms of resistance and power dissipation. For example, to sense a 100 mV signal from a 5.0 A current using a normal MOSFET would require a 20 mΩ, 1.5 W (using a factor of 3 derating for power) resistor. If a SENSEFET with a ratio of 1000:1 were used for the same current and sense voltage, a 20 Ω (R = 0.1 V/0.005 A) resistor is required that must dissipate 0.5 mW. This results in a significant cost savings for the current sense resistor.

Basic Circuit Operation

Figure 1 shows a simplified schematic of the current limit circuit. The main FET (Q_M) conducts the majority of the load current. The sense FET (Q_S) conducts only a small amount of current, but this current is normally related to the current flowing in Q_m by the ratio (k) of the cells. The sense current flows through R_S and generates a sense voltage. This voltage is used by the current limit amplifier to reduce the gate drive on the SENSEFET if the current, measured by V_S, becomes equal to the reference voltage to the amplifier.

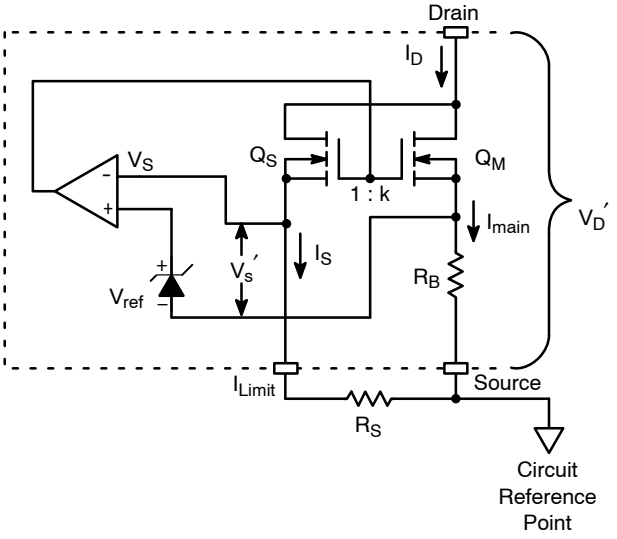

Figure 1. SENSEFET and Current Limit Circuit

R_B is the resistance of the bond wires in the source lead. Since there may be a significant amount of voltage dropped across this resistance relative to the sense reference voltage, and since the current sense reference voltage is referenced to the node between the source of the power FET and R_B, it must be taken into account.

Ideally, the current in Q_S is a fixed ratio of the current in Q_M. The theoretical relationship between Imain and V_S is:

$$V_S = \frac{I_{main}}{k} R_S$$

where k is the ratio of the main FET cells divided by the sense FET cells.

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Due to the sense resistor, this ratio has some variation to it. More importantly however, Isense only follows the ratio when there is adequate voltage at the drain to generate the correct sense voltage.

The following example illustrates this concept and is based on the circuit in Figure 1.

k (main : sense) = 1000 : 1
$R_{DSon(main)}$ = 40 mΩ
V_{ref} = 200 mV
I_D = 4.0 A
R_S = 50 Ω

According to the ratio, the sense current should be:

$$I_S = \frac{I_D}{1000} = \frac{4\ A}{1000} = 4\ mA$$

and the sense voltage would be:

$$V_S = 4\ mA \cdot 50\ \Omega = 200\ mV$$

which would be on the verge of current limit. However, the sense voltage must be less than the drain−source voltage, and if the FET is fully enhanced, the drain−source voltage is:

$$V_{DS} = 4\ A \cdot 0.04\ \Omega = 160\ mV$$

Under this condition, the sense voltage is the output of the voltage divider formed by the R_{DSon} of the sense FET and the sense resistor, R_S. This would be:

$$V_S = 160\ mV \frac{R_s}{R_{DSon(sense)} + R_s}$$

$$V_S = 160\ mV \frac{50\ \Omega}{(0.04\ \Omega \cdot 1000) + 50\ \Omega}$$

$$V_S = 89\ mV$$

which is roughly half of the 160 mV that would be expected using the straight ratio equation. This is because there are two distinct modes of sensing current in a SENSEFET, depending on whether the main power FET is in its linear or saturated region of operation.

Linear Mode

The linear mode of operation is applicable when the hot swap unit is overloaded, i.e. at high current levels where the FET is still fully enhanced. In this mode of operation the available voltage from drain to source is based on the drain current and the R_{DSon} of the main FET. It should be understood that the R_{DSon} given in the data sheet includes the bond wire resistance, but they must shown separately in this model to properly evaluate this circuit. To evaluate the operation of this circuit, the following analysis applies:

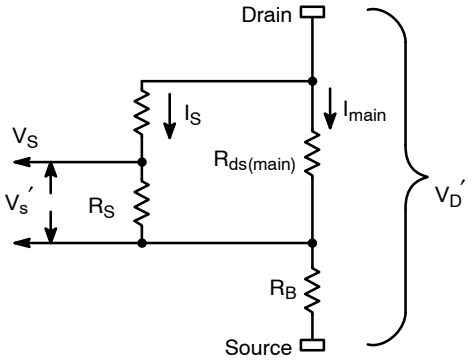

Figure 1. Linear (Overload) Mode Equivalent Circuit

The voltage drop across the drain−source terminal is:

$$V_D' = I_m \cdot \left(R_{ds(main)} + R_B\right) \quad \text{(eq. 1)}$$

Assuming $I_m \cong I_D$ the sense voltage V_s' is generated by the voltage divider consisting of $R_{ds(sense)}$ and R_S, less the drop across the bond wire, or:

$$V_s' = \left(V_D' - I_m \cdot R_B\right)\frac{R_S}{R_S + R_{ds(sense)}} \quad \text{(eq. 2)}$$

The resistance of the sense cells is the resistance of the main FET cells scaled by k, or:

$$R_{ds(sense)} = k \cdot R_{ds(main)}$$

Combining the above equations yields:

$$V_s' = \left[I_m \cdot \left(R_{ds(main)} + R_B\right) - I_m \cdot R_B\right]\frac{R_S}{R_S + \left(k \cdot R_{ds(main)}\right)} \quad \text{(eq. 3)}$$

$$V_s' = \left[I_m \cdot \left(R_{ds(main)}\right)\right]\frac{R_S}{R_S + k \cdot R_{ds(main)}}$$

For the current limit circuit to begin to function, V_s' must equal V_{ref}, so substituting V_{ref} into the above equation yields:

$$V_{ref} = \left[I_m \cdot \left(R_{ds(main)}\right)\right]\frac{R_S}{R_S + k \cdot R_{ds(main)}}$$

$$V_{ref} \cdot \left[R_S + k \cdot R_{ds(main)}\right] = I_m \cdot R_{ds(main)} \cdot R_S \quad \text{(eq. 4)}$$

Solving Equation 4 for I_m yields:

$$I_m = \frac{V_{ref} \cdot \left[R_S + k \cdot R_{ds(main)}\right]}{R_{ds(main)} \cdot R_S}$$

$R_{ds(on)}$ as listed on the data sheet is the resistance between the drain and source terminals, or $R_{ds(main)} + R_B$ so in terms of $R_{ds(on)}$, the main current is:

$$I_m = \frac{V_{ref} \cdot \left[R_S + k \cdot \left(R_{ds(on)} - R_B\right)\right]}{\left(R_{ds(on)} - R_B\right) \cdot R_S} \quad \text{(eq. 5)}$$

Solving Equation 4 in terms of R_S:

$$V_{ref} \cdot R_S + V_{ref} \cdot R_{ds(main)} = I_m \cdot R_{ds(main)} \cdot R_S$$

$$R_S\left(I_m \cdot R_{ds(main)} - V_{ref}\right) = V_{ref} \cdot k \cdot R_{ds(main)}$$

$$R_S = \frac{V_{ref} \cdot k \cdot R_{ds(main)}}{I_m \cdot R_{ds(main)} - V_{ref}}$$

Substituting $R_{ds(on)} - R_B$ for $R_{ds(main)}$ yields:

$$R_S = \frac{V_{ref} \cdot k \cdot \left(R_{ds(on)} - R_B\right)}{I_m \cdot \left(R_{ds(on)} - R_B\right) - V_{ref}} \quad \text{(eq. 6)}$$

Saturated Mode

In the saturated mode of operation, the FET is not fully enhanced as would be the case for a short circuit. This is the mode of operation at turn on of the hot swap device, since the load capacitance appears as a short circuit while it is charging. Essentially, this mode occurs any time there is a significant voltage (> 0.5 V) across the drain to source nodes of the FET. During a short circuit event, the drain to source voltage is simply the input voltage. When charging a capacitor, the drain to source voltage begins as the input voltage and then gradually reduces as the capacitor charges.

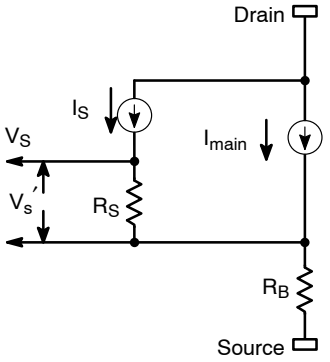

Figure 1. Linear (Overload) Mode Equivalent Circuit

In the saturated mode, there is ample drain−to−source voltage to allow the sense FET (Q_S) to operate on the ratio of the cells of the two FETs. Under this condition, the relationship of the sense voltage to drain current is:

$$I_S = \frac{I_m}{k} \quad \text{(eq. 7)}$$

$$V_S' = I_S \cdot R_S - I_m \cdot R_B \quad \text{(eq. 8)}$$

$$V_S' = \frac{I_m}{k} \cdot R_S - I_m \cdot R_B$$

$$V_S' = I_m\left(\frac{R_S}{k} - R_B\right) \quad \text{(eq. 9)}$$

Since V_{ref} is equal to V_s‘ at the point when the current limit circuit becomes active, we can solve for I_m:

$$V_{ref} = I_m \frac{R_S - k \cdot R_B}{k}$$

$$I_m = \frac{V_{ref} \cdot k}{R_S - (k \cdot R_s)} \quad \text{(eq. 10)}$$

Or, solving Equation 9 for R_S the equation becomes:

$$R_S = k \cdot \left[\frac{V_{ref}}{I_m} + R_B\right] \quad \text{(eq. 11)}$$

Short Circuit Current Limit Equation

Equation 11 describes the relationship between the short circuit current and the sense resistor, which can be seen in Figures 2 and 3.

Characterization of Current Limit Circuit

These two equations (Equations 6 and 11) can be used to calculate the current limit levels under the two conditions described. This same data is taken empirically for each device and presented in the data sheet.

It is recommended that the curves from the data sheet be used when determining biasing components for a device, since this data takes into account secondary effects that are not included in this analysis.

The data in Figures 2 and 3 shows both the empirical data and the calculated data for the NIS5101, hot swap device. The calculated graph uses Equations 6 and 11 with the following variables:

k = 1000
V_S = 70 mV
R_B = 3.0 mΩ
R_{DSon} = 38 mΩ

It can be seen from these charts that there are some differences between the calculated and empirical data, but in general there is reasonable agreement between the two.

The overload current level in Figure 3 reaches an asymptote. It is at a level of about 2.4 A at 1.0 kΩ and decreases slightly from there. This level can be determined by the equation:

$$I_{minOL} = \frac{V_{ref}}{R_{DSon}}$$

which in this case is:

$$I_{min\,OL} = \frac{90\ mV}{41\ m\Omega} = 2.2\ A$$

which will be the final value for very high values of the current limit resistor.

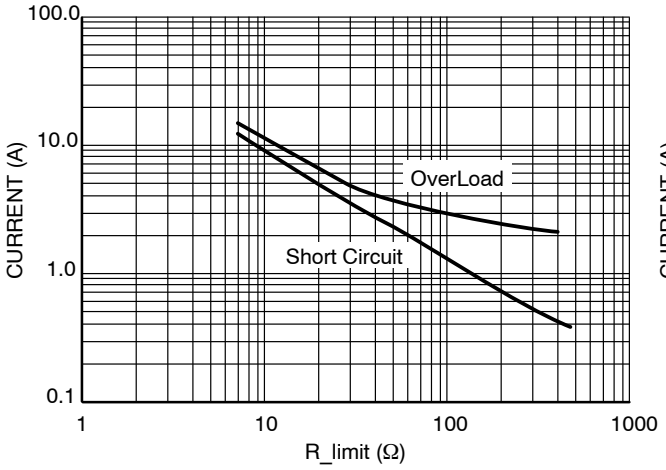

Figure 2. Empirical Data for NIS5101 Current Limit Circuit

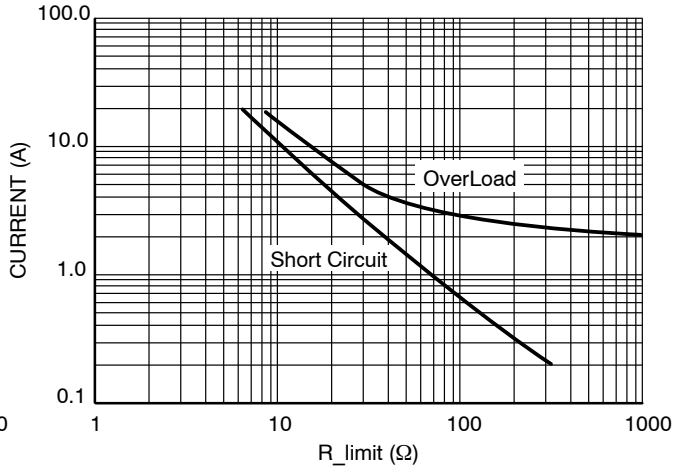

Figure 3. Calculated Data for NIS5101 Current Limit Circuit

Thermal Effects

It is helpful to understand the thermal implications of this circuit. The reference voltage is temperature compensated and will vary only slightly over temperature, however the on resistance of the FET is much more dependant on temperature.

Figure 4 shows the effects of temperature on the on resistance for a 40 mΩ. 100 V FET, similar to the one used in the NIS5101.

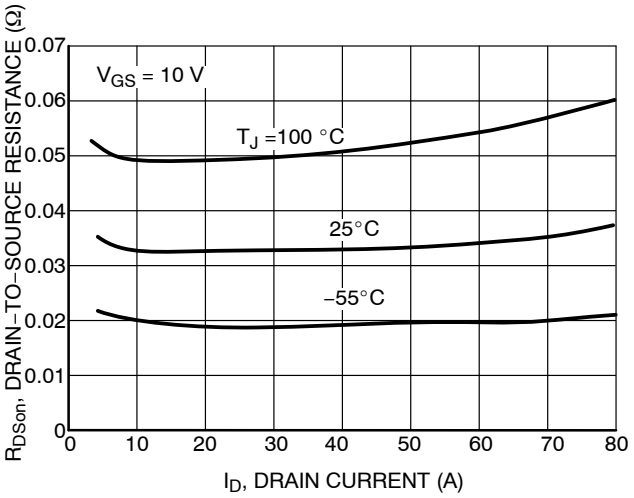

Figure 4. On−Resistance vs. Drain Current and Temperature

The change in on resistance overtemperature has minimal effect on the short circuit current limit. This is due to the fact that the short circuit current equation (eq. 10) has no R_{DSon} term in it although the bond wire resistance R_b is included and does cause a minor shift at high currents.

Figure 5 shows an NIS5101 in current limit using a 20 Ω current limit resistor and charging a 5200 μF capacitor. It can be seen that the current is very flat until the thermal shutdown point is reached at which time the current goes to zero. The current pulse begins with the die temperature at 25°C and shuts down when it reaches 130°C. Over this range of temperatures the short circuit current only changes 6%.

The overload current is more dependant on the R_{DSon} of the FET as well as the bond wire resistance and therefore will vary more with temperature. The temperature changes for the R_{DSon} of the FET can be approximated from the data in Figure 4. This information is used, along with the change in resistance of the bond wires to calculate the data in Figure 6.

The bond wires are aluminum and have a resistive temperature coefficient of 0.0039%/°C. The change in bond wire resistance from 25°C to 100°C is:

$$R(t) = R_{25}\,[1 + 0.00390(t - 25°C)]$$

$$0.004\ \Omega\,[1 + 0.00390(100°C - 25°C)] = 0.0052\ \Omega$$

and the change in R_{DSon} over the same temperature range is 53% from Figure 4.

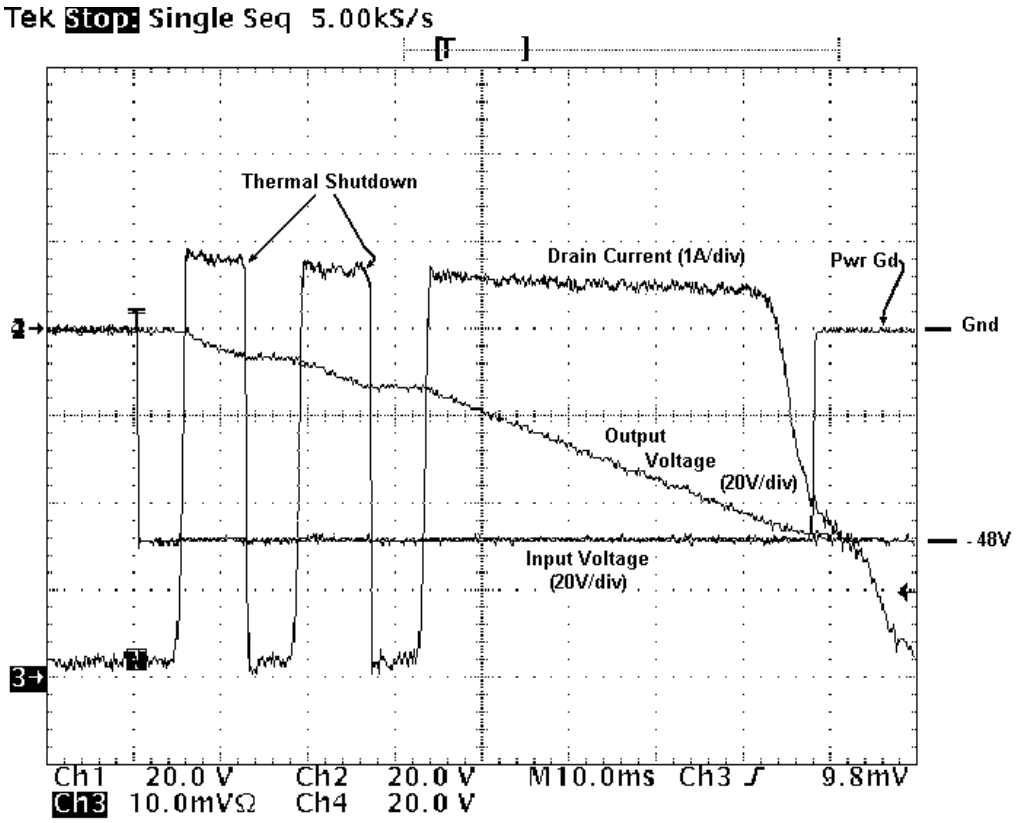

Figure 5. Short Circuit Current Limit

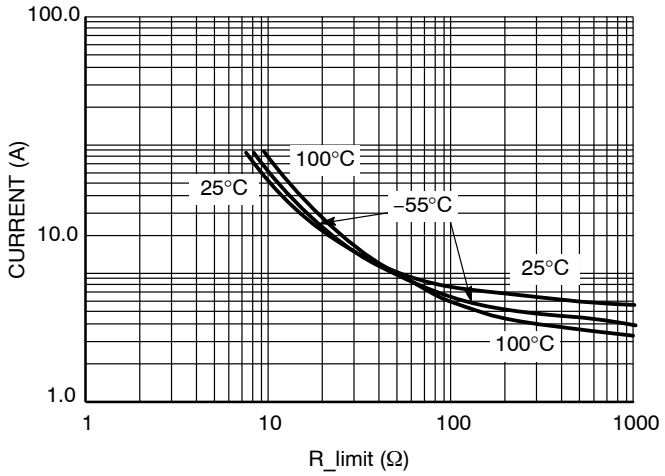

Figure 6. Calculated Data for Overload Limit for NIS5101 Overtemperature

Table 1. BASIC PARAMETERS

	k	R_B	$R_{DS(on)}$ Typ	V_{ref}
NIS5102	1400	0.3 mΩ	15 mΩ	70 mV
NIS5112	1000	0.7 mΩ	25 mΩ	80 mV

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