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AN-7012

FPF2100/7 Evaluation Board User's Guide

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AN-7012

FPF2100/7 Evaluation Board User's Guide

Evaluation Board Description

The FPF2100/7 board is an Evaluation Module (EVM) for the Fairchild Semiconductor FPF2100/1/2/3/4/5/6/7 smart load switches family. The FPF2100/7 family contains a 0.125Ω P-channel MOSFET with controlled turn-on, fast turn-off, thermal shutdown, under voltage lock out, and current limit. The current limit is guaranteed for 200 mA for the FPF2100/1/2/3 and 400 mA for the FPF2104/5/6/7. The operating voltage range is 1.8V to 5.5V. The EVM board provides access for monitoring all pins, and simulates the fault conditions as they might occur in a real application. This is accomplished by changing the states of the ON pin, input voltage, and output current and voltage. See Figure 1 page 2, for a detailed view of the board.

Current-Limit

The output current can be sensed with a current probe by removing the R3 shunt and soldering a loop across it. The FPF2100/7 EVM board has a nominal load in normal operation. By momentarily pushing the SW1 switch the load switch will be put in an overcurrent condition. In addition, the overcurrent condition may be triggered by an external signal through the external over-current terminal (TP3). The three load conditions are as follows:

- Nominal load: Normal operation with $R_1 = 500\Omega$ and $C_1 = 0.1\mu\text{F}$ load.
- Moderate overcurrent: Output is loaded with a 2.2Ω resistor (J2 in position 2).
- Hard short: Output is connected directly to ground (J2 in position 1).

Extra space has been provided on the board next to R1 and C1 for the user to mount any desired load for further experiments.

Monitoring the FLAGB

The status of the FLAGB pin can be monitored via TP1 either by probing directly the FLAGB pin or by lighting a small LED. For this purpose J3 needs to be set as shown in Figure 1. For parts without Auto-Restart the LED stays lit in current limit conditions until the SW2 switch is toggled. For parts with Auto-Restart the LED will light only as long as the pushbutton switch (SW1) is being held down.

ON Pin

The status of the ON pin can be monitored through TP2. Referring to the part number and test conditions, three mechanisms have been employed to change the ON pin condition:

- Using SW2 for manual ON/OFF switching. This can be used for resetting a part without Auto-Restart in latch off mode.
- Using External ON terminal (TP4) for driving the ON pin with an external signal.
- Using J2 for setting the ON pin polarity. Set J2 as shown in Figure 1.

Contents of Evaluation Kit

- Evaluation Board
- Cable
- CD
- FPF2100/7 sample parts

Evaluation Board Specifications

The Evaluation Module has test points for convenient access to the all pins and jumpers for setting the various load conditions along with switches for toggling the ON pin and configuring the ON pin polarity. The board is a stand alone unit for testing all functions. The operation input voltage range is 1.8V-5.5V. Board dimensions are 1.75 x 2.35 inches.

Evaluation Board

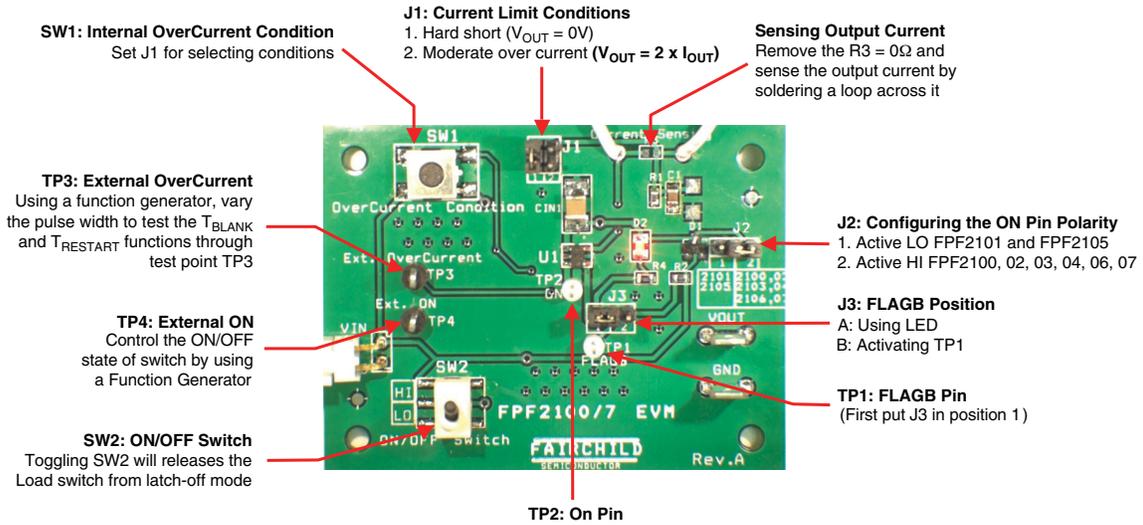


Figure 1. FPF2100/7 EVM Board

Evaluation Board Schematic

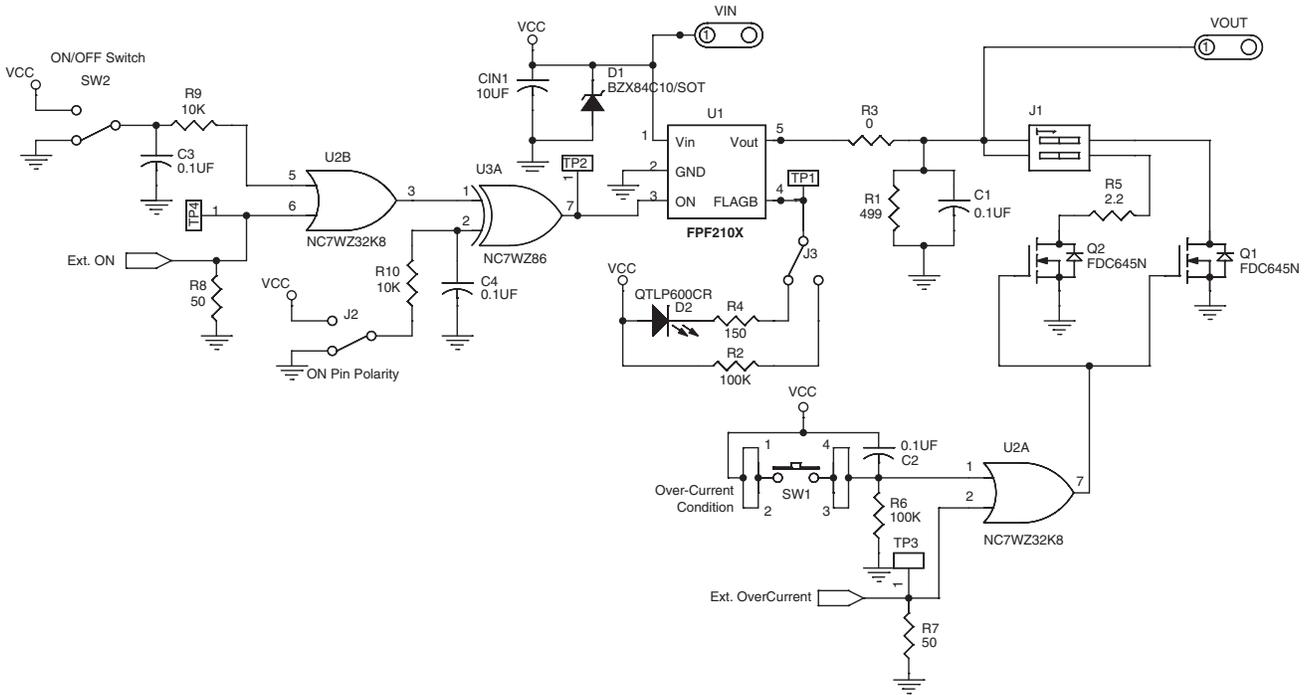


Figure 2. FPF2100/7 EVM Board Schematic

Evaluation Board Block Diagram

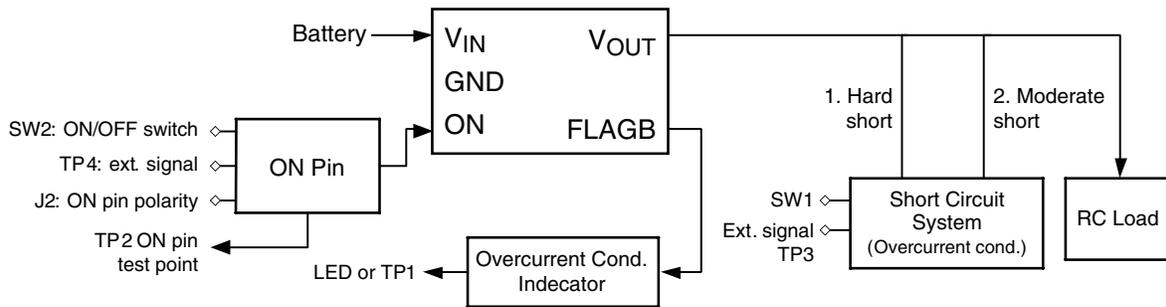


Figure 3. FPF2100/7 EVM Board Block Diagram

Setup and Test Procedure

The following equipment is recommended for testing:

- A four-channel oscilloscope
- Current probe
- One adjustable power supply, 0V-6V@6A
- Voltmeter
- Function generator with burst function single pulse

The EVM board is a suitable platform for testing the main electrical characteristics of the FPF2100/7 products. Various tests such as under voltage lock out, ON input logic voltage, Current Limit value and all dynamic characteristics of the load switch can be performed by using two methods for changing the output, and ON pin condition. The first method is by changing the SW1 or SW2 switches manually on the board, and the second by applying an external signal pulse through TP3 or TP4 for more detailed observation. Here are two examples of test setup:

1. Measuring t_{BLANK} and $t_{RESTART}$ value (Figures 4 to 6)

- Power up the board with $V_{IN} = 3.3V$.
- Remove the current sense resistor (R3) and solder a small wire across R3 in order to use oscilloscope current probe.
- Put the shunt of J3 in position 2, this will connect the FLAGB pin to TP1.
- Put the shunt of J1 to position 2 for moderate overcurrent.
- Connect an external pulse from a function generator to TP3. For better triggering the events on the oscilloscope, a single burst pulse is recommended.

2. Current Limit Response Time at moderate short (Figure 7)

- Power up the board with $V_{IN} = 3.3V$
- Put the shunt of J2 in position 1
- Put the SW2 in position LO
- Put the shunt of J1 in position 2
- Connect an external pulse from a function generator to TP4. For better triggering the events on the oscilloscope, a single burst pulse is recommended
- Push down the pushbutton switch (SW1) while pulsing the TP4

Test Results

1. Measuring t_{BLANK} and $t_{RESTART}$ of FPF2100 (Figures 4 to 6)

This test has been designed to demonstrate the FPF2100 behavior while the output is in a moderate short for 40ms, 170ms, and 180ms. The board setup is described in part 2.0 of this document.

Figure 4 shows the FPF2100 is in an overcurrent condition for 40ms. In this case the load switch limits the output current to the Overcurrent Limit value for t_{BLANK} time. Since the short stays longer than blanking time, the load switch turns off for $t_{RESTART}$ time and the FLAGB pin activates.

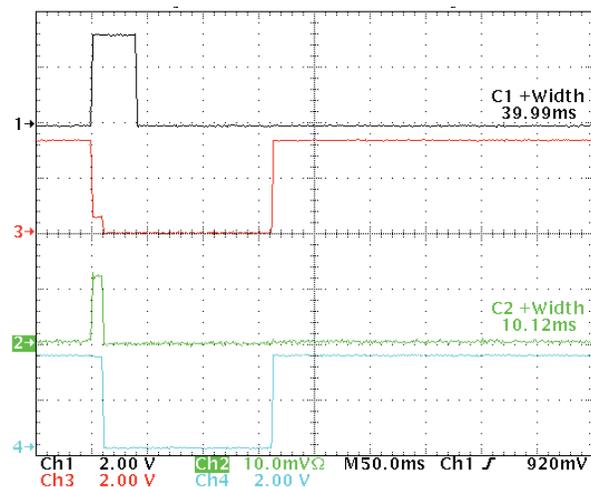


Figure 4. $t_{BLANK} < \text{Overcurrent} = 40\text{ms} < t_{BLANK} + t_{RESTART}$

Figure 4

Ch1 = External overcurrent signal has been applied to gate of a NMOS

Ch2 = I_{OUT} (200mA/div)

Ch3 = V_{OUT}

Ch4 = FLAGB

Figure 5 shows the overcurrent condition stays longer than the $t_{RESTART}$ time. The load switch turns on after $t_{RESTART}$ time has expired and senses the overcurrent condition again. The constant current limit will be supplied to the output for t_{BLANK} . At the end of the second t_{BLANK} , the short was removed from the line and the load switch is in normal operation.

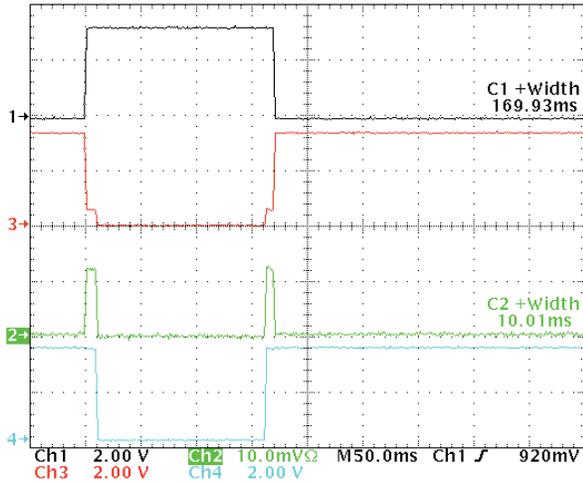


Figure 5. $t_{BLANK} + t_{RESTART} < \text{Overcurrent} = 160\text{ms} < 2x t_{BLANK} + t_{RESTART}$

Figure 6 shows that the overcurrent condition stays longer than one cycle of $t_{BLANK} + t_{RESTART}$. The values of t_{BLANK} and $t_{RESTART}$ can be measured from channel 2 of this figure, where $t_{BLANK} = 10\text{ms}$ and $t_{RESTART} = 150\text{ms}$.

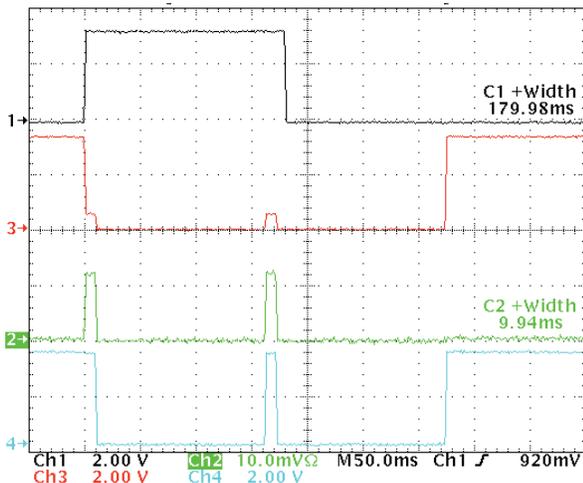


Figure 6. $2x t_{BLANK} + t_{RESTART} < \text{Overcurrent} = 80\text{ms}$

Figures 5 and 6

- Ch1 = External overcurrent signal has been applied to gate of a NMOS
- Ch2 = I_{OUT} (200mA/div)
- Ch3 = V_{OUT}
- Ch4 = FLAGB

2. Current Limit Response Time Test (Figure 7)

This test has been designed to measure the load switch's response time while the output is loaded by a small resistor, 2.2Ω to GND (moderate short). Figure 7 shows response when the input voltage is connected to 3.3V and a moderate short is applied to the output while the ON pin is triggered HI. From the waveforms, it can be seen that the delay between ON pin triggering and output current is about $27\mu\text{s}$.

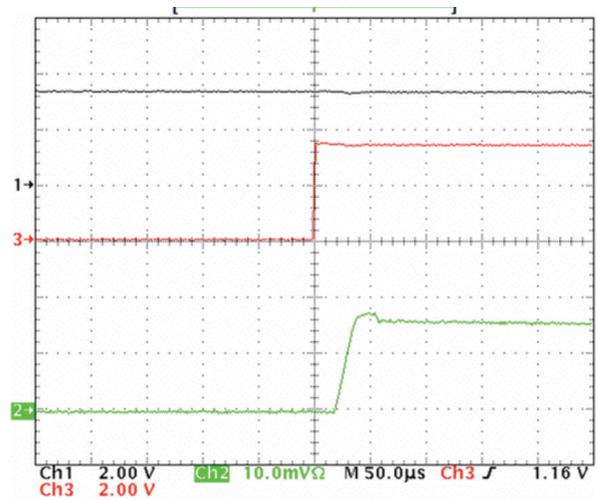


Figure 7. Current Limit Response Time Test

Figure 7

- Ch1 = $V_{IN} = 3.3\text{V}$
- Ch2 = I_{OUT} (200mA/div)
- Ch3 = V_{ON}

Table 1. Evaluation Board Bill of Materials (BOM)

Item	Quantity	Reference	Part	Mfg
1	1	CIN1	10UF	Any
2	4	C1, C2, C3, C4	0.1UF	Any
3	1	D1	BZX84C10 SOT	Fairchild
4	1	D2	QTLP600CR	Fairchild
5	1	J1	Dual Jumper 2mm	Any
6	2	J2, J3	Conn Header 2mm Single	Any
7	2	Q1, Q2	FDC645N	Fairchild
8	1	R1	499	Any
9	2	R2, R6	100K	Any
10	1	R3	0	Any
11	1	R4	150	Any
12	1	R5	2.2	Any
13	2	R7, R8	50	Any
14	2	R9, R10	10K	Any
15	1	SW1	Pushbutton-SPST	Any
16	1	SW2	SPDT	Any
17	4	TP1, TP2, TP3, TP4	Test Point	Any
18	1	U1	FPF2100/1/2/3/4/5/6/7	Fairchild
19	1	U2	NC7WZ32K8	Fairchild
20	1	U3	NC7WZ86	Fairchild

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EcoSPARK™	I ² C™	MSXPro™	RapidConnect™	UniFET™
E ² C MOS™	i-Lo™	OCX™	μSerDes™	VCX™
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		PowerEdge™	SuperSOT™-6	

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