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AN-9088

Smart Power Module, 600V SPM3® Ver6, Series Application Note

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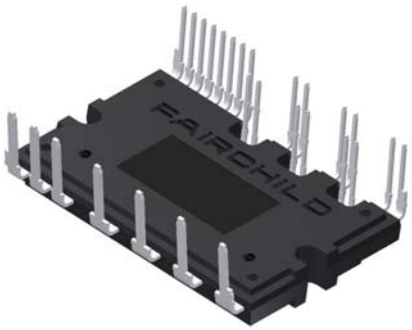
APPLICATION NOTE

1. Introduce

This application note supports the 600V SPM3 version 6 series. It should be used in conjunction with SPM3 datasheets, Onsemi IPM design reference guidance *(RD-572)*, and application note *AN-9086 (Mounting Guidance)*



1.1. Design Concept

The SPM3 design objective is to provide a minimized package and a low power consumption module with improved reliability. This is achieved by applying new gate-driving High-Voltage Integrated Circuit (HVIC), a new Insulated-Gate Bipolar Transistor (IGBT) of advanced silicon technology, and improved Direct Bonded Copper (DBC) substrate base transfer mold package. The SPM3 achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverter motor drives for industrial use, such as air conditioners, general-purpose inverters and serve motors.
The temperature sensing function of SPM3 version 6 products is implemented in the LVIC to enhance the system reliability. An analog voltage proportional to the temperature of the LVIC is provided for monitoring the module temperature and necessary protections against over-temperature situations. The right figure show the package outline structure.

1.2. Key Features

- 600 V 30 A 3-Phase IGBT Inverter Including Control ICs for Gate Driving and Protections
- Very Low Thermal Resistance by Adopting DBC Substrate
- Easy PCB Layout due to Built-in Bootstrap Diodes
- Divided Negative DC-Link Terminals for Inverter Three-Leg current Sensing
- Single-Grounded Power Supply due to Built-in HVICs and Bootstrap Operations
- Built-in Temperature Sensing Unit of IC
- Isolation Rating of 2500 VRMS/min

2. Product description

2.1. Ordering information

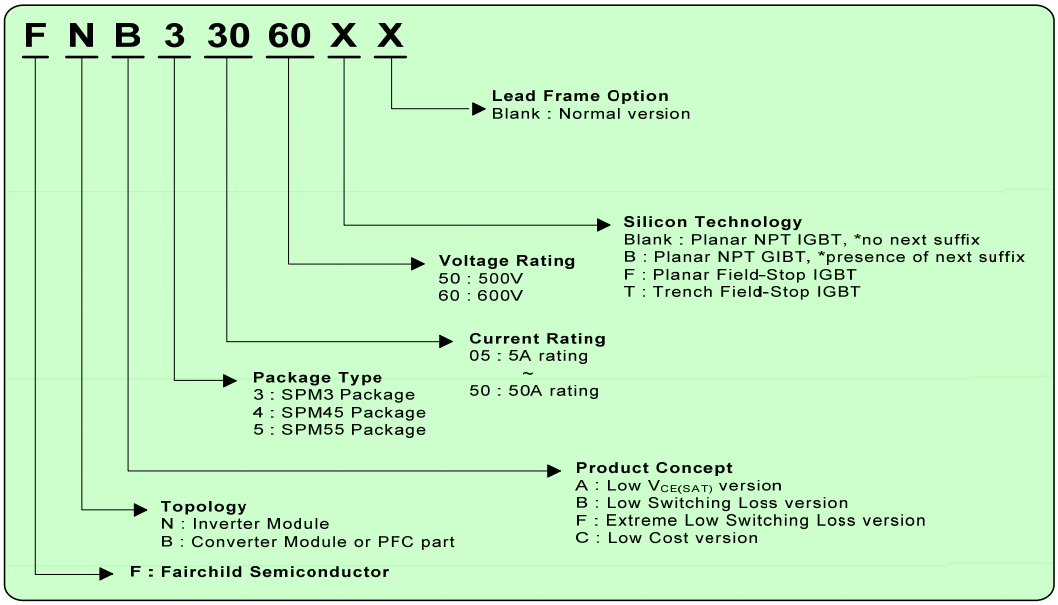


Figure 1. Ordering information of SPM®3 V6

2.2. Product Line-up

Table 1 shows the basic line up without package variations. Online loss and temperature simulation tool, Motion Control Design Tool is recommended to find out the right SPM product for the desired application

Table 1. Product Line-up

Target Application	Device	IGBT Rating	Motor Rating(1)	Isolation Voltage
Air Conditioners, Industrial Motor, General-purpose inverters, Servo motors	FNB33060T	30 A / 600 V	2.2 kW	V_{ISO} = 2500 V_{RMS} (Sine 60 Hz, 1-min All Shorted Pins Heat Sink)
	FNB34060T	40 A / 600 V	3.0kW	
	FNB35060T	50 A / 600 V	3.7kW	

Notes:

1. These motor ratings are general ratings, so may be changed by the operation conditions.

2.3. SPM3 Version Comparison

As it can be seen from Table 2, SPM3 Version 6 products have at least the same or lower V_{CESAT_MAX} compared with the predecessors. Old version products were not released at the same time, and, therefore, there are differences even within the same version products. This version 6 product is the first version in which all the line-up was released at the same with consistent features.

The 600V SPM 3 version 6 products are much more rugged than previous versions in many aspects.

- V_{DD}-Com and V_B-V_S surge noise immunity level increased about 50%. In other words, when a single surge pulse comes in between these pins, Version 2 products can endure 50% higher level of surge voltage without malfunction.
- Destruction level against surge pulses consecutively coming in between V_B and V_S improved significantly.

It should be noted that quiescent current of V_{DD} increased because of TSU function. It does not affect much on selecting the bootstrap capacitor value, but the stand-by power increased by about 2.1mW. There is no change in quiescent current of V_{BS}.

Table 2. SPM3 Version Comparison

SPM3 Version		Version 4		Version 5	Version 6
IGBT Silicon Tech		Planar NPT IGBT		Planar(15, 20 A) / Trench (30 A) NPT IGBT	Trench Field Stop IGBT
Substrate		Full Pack	DBC	Only DBC	Only DBC
Current Rating / V_{CESAT}	5 [A]	FSBF5CH60B / 2.0 [V]	-	-	-
	10 [A]	FSBF10CH60B / 2.0 [V]	-	-	-
	15 [A]	-	FSBB15CH60C / 2.0 [V]	FSBB15CH60D / 2.0 [V]	-
	20 [A]	-	FSBB20CH60C / 2.0 [V]	FSBB20CH60D / 2.0 [V]	-
	30 [A]	-	FSBB20CH60C / 2.4 [V]	FSBB30CH60D / 2.1 [V]	FNB33060T / 1.6 [V]
	40 [A]	-	-	-	FNB34060T / 1.5 [V]
	50 [A]	-	-	-	FNB35060T / 1.65 [V]
V_S-Output		Inner Bonding		Inner Bonding	Inner Bonding
Bootstrap Diode		O		O	O
OC/UV Protection		O		O	O
Thermal Sensing		X		O	O

3. Package

3.1. Internal Circuit Diagram

Major differences between SPM®3Version 6 and previous versions are colored in red in the internal circuit diagram as shown in Figure 2. Even though some old versions also have these features, Version 6 is the second version which widely adopts these features. Main difference was changed from CFOD to V_{TS}. The V_{TS} pin is from LVIC and gives out the temperature sensing signal.

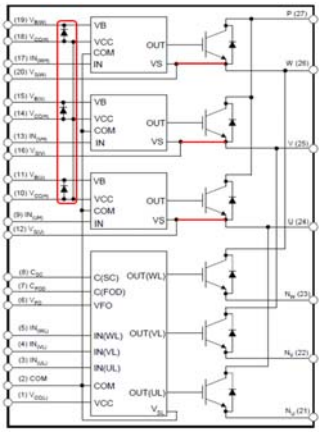
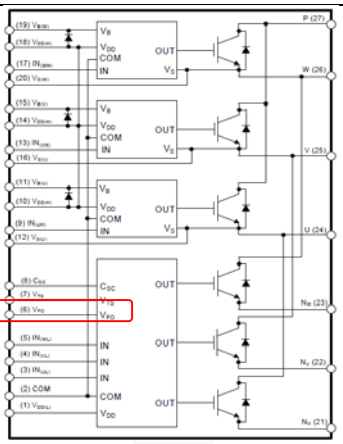
SPM3 Version	Version 4	Version 5&6
Internal Circuit Diagram		
Difference Point	Inner Bonding and add to Bootstrap diode base on Version 2	Changed from CFOD to V_{TS} base on Version 4

Figure 2. SPM3 Version Comparison Internal Circuit

3.2. Pin Description

Figure 3Figure 3 shows the location of pins, the names and dummy pins of SPM3 series.

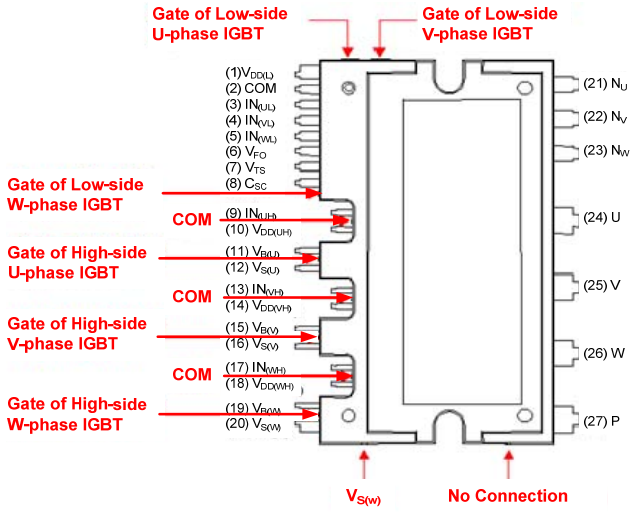


Figure 3. Pin Numbers, Names and Dummy Pins

In the later section illustrates the internal structure of the module in more detail. The detail functional descriptions are provided in Table 3.

Table 3. Pin Description

Pin Number	Name	Description
1	$V_{DD(L)}$	Low-Side Bias Voltage for IC and IGBT Driving
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low-Side U Phase
4	$IN_{(VL)}$	Signal Input for Low-Side V Phase
5	$IN_{(WL)}$	Signal Input for Low-Side W Phase
6	V_{FO}	Fault Output
7	V_{TS}	Output for LVIC Temperature Sensing Voltage
8	C_{SC}	Shunt down input for over current protection
9	$IN_{(UH)}$	Signal Input for High-Side U Phase
10	$V_{DD(H)}$	High-Side Common Bias Voltage for IC and IGBT Driving
11	$V_{B(U)}$	High-Side Bias Voltage for U Phase IGBT Driving
12	$V_{S(U)}$	High-Side Bias Voltage Ground for U Phase IGBT Driving
13	$IN_{(VH)}$	Signal Input for High-Side V Phase
14	$V_{DD(H)}$	High-Side Common Bias Voltage for IC and IGBT Driving
15	$V_{B(V)}$	High-Side Bias Voltage for V Phase IGBT Driving
16	$V_{S(V)}$	High-Side Bias Voltage Ground for V Phase IGBT Driving
17	$IN_{(WH)}$	Signal Input for High-Side W Phase
18	$V_{DD(H)}$	High-Side Common Bias Voltage for IC and IGBT Driving
19	$V_{B(W)}$	High-Side Bias Voltage for W Phase IGBT Driving
20	$V_{S(W)}$	High-Side Bias Voltage Ground for W Phase IGBT Driving
21	N_U	Negative DC Link Input for U Phase
22	N_V	Negative DC Link Input for V Phase
23	N_W	Negative DC Link Input for W Phase
24	U	Output for U Phase
25	V	Output for V Phase
26	W	Output for W Phase
27	P	Positive DC Link Input

3.3. Detailed Pin Definition and Notification

Pins: $V_{B(U)}$-$V_{S(U)}$, $V_{B(V)}$-$V_{S(V)}$, $V_{B(W)}$-$V_{S(W)}$

- High-side bias voltage pins for driving the IGBT / high-side bias voltage ground pins for driving the IGBTs.
- These are drive power supply pins for providing gate drive power to the high-side IGBTs.
- The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side IGBTs.
- Each bootstrap capacitor is charged from the V_{DD} supply during ON state of the corresponding low-side IGBT.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a low-ESR, low-ESL filter capacitor should be mounted very close to these pins.
- Low-side bias voltage pin / high-side bas voltage pins.

Pins: $V_{DD(L)}$, $V_{DD(H)}$

- These are control supply pins for the built-in ICs.
- These four pins should be connected externally.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a low-ESR, low-ESL filter capacitor should be mounted very close to these pins.
- Low-side common supply ground pins.

Pin: COM

- These are supply ground pins for the built-in ICs.
- Important! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin.
- Bootstrap diode cathode pins.

Pins: $V_{B(U)}$, $V_{B(V)}$, $V_{B(W)}$

- These are pins to connect internal bootstrap diode for each high-side bootstrapping.
- External resistor should be connected between these pins and each VDD(xH).
- Signal input pins.

Pins: $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$

- These pins control the operation of the built-in IGBTs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt-trigger circuit composed of 5 V-class CMOS.
- The signal logic of these pins is active HIGH. The IGBT associated with each of these pins is turned.
- ON when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the Motion SPM 3 against noise influences.
- To prevent signal oscillations, an RC coupling as illustrated in Figure 25 is recommended.
- Short-circuit and over-current detection input pin.

Pin: C_{SC}

- The current sensing shunt resistor should be connected between the pin C_{SC} and the low-side ground COM to detect short-current.
- The shunt resistor should be selected to meet the detection levels matched for the specific application. An RC filter should be connected to the CSC pin to eliminate noise.
- The connection length between the shunt resistor and CSC pin should be minimized.
- Fault output pin.

Pin: V_{FO}

- This is the fault output alarm pin. An active LOW output is given on this pin for a fault state condition in the SPM.
- The alarm conditions are: Short-Circuit Current Protection (SCP), and low-side bias Under-Voltage Lockout (UVLO).
- The VFO output is open drain configured. The VFO signal line should be pulled to the 5 V logic power supply with approximately 4.7 kΩ resistance.
- Analog Temperature Sensing Output Pin**.**

Pin: V_{TS}

- This is to indicate the temperature of LVIC with analog voltage. LVIC itself creates some power loss, but mainly heat generated from the IGBTs will increase the temperature of the LVIC.
- VTS versus temperature characteristics is illustrated in Figure 15.
- Positive DC-link pin.

Pin: P

- This is the DC-link positive power supply pin of the inverter.
- It is internally connected to the collectors of the high-side IGBTs.
- To suppress surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (tip: metal film capacitor is typically used).
- Negative DC-link pins.

Pins: NU, NV, NW

- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side IGBT emitters of the each phase.
- These pins are used to one shunt or three shunt resistor.
- Inverter power output pins.

Pins: U, V, W

- Inverter output pins for connecting to the inverter load (e.g. motor).

3.4. Package Structure

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are important in determining the performance. A trade-off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to good package technology lies in the optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In 600V SPM®3, technology was developed with DBC substrate that resulted in good heat dissipation characteristics. Power chips are attached directly to the DBC substrate. This technology is applied 600V SPM3, achieving improved reliability and heat dissipation.
Figure 4 shows the package outline and the cross-sections of the 600V SPM3 package.

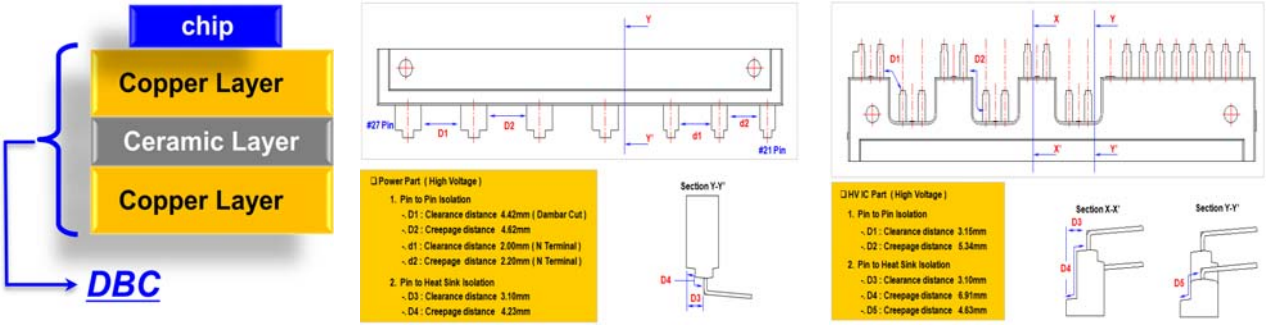


Figure 4. Vertical Structure for Heat Dissipation and Distance for Isolation

Figure 5 shows the internal package structure including the lead frame and boding wires. This design has been revise several times to further improve the manufacturability and the reliability to please the customers more.

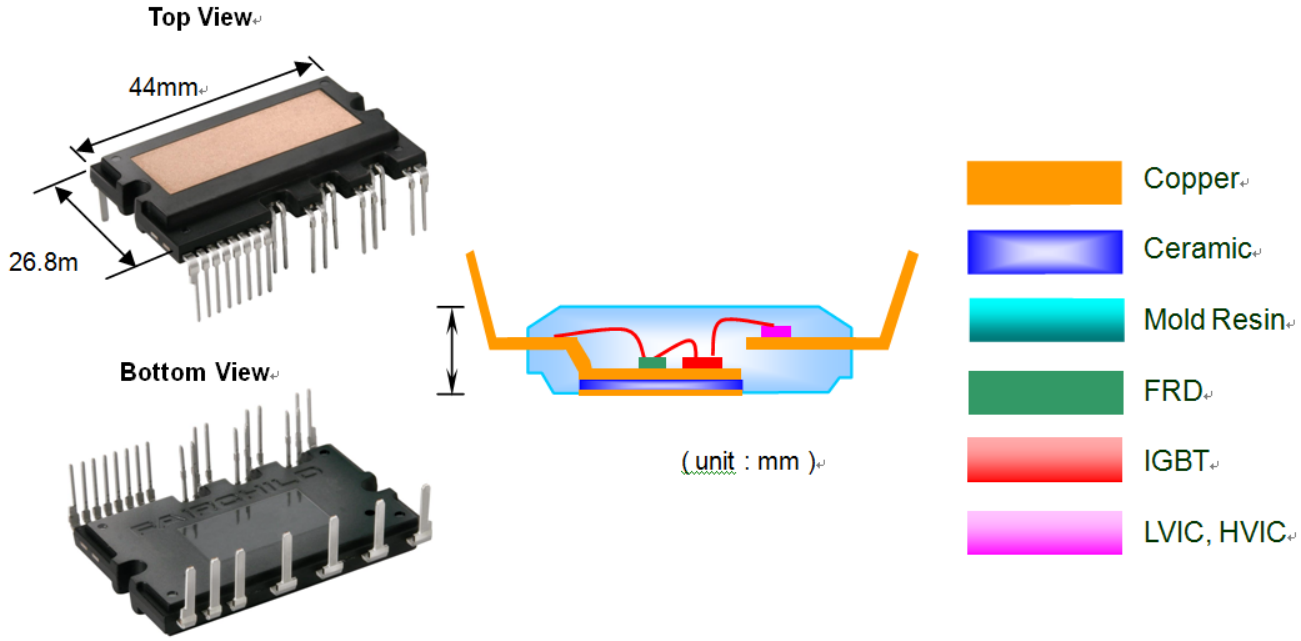
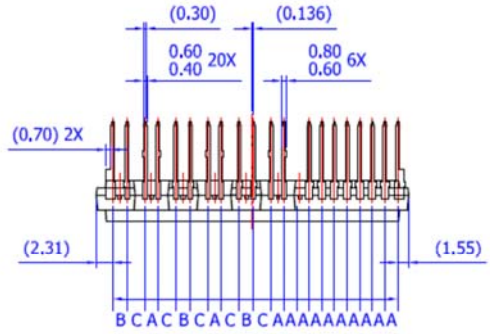
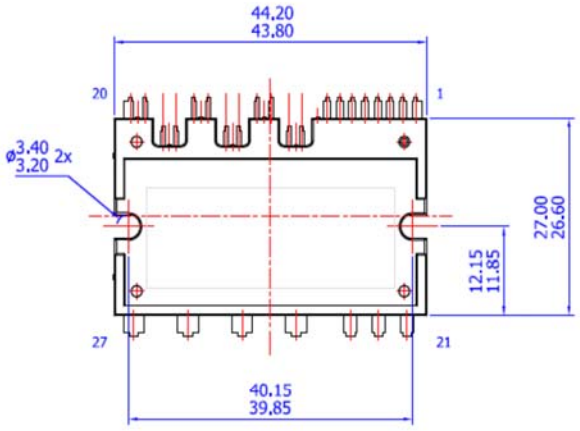


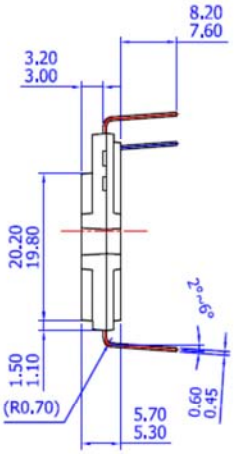
Figure 5. Package Structure and Cross Section for SPM27

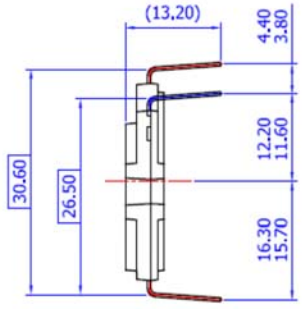
3.5. Marking Specification

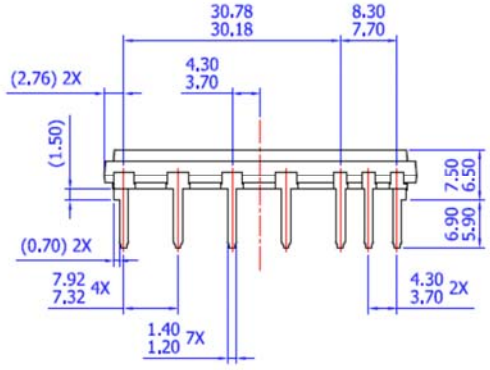


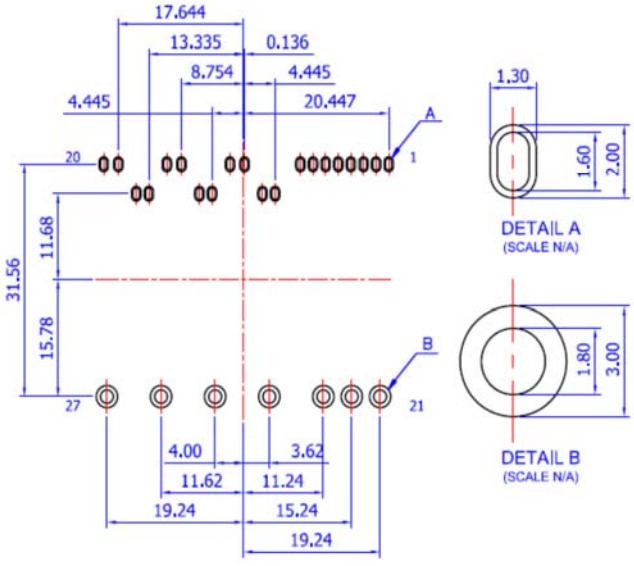
LEAD PITCH (TOLERANCE : ±0.30)
A : 1.778
B : 2.050
C : 2.531











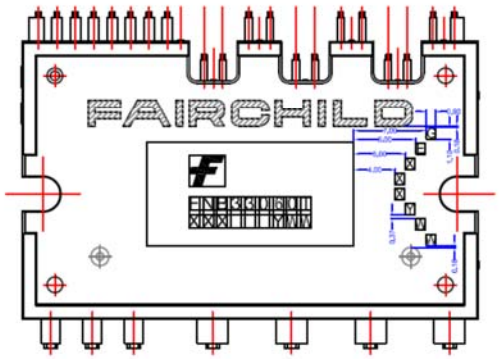
NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) ( ) IS REFERENCE
E) [ ] IS ASS'Y QUALITY
F) DRAWING FILENAME: MOD27BAREV2.0
G) FAIRCHILD SEMICONDUCTOR

LAND PATTERN RECOMMENDATIONS

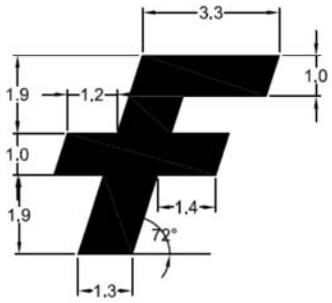
3.6. Marking Specification

REV	REVISION HISTORY	INITIATOR	DATE
1.0	NEW RELEASE	BS WON	2015.11.30

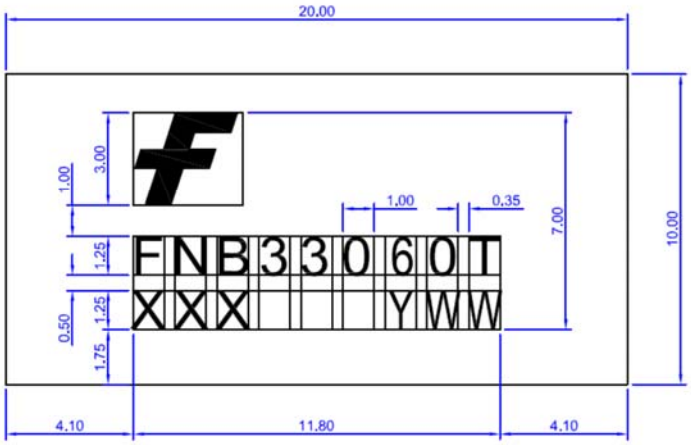
* MARKING LAY-OUT



FAIRCHILD SEMICONDUCTOR LOGO
DIMENSIONAL PROPORTION



* MARKING DIMENSION



X	Alphabet
2010	A
2011	B
2012	C
2013	D
2014	E
2015	F
2016	G
2017	H
2018	J
2019	K
2020	A

*** NOTE**

1. F : FAIRCHILD LOGO
2. XXX : LAST 3 DIGITS OF LOT NO(OPTION CODE)
3. YWW : WORK WEEK CODE ("Y" REFERS TO THE RIGHT ALPHABET CHARACTER TABLE)
4. Hole Side Marking :
   - -. GE : FNB33060T (Product name)
   - -. XXX : Last 3 digits of Lot No.
   - -. YWW : Work Week Code("Y" Refers to the right alphabet character table)

DESIGNED BY	CHECKED BY	CHECKED BY	APPROVED BY
BS WON	SW IM	KY LEE	JS SON
2015.11.30	2015.11.30	2015.11.30	2015.11.30

TITLE FNB33060T
SPM27-RA MARKING LAY-OUT

UNIT	TOLERANCE	SCALE
mm	N / A	N / A

DWG. NO	SPEC. NO	SHEET
FNB33060T	FSSD0932	1/1

4. Product Synopsis

This section discusses electrical specification, characteristics and mechanical characteristics.

4.1. Absolute Maximum Rating (T_J=25°C, unless otherwise specified)

Table 4. Inverter Part (Base on FNB33060T)

Symbol	Parameter	Conditions	Rating	Unit
V_{PN}	Supply Voltage	Applied between P –NU, NV, NW	450	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P – NU, NV, NW	500	V
V_{CES}	Collector – Emitter Voltage		600	V
$\pm I_C$	Each IGBT Collector Current	T_C=25°C, T_J≤150°C (Note 2)	30	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	T_C=25°C, T_J≤150°C, Under 1 ms Pulse Width(2)	60	A
P_C	Collector Dissipation	T_C=25°C per One Chip	89	W
T_J	Operating Junction Temperature (Note 3)		-40~150	°C

Notes:

2. These values had been made on acquisition by the calculation considered to design factor.
3. The maximum junction temperature rating of power chips integrated within the SPM3 version 6 products are 150°C.

Table 5. Control Part

Symbol	Parameter	Conditions	Rating	Unit
V_{DD}	Control Supply Voltage	Applied between $V_{DD(H)}$, $V_{DD(L)}$ - COM	20	V
V_{BS}	High-Side Control Bias Voltage	Applied between $V_{B(U)}$-$V_{S(U)}$,$V_{B(V)}$-$V_{S(V)}$, $V_{B(W)}$-$V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, - COM	-0.3~V_{DD}+0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} – COM	-0.3~V_{DD}+0.3	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} Pin	2	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} - COM	-0.3~V_{DD}+0.3	V

Table 6. Bootstrap Diode Part

Symbol	Parameter	Conditions	Rating	Unit
V_{RRM}	Maximum Repetitive Reverse Voltage		600	V
I_F	Forward Current	T_C=25°C, T_J≤150°C	0.5	A
I_{FP}	Forward Current (Peak)	T_C=25°C, T_J≤150°C, Under 1 ms Pulse Width	2.0	A
T_J	Operating Junction Temperature		-40~150	°C

Table 7. Total System

Symbol	Parameter	Conditions	Rating	Unit
$V_{PN(PROT)}$	Self Protection Supply Voltage Limit (Short-Circuit Protection Capability)	VDD, VBS=13.5~16.5 V, TJ=50°C, Non-Repetitive, < 2 μs	400	V
T_C	Module Case Operation Temperature	See Figure 6**Error! Reference source not found.**	-40~125	°C
T_{STG}	Storage Temperature		-40~125	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1-Minute, Connect Pins to Heat Sink	2500	Vrms

Table 8. Thermal Resistance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (Note 4)	Inverter IGBT Part (per 1/6 Module)	1.4			°C/W
$R_{th(j-c)F}$		Inverter FWD Part (per 1/6 Module)	2.4			

Note:

4. For the measurement point of case temperature (T_C), please refer Figure 6

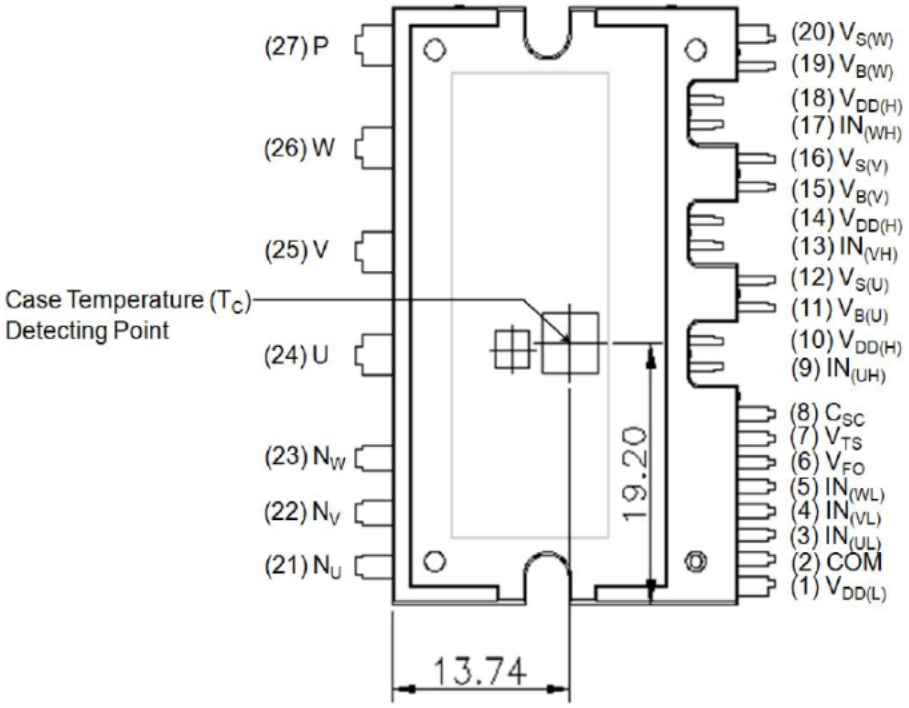


Figure 6. Case Temperature (T_C) Detecting Point

4.2. Electrical Characteristic (T_J=25°C, unless otherwise specified)

Table 9. Inverter Part (Base on FNB33060T)

Symbol		Parameter	Condition		Min	Typ	Max	Unit
$V_{CE(SAT)}$		Collector–Emitter Saturation Voltage	V_{DD}, V_{BS}=15 V, V_{IN}=5 V	I_C=30 A, T_J=25°C		1.60	2.20	V
V_F		FWD Forward Voltage	V_{IN}=0 V	I_F=30 A, T_J=25°C		2.00	2.60	V
HS	t_{ON}	Switching Times	V_{PN}=300 V, V_{DD}=15 V, V_{BS}=15 V, I_C=30 A T_J=25°C, V_{IN}=0 V ↔ 5 V, Inductive Load See Figure 7		0.50	0.90	1.40	µs
	$t_{C(ON)}$					0.25	0.55	µs
	t_{OFF}					0.85	1.35	µs
	$t_{C(OFF)}$					0.15	0.40	µs
	t_{rr}					0.08		µs
LS	t_{ON}				0.40	0.80	1.30	µs
	$t_{C(ON)}$					0.25	0.55	µs
	t_{OFF}					0.90	1.40	µs
	$t_{C(OFF)}$					0.15	0.45	µs
	t_{rr}				0.10			µs
I_{CES}		Collector – Emitter Leakage Current	V_{CE}=V_{CES}				5	mA

Note:

5. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detail information, please see and Figure 7

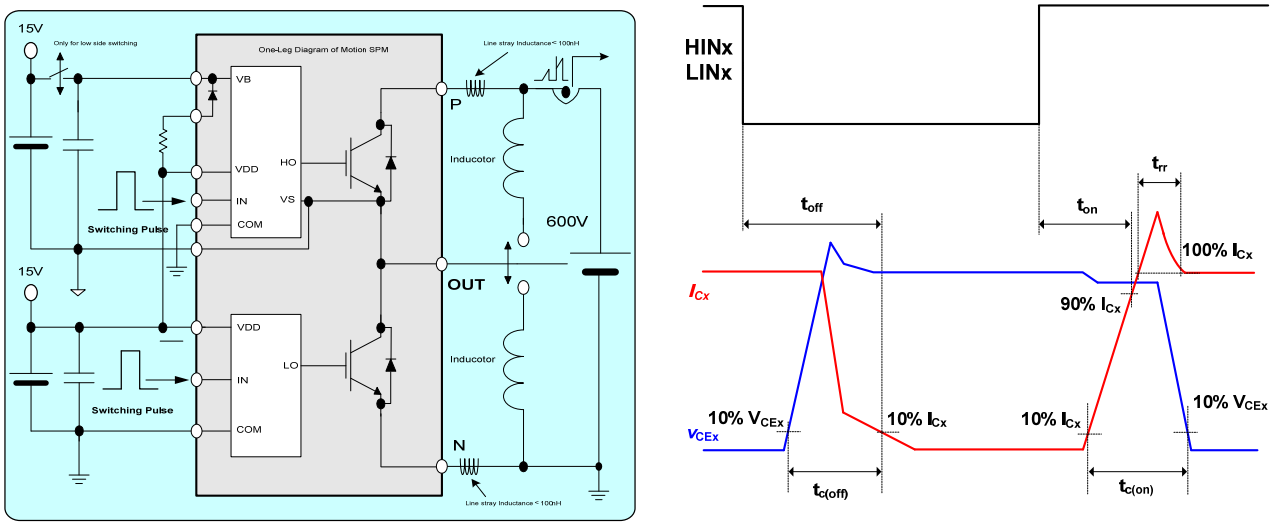


Figure 7. Switching Evaluation Circuit and Switching Time Definition

Table 10. Bootstrap Diode Part

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_F	Forward Voltage	I_F=0.1 A, T_J=25°C		2.5		V
t_{rr}	Reverse Recovery Time	I_F=0.1 A, dI_F / dt=50 A/µs, T_J=25°C		80		ns

Table 11. Control Part

Symbol	Parameter	Condition		Min	Typ	Max	Unit
I_{QDDH}	Quiescent V_{DD} Supply Current	$V_{DD(H)}$=15V, $IN_{(UH,VH,WH)}$ =0V	$V_{DD(H)}$ - COM			0.50	mA
I_{QDDL}		$V_{DD(L)}$=15V, $IN_{(UL,VL,WL)}$ =0V	$V_{DD(L)}$ - COM			6.00	
I_{PDDH}	Operating High-Side V_{DD} Supply Current	$V_{DD(H)}$=15V, f_{PWM}=20 kHz, Duty=50%, Applied to One PWM Signal Input for High Side				0.50	mA
I_{PDDL}		$V_{DD(L)}$=15V,f_{PWM}=20 kHz, Duty=50%, Applied to One PWM Signal Input for Low Side				10.0	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS}=15V, $IN_{(UH,VH,WH)}$=0V				0.30	mA
I_{PBS}	Operating V_{BS} Supply Current	V_{DD}=V_{BS}=15 V, f_{PWM}=20 kHz, Duty=50%, Applied to One PWM Signal Input for High Side				4.50	mA
V_{FOH}	Fault Output Voltage	V_{DD}=15 V, V_{SC}=0 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up		4.5			V
V_{FOL}		V_{DD}=15 V, V_{SC}=1 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up				0.5	
$V_{SC(ref)}$	Short-Circuit Trip Level	V_{DD}=15 V	C_{SC} - COM	0.45	0.50	0.55	V
UV_{DDD}	Supply Circuit, Under-Voltage Protection (Note 6)	Detection Level		9.8		13.3	V
UV_{DDR}		Reset Level		10.3		13.8	
UV_{BSD}		Detection Level		9.0		12.5	
UV_{BSR}		Reset Level		9.5		13.0	
t_{FOD}	Fault-Out Pulse Width			50			µs
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $IN_{(UH,VH,WH)}$ - COM, $IN_{(UL,VL,WL)}$ - COM				2.6	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8			

Note:

6. Short-circuit current protection is functioning only at low side.

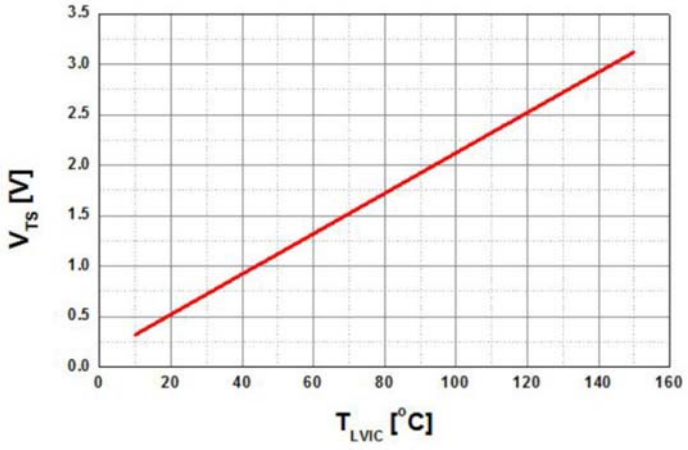


Figure 8. Temperature Profile of V_{TS} (Typical)

4.3. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PN}	Supply Voltage	Applied between P - N_U, N_V, N_W		300	400	V
V_{DD}	Control Supply Voltage	Applied between $V_{DD(UH,VH,WH)}$ - COM, $V_{DD(L)}$ - COM	14.0	15.0	16.5	
V_{BS}	High-Side Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	13.0	15.0	18.5	V
dV_{DD}/dt, dV_{BS}/dt	Control Supply Variation		-1		+1	V/µs
t_{dead}	Blanking Time for Preventing Arm-Short	For Each Input Signal	1.0			µs
f_{PWM}	PWM Input Signal	-40°C ≤ T_C ≤ 125°C, - 40°C ≤ T_J ≤ 150°C			20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W – COM (Including Surge Voltage)	-5		5	V
$P_{WIN(ON)}$	Minimum Input Pulse Width	V_{DD}=V_{BS}=15V, I_C ≤ 60A, Wiring Inductance between $N_{U,V,W}$ and DC Link N<10nH[7]	2.0.			µs
$P_{WIN(OFF)}$			2.0			
T_J	Junction Temperature		-40		150	°C

Note:

7. This product might not make response if input pulse with is lee than the recommended value.

4.4. Mechanical Characteristics

Parameter	Condition		Min	Typ	Max	Unit
Device Flatness	See Figure 9**Error! Reference source not found.**		0		+150	µm
Mounting Torque	Mounting Screw: M3 See Figure 10	Recommended 0.7 N·m	0.6	0.7	0.8	N·m
		Recommended 7.1 kg·cm	6.2	7.1	8.1	kg·cm
Terminal Pulling Strength	Load 19.6 N		10			s
Terminal Bending Strength	Load 9.8 N, 90° Bend		2			Times
Weight	Module Weight			50		g

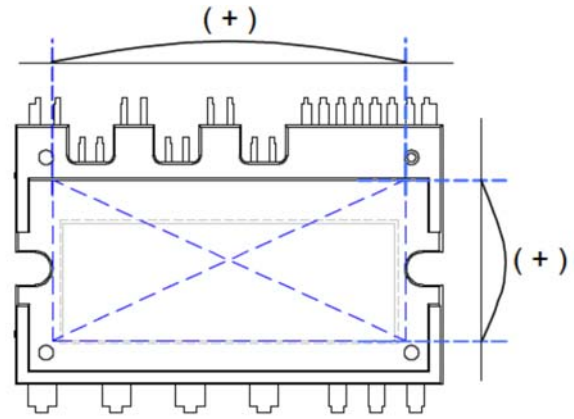


Figure 9. Flatness Measurements Position

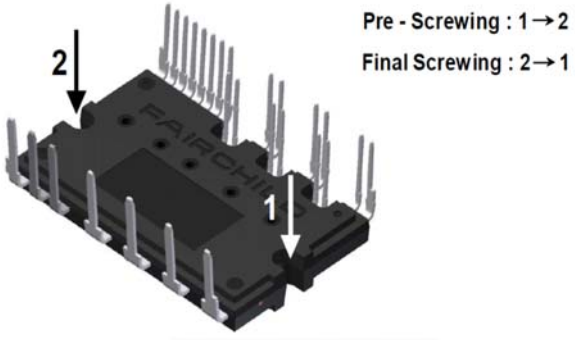


Figure 10. Mounting Screw Torque Order

5. Operation Sequence for Protections

5.1. Short Circuit Protection

The 600V SPM®3 uses external shunt resistor for the short circuit current detection, as shown in Figure 11. LVIC has a built-in short-circuit current protection function. This protection function senses the voltage to the CSC pin. If this voltage exceeds the $V_{SC(ref)}$ (the threshold voltage trip level of the short-circuit) specified in the device datasheets($V_{SC(ref)}$, typ. is 0.5 V), a fault signal is asserted and the all low side IGBTs are turned off.

Typically, the maximum short-circuit current magnitude is gate-voltage dependent: higher gate voltage (V_{DD} and V_{BS}) results in larger short-circuit current. To avoid potential problems, the maximum short-circuit trip level is set below 1.5 times the nominal rated collector current. The LVIC short-circuit current protection-timing chart is shown in Figure 12.

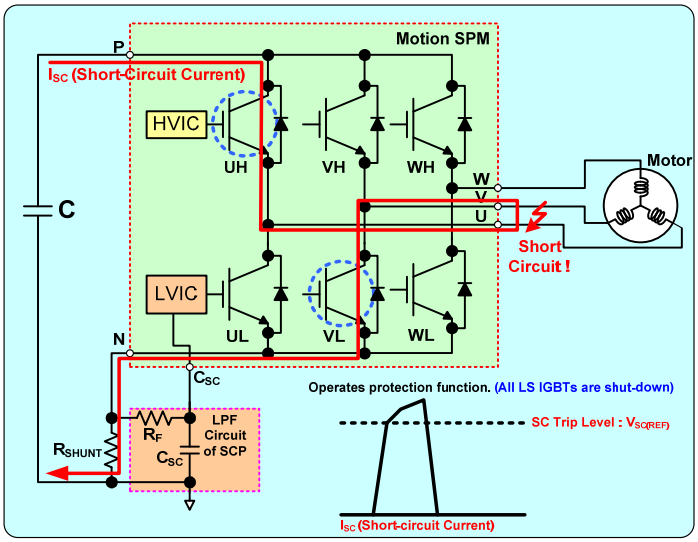


Figure 11. Operation of Short-Circuit Protection

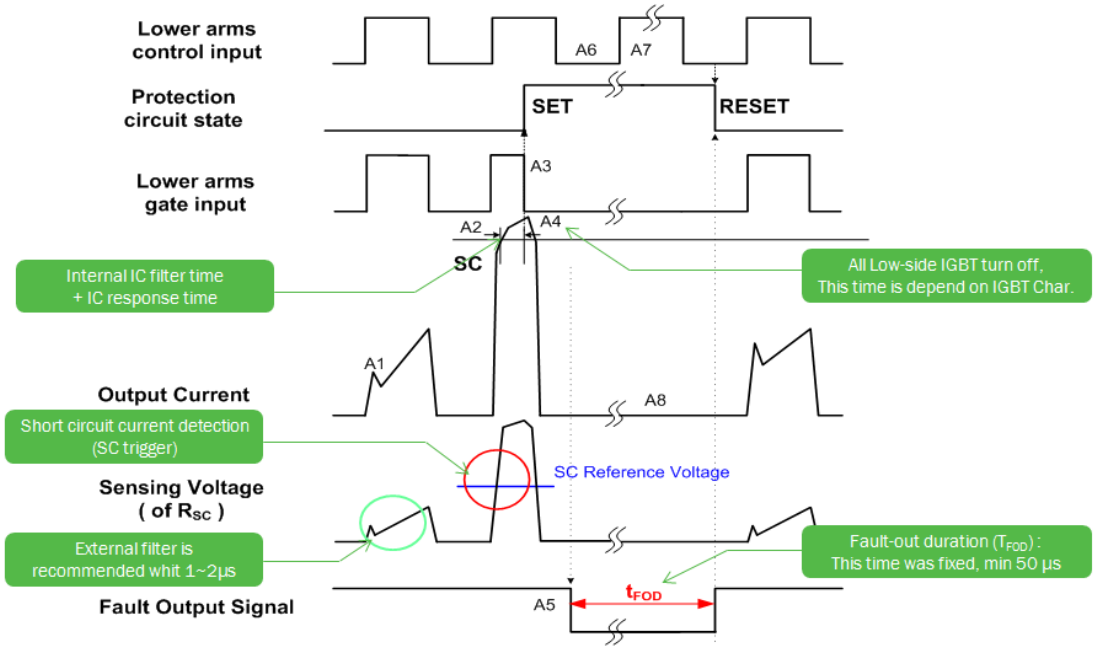


Figure 12. Timing Chart of Short-Circuit Protection Function

Notes:

8. A1-normal operation: IGBT on and carrying current.
9. A2-short-circuit current detection (SC trigger).
10. A3-hard IGBT gate interrupt.
11. A4-IGBT turns OFF.
12. A5-fault output timer operation start with internal delay (typ. 2.8 µs), Fault-out duration time is fix (min. 50 µs).
13. A6-input "L": IGBT OFF state.
14. A7-input "H": IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.
15. A8-IGBT keeps OFF state

5.2. Under-Voltage Lockout Protection

The LVIC has an Under-Voltage Lockout protection (UVLO) function to protect the low-side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 13

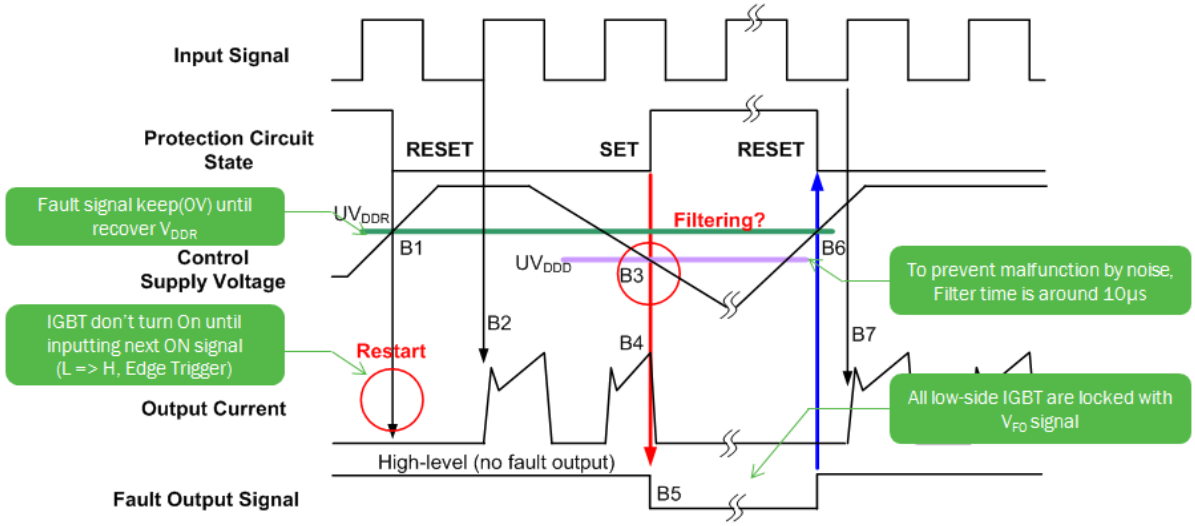


Figure 13. Timing Chart of Low-side Under-Voltage Protection Function

Notes: (Low-Side Protection Sequence)

16. B1-control supply voltage rise: after the voltage rises UV_{DDR}, the circuits starts to operate when the next input is applied (L => H)
17. B2-normal operation: IGBT ON and carrying current.
18. B3-under-voltage detection (UV_{DDD}).
19. B4-IGBT OFF in spite of control input is alive.
20. B5-Fault output signal starts.
21. B6-under-voltage reset (UV_{DDR}).
22. B7-normal operation: IGBT ON and carrying current

5.3. Under-Voltage Lockout Protection (High-side UVLO)

The HVIC has an under-voltage lockout function to protect the high-side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 14. A fault-out (FO) alarm is not given for low HVIC bias conditions

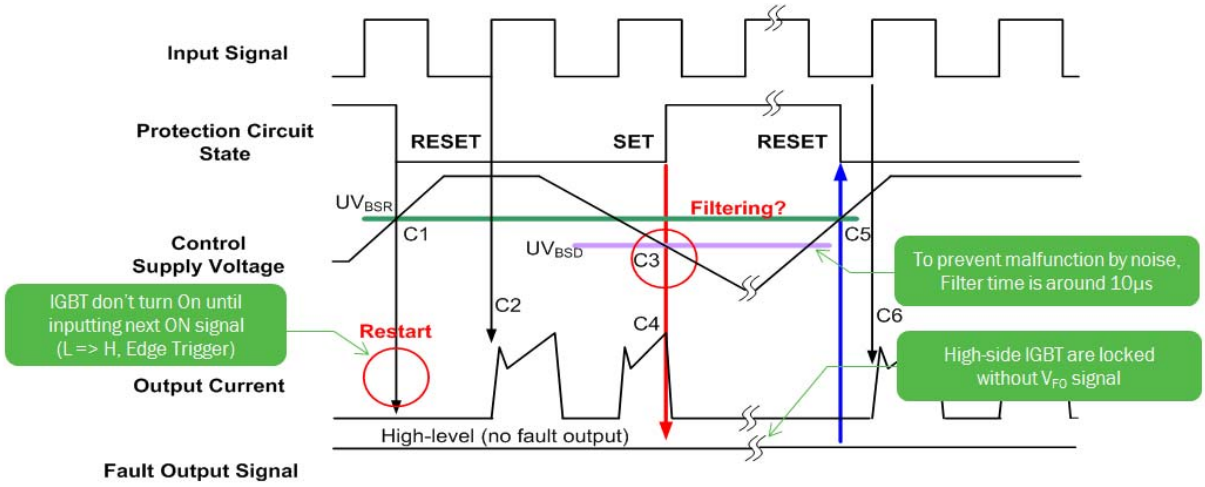


Figure 14. Timing Chart of High-Side Under-Voltage Protection Function

Notes: (High-Side Protection Sequence)

23. C1-control supply voltage rises: after the voltage reaches UV_{BSR}, the circuit starts when the next input is applied.
24. C2-normal operation: IGBT ON and carrying current.
25. C3-under-voltage detection (UV_{BSD}).
26. C4-IGBT OFF in spite of control input is alive, but there is no fault output signal.
27. C5-under-voltage reset (UV_{BSR}).
28. C6-normal operation: IGBT ON and carrying current

6. Key Parameter Design Guidance

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of the 600V SPM®3 version 6 series

6.1. Thermal Sensing Unit (TSU)

The junction temperature of power devices should not exceed the maximum junction temperature. Even though there is some margin between the T_{JMAX} specified on the datasheet and the actual T_{JMAX} at which power devices get destroyed, caution should be given to make sure the junction temperature stays well below the $_{JMAX}$. One of the inconveniences in using previous versions of SPM 3 series products was lack of temperature monitoring. An NTC had to be mounted on the heat sink or very close to the module if over-temperature protection is required in the application

6.1.1. Basic Concept

Thermal Sensing Unit uses technology based on the temperature dependency of transistor Vbe; Vbe decrease 2 mV as temperature increase 1°C.

The Thermal Sensing Unit analog voltage output reflects the temperature of the LVIC in 600V SPM 3 version 6 series products. The relationship between V_{TS} voltage output and LVIC temperature is shown in Figure 16. It does not have any self-protection function, and, therefore, it should be used appropriately based on application requirement. It should be noted that there is a time lag from IGBT temperature to LVIC temperature. It is very difficult to respond quickly when temperature rises sharply in a transient condition such as shoot-through event. Even though TSU has some limitation, it will be definitely useful in enhancing the system reliability.

Figure 15 shows the LVIC location of SPM3 series.

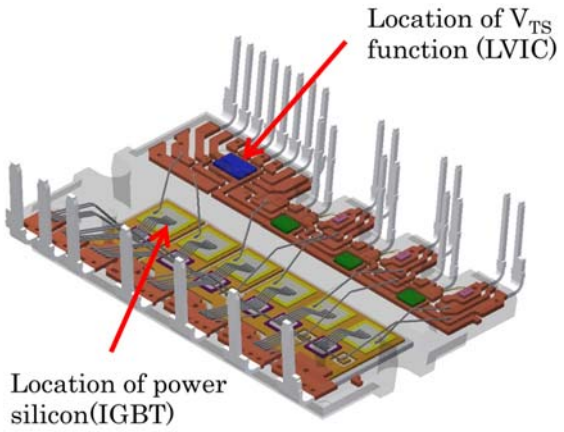


Figure 15. Location of VTS Function (LVIC)

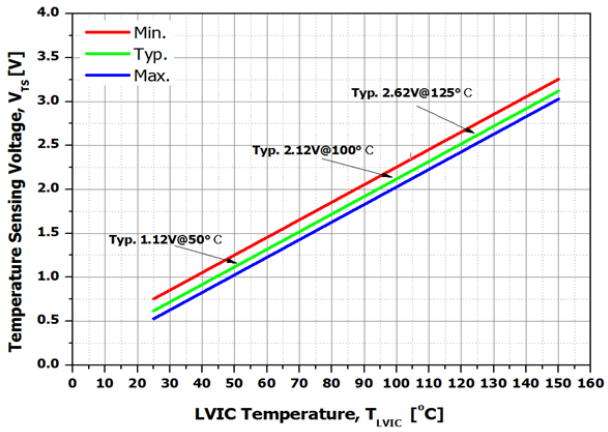


Figure 16. Temperature vs. V_{TS}

Error! Reference source not found. shows the equivalent circuit diagram of TSU inside IC and a typical application diagram. This output voltage is clamped to 5.2 V by an internal Zener diode, but in case the maximum input range of Analog to Digital converter of MCU is below 5.2 V, an external Zener diode should be inserted between an A/D input pin and the analog ground pin of MCU. An amplifier can be used to change the range of voltage input to the Analog to Digital converter to have better resolution of the temperature. It is recommended to add a ceramic capacitor of 1000 pF between V_{TS} and Com (Ground) to make the V_{TS} more stable.

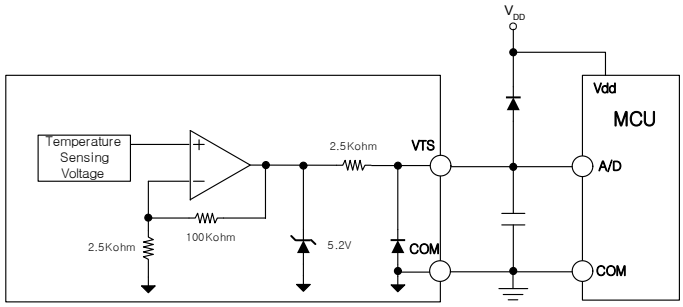
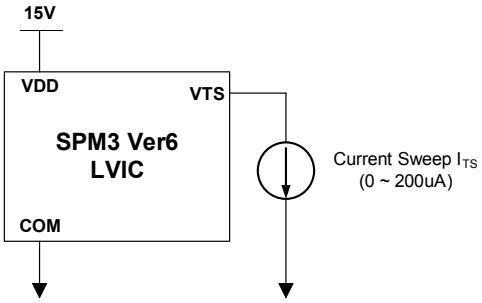


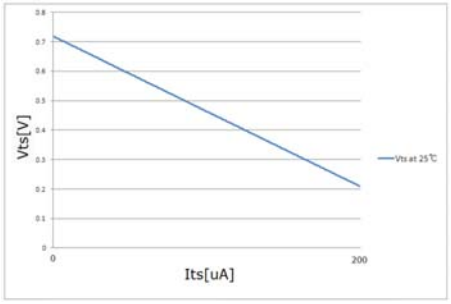
Figure 17. Internal Block Diagram and Interface Circuit of TSU

Figure 18 shows the sourcing capability of V_{TS} pin at 25°C and the test method. V_{TS} voltage decreases as the sourcing current increases. Therefore, the load connected to V_{TS} pin should be minimized to maintain the accurate voltage output level without degradation. Figure 16Figure 16 shows that the relationship between V_{TS} voltage and LVIC temperature. It can be expressed as the following equation.

- $V_{TS,min} = 0.02*T_{LVIC} + 0.04$ [V]
- $V_{TS,typ} = 0.02*T_{LVIC} + 0.14$ [V]
- $V_{TS,max} = 0.02*T_{LVIC} + 0.24$ [V]



(a) Test Method



(B) Test Result

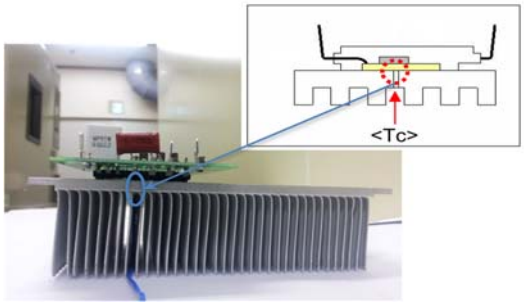
Figure 18. Real Load Variation of VTS

The maximum variation of V_{TS} is 0.24 V, and the minimum variation of V_{TS} is 0.04 V due to process variation which is equivalent ±5°C approximately. This is regardless of the temperature because the slopes of three lines are identical. If the ambient temperature information is available, for example, through NTC in the system, V_{TS} can be measured to adjust the offset before the motor starts to operate.

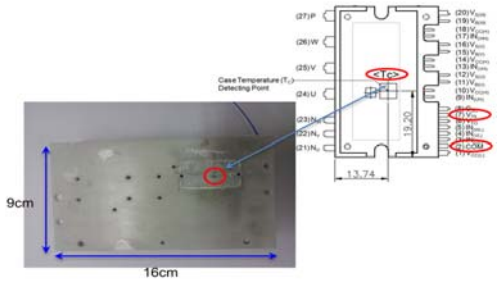
As temperature decreases further below 0°C, V_{TS} decreases linearly until it reaches zero volts. If the temperature of LVIC increases above 150°C, which is above the maximum operating temperature, V_{TS} would increase theoretically up to 5.2 V until it gets clamped by the internal Zener diode.

6.1.2. Test Method

This test result shows correlation between V_{TS} and T_C, but this correlation will be changed each customer real application conditions. Figure 19 shows the test board and temperature measure point.



(a) Test board



(B) Heat-sink Size and Measure Point of T_C

Figure 19. Heat-sink size and measure point of T_C

We tested real load by servo dynamo systems, refer to the Figure 20.

Figure 20. Real Load Dynamometer

We have compared between convection cooling and forced cooling mode. Figure 21 shows the cooling conditions
To avoid external environment, we used the case, refer to Figure 22.
Test conditions were V_{DD} =15 V, V_{DC}=300 V, Frequency = 5 kHz and PWM method=SPWM.

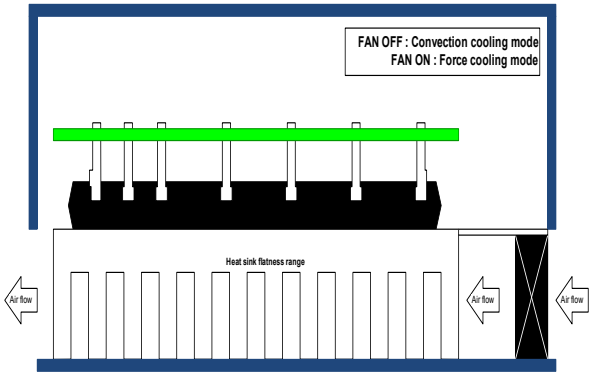


Figure 21. Cooling Conditions

Figure 22. Test Environment

6.1.3. Test Results

Figure 23 and Figure 24 shows the test result. As the test results, T_C and V_{TS} temperatures have a variable gap by cooling conditions. Fragmentarily, this test result shows, V_{TS} value is depend on cooling conditions (Heat sink size, Fan speed and etc). Temperature gap has about 20 degree between T_C and V_{TS} in convection cooling mode. And gap has about 10 degree in force cooling mode.

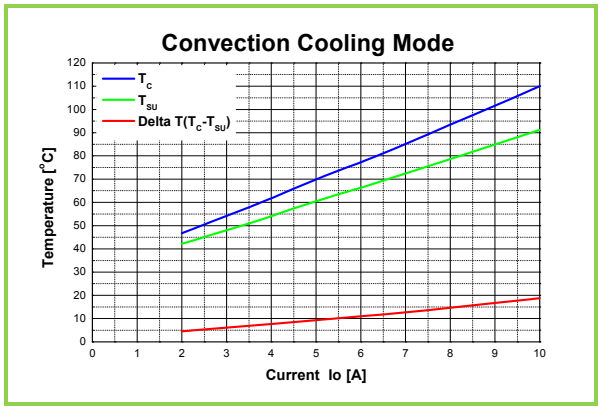


Figure 23. Convection Cooling Mode

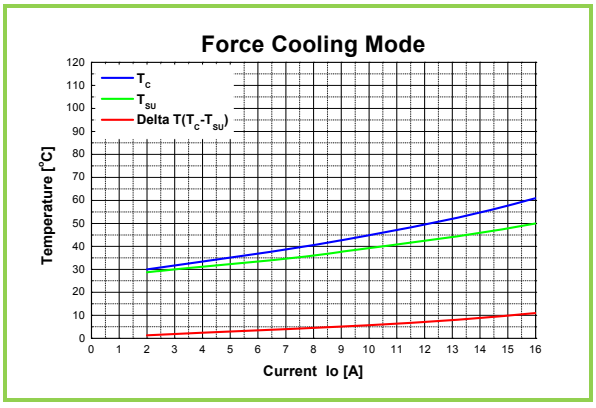


Figure 24. Force Cooling Mode

In conclusion, if the customer wants to use the thermal sensing unit (T_{SU}), they should make adjustment in real operation conditions by themselves. And heat generated at IGBT and FWDi transfer to LVIC through modeling resin of package and outer heat sink. So LVIC temperature cannot respond to rapid temperature rise of those power chips effectively.

Table 12. V_{TS} Table of LVIC

T_{LVIC} (°C)	V_{MIN} (V)	V_{TYP} (V)	V_{MAX} (V)	T_{LVIC} (°C)	V_{MIN} (V)	V_{TYP} (V)	V_{MAX} (V)
25	0.54	0.64	0.74	70	1.44	1.54	1.64
26	0.56	0.66	0.76	71	1.46	1.56	1.66
27	0.58	0.68	0.78	72	1.48	1.58	1.68
28	0.60	0.70	0.80	73	1.50	1.60	1.70
29	0.62	0.72	0.82	74	1.52	1.62	1.72
30	0.64	0.74	0.84	75	1.54	1.64	1.74
31	0.66	0.76	0.86	76	1.56	1.66	1.76
32	0.68	0.78	0.88	77	1.58	1.68	1.78
33	0.70	0.80	0.90	78	1.60	1.70	1.80
34	0.72	0.82	0.92	79	1.62	1.72	1.82
35	0.74	0.84	0.94	80	1.64	1.74	1.84
36	0.76	0.86	0.96	81	1.66	1.76	1.86
37	0.78	0.88	0.98	82	1.68	1.78	1.88
38	0.80	0.90	1.00	83	1.70	1.80	1.90
39	0.82	0.92	1.02	84	1.72	1.82	1.92
40	0.84	0.94	1.04	85	1.74	1.84	1.94
41	0.86	0.96	1.06	86	1.76	1.86	1.96
42	0.88	0.98	1.08	87	1.78	1.88	1.98
43	0.90	1.00	1.10	88	1.80	1.90	2.00
44	0.92	1.02	1.12	89	1.82	1.92	2.02
45	0.94	1.04	1.14	90	1.84	1.94	2.04
46	0.96	1.06	1.16	91	1.86	1.96	2.06
47	0.98	1.08	1.18	92	1.88	1.98	2.08
48	1.00	1.10	1.20	93	1.90	2.00	2.10
49	1.02	1.12	1.22	94	1.92	2.02	2.12
50	1.04	1.14	1.24	95	1.94	2.04	2.14
51	1.06	1.16	1.26	96	1.96	2.06	2.16
52	1.08	1.18	1.28	97	1.98	2.08	2.18
53	1.10	1.20	1.30	98	2.00	2.10	2.20
54	1.12	1.22	1.32	99	2.02	2.12	2.22
55	1.14	1.24	1.34	100	2.04	2.14	2.24
56	1.16	1.26	1.36	101	2.06	2.16	2.26
57	1.18	1.28	1.38	102	2.08	2.18	2.28
58	1.20	1.30	1.40	103	2.10	2.20	2.30
59	1.22	1.32	1.42	104	2.12	2.22	2.32
60	1.24	1.34	1.44	105	2.14	2.24	2.34
61	1.26	1.36	1.46	106	2.16	2.26	2.36
62	1.28	1.38	1.48	107	2.18	2.28	2.38
63	1.30	1.40	1.50	108	2.20	2.30	2.40
64	1.32	1.42	1.52	109	2.22	2.32	2.42
65	1.34	1.44	1.54	110	2.24	2.34	2.44
66	1.36	1.46	1.56	111	2.26	2.36	2.46
67	1.38	1.48	1.58	112	2.28	2.38	2.48
68	1.4	1.5	1.6	113	2.30	2.40	2.50
69	1.42	1.52	1.62	114	2.32	2.42	2.52

T_{LVIC} (°C)	V_{MIN} (V)	V_{TYP} (V)	V_{MAX} (V)	T_{LVIC} (°C)	V_{MIN} (V)	V_{TYP} (V)	V_{MAX} (V)
115	2.34	2.44	2.54	133	2.70	2.80	2.90
116	2.36	2.46	2.56	134	2.72	2.82	2.92
117	2.38	2.48	2.58	135	2.74	2.84	2.94
118	2.40	2.50	2.60	136	2.76	2.86	2.96
119	2.42	2.52	2.62	137	2.78	2.88	2.98
120	2.44	2.54	2.64	138	2.80	2.90	3.00
121	2.46	2.56	2.66	139	2.82	2.92	3.02
122	2.48	2.58	2.68	140	2.84	2.94	3.04
123	2.50	2.60	2.70	141	2.86	2.96	3.06
124	2.52	2.62	2.72	142	2.88	2.98	3.08
125	2.54	2.64	2.74	143	2.90	3.00	3.10
126	2.56	2.66	2.76	144	2.92	3.02	3.12
127	2.58	2.68	2.78	145	2.94	3.04	3.14
128	2.60	2.70	2.80	146	2.96	3.06	3.16
129	2.62	2.72	2.82	147	2.98	3.08	3.18
130	2.64	2.74	2.84	148	3.00	3.10	3.20
131	2.66	2.76	2.86	149	3.02	3.12	3.22
132	2.68	2.78	2.88	150	3.04	3.14	3.24

6.2. Selection of Shunt Resistor

Figure 25 shows an example circuit of the SC protection using 1-shunt resistor. The line current on the N side DC-ink is detected and the protective operation signal is passed through the RC filter. If the current exceeds the SC reference level, all the gates of the N-side three-phase IGBTs are switched to the OFF state and the F_O fault signal is transmitted to MCU. Since SC protection is non-repetitive, IGBT operation should be immediately halted when the F_O fault signal is given.

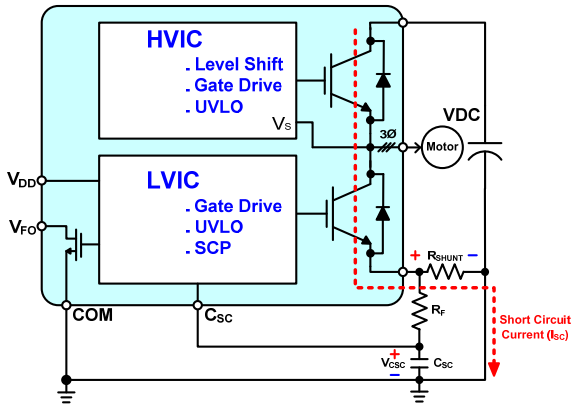


Figure 25. Short Circuit Current Protection Circuit with One Shunt Resistor

6.2.1. The value of shunt resistor is calculated by the following equation.

- Maximum SC current trip level: $I_{SC(max)}$=1.5 * I_C (rated current)
- SC trip referenced voltage: V_{SC}=min. 0.45 V, typ. 0.5 V, max. 0.55 V
- Shunt resistance : $I_{SC(max)}=V_{SC(max)}/R_{SHUNT(min)} \rightarrow R_{SHUNT(min)}=V_{SC(max)}/I_{SC(max)}$
- If the deviation of shunt resistor should is limited below ±5%,

$R_{SHUNT(typ)}=R_{SHUNT(min)}/0.95, R_{SHUNT(max)}=R_{SHUNT(typ)}*1.05$

- Actual SC trip current level becomes:

$I_{SC(typ)}=V_{SC(typ)}$ / $R_{SHUNT(min)}$, $I_{SC(min)}$ = $V_{SC(min)}$ / $R_{SHUNT(max)}$

- Inverter output power:

$P_{OUT} = \sqrt{3} \times \mathbf{VO,LL} \times \mathbf{I_{O(RMS)}} \times \mathbf{PF}$

Where:

$V_{O,LL}=\frac{\sqrt{3}}{\sqrt{2}} \times \mathbf{MI} \times \frac{\mathbf{V_{DC}}}{\mathbf{2}}$

I(O)RMS = Maximum load current of inverter; and

MI = Modulation Index;

VDC = DC link voltage;

PF = Power Factor

- Average DC Current

$I_{DC\_AVG} = V_{DC\_Link} / (P_{out} \times Eff)$

Where:

Eff = Inverter Efficiency

- The power rating of shunt resistor is calculated by the following equation.

$P_{SHUNT} = (I^2_{RMS} * R_{SHUNT} * Margin) / De\text{-}rating\ Ratio$

Where:

Shunt resistor typical value at T_C=25°C (R_{SHUNT})

De-rating ratio of shunt resistor at T_{SHUNT}=100°C (From datasheet of shunt resistor)

Safety margin (Determine by customer)

6.2.2. The value of shunt Resistor calculation Examples:

- DUT: FNB33060T
- Tolerance of shunt resistor: ±5%
- SC Trip Reference Voltage:
- $V_{SC(min)}$ = 0.45 V, $V_{SC(typ)}$ = 0.50 V, $V_{SC(max)}$ = 0.55 V
- Maximum Load Current of Inverter (I_{RMS}): 21 A_{rms}
- Maximum Peak Load Current of Inverter ($I_{C(max)}$): 45 A
- Modulation Index(MI): 0.9
- DC Link Voltage(V_{DC_Link}): 300 V
- Power Factor (PF): 0.8
- Inverter Efficiency(Eff): 0.95
- Shunt Resistor Value at T_C = 25°C (R_{SHUNT}): 11.0 mΩ
- De-rating Ration of Shunt Resistor at T_{SHUNT} = 100°C: 70% (refer to Figure 26)
- Safety Margin: 20%

6.2.3. Calculation Results:

- $I_{SC(max)}$: 1.5 * $I_{C(max)}$ = 1.5 * 30 A = 45 A
- $R_{SHUNT(typ)}$: $V_{SC(typ)}$ / $I_{SC(max)}$ = 0.50 V / 45 A = 11.0 mΩ
- $R_{SHUNT(max)}$: $R_{SHUNT(typ)}$ * 1.05 = 11 mΩ *1.05 A = 11.55 mΩ
- $R_{SHUNT(min)}$: $R_{SHUNT(typ)}$ * 0.95 = 11 mΩ *0.95 A = 10.45 mΩ
- $I_{SC(min)}$: $V_{SC(min)}$ / $R_{SHUNT(max)}$ = 0.45 V / 11.55 mΩ = 38.96 A
- $I_{SC(max)}$: $V_{SC(typ)}$ / $R_{SHUNT(min)}$ = 0.55 V / 10.45 mΩ = 52.6 A
- $P_{OUT} = \sqrt{3} \times \left(\frac{\sqrt{3}}{\sqrt{2}} \times MI \times \frac{V_{DC}}{2}\right) \times I_{(0)RMS} \times PF = \frac{3}{\sqrt{2}} \times 0.9 \times (300/2) \times 21 \times 0.8$ = 4,811 W
- I_{DC_AVG} = (P_{OUT}/Eff) / V_{DC_Link} = 16.88 A
- P_{SHUNT} = ($I^2_{DC\_AVG} \times R_{SHUNT} \times$ Margin) / De-rating Ratio = ($16.88^2 \times 0.012 \times 1.2$) / 0.7 = 5.86 W (therefore, the proper power rating of shunt resistor is over 6.0 W).

When over-current events are detected, the 600 V Motion SPM®3 version 6 series shuts down all low-side IGBTs and sends out the fault-out (F_O) signal. Fault-out pulse width is fixed; minimum value is 50 μs.

To prevent malfunction, it is recommended that an RC filter be inserted at the C_{SC} pin. To shut down IGBTs within 3 μs when over-current situation occurs, a time constant of 1.5 ~ 2 μs is recommended.

Table 13 shows the shunt resistance and typical short-circuit protection current

Table 13. Over-Current(OC) Protection Trip Level

Device	R_{SHUNT}	OC Trip Level	Remark
FNB33060T	11 mΩ	45 A	It is typical value
FNB34060T	8.3 mΩ	60 A	
FNB35060T	6.7 mΩ	75 A	

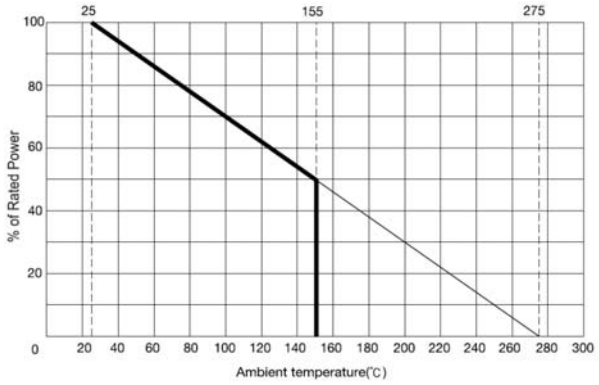


Figure 26. De-rating Curve Example of Shunt Resistor (from RARA Elec.)

6.3. Time Constant of Internal Delay

An RC filter is prevents noise-related Short-Circuit Current Protection (SCP) circuit malfunction. The RC time constant is determined by the applied noise time and the Short-Circuit Current Withstanding Time (SCWT) of SPM3 version6 series.

When the R_{SC} voltage exceeds the SCP level, this is applied to the CSC pin via the RC filter. The RC filter delay (T1) is the time required for the CSC pin voltage to rise to the referenced SCP level. The LVIC has an internal filter time (logic filter time for noise elimination: T2, around 0.7 μs). Consider this filter time when designing the RC filter of V_{CSC}

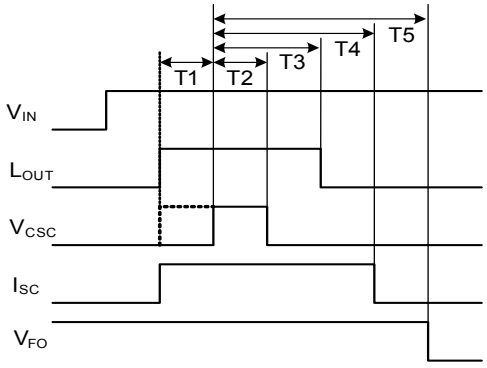


Figure 27. Timing Diagram

Notes:

29. V_{IN}: Voltage of input signal.
30. LOUT: VGE of low-side IGBT.
31. VCSC: Voltage of CSC pin.
32. ISC: Short-circuit current.
33. VFO: Voltage of VFO pin.
34. T1: filtering time of RC filter of VCSC.
35. T2: filtering time of CSC. If VCSC width is less than T2, SCP does not operate.
36. T3: delay from CSC triggering to gate-voltage down.
37. T4: delay from CSC triggering to short-circuit current.
38. T5: delay from CSC triggering to fault-out signal.

Figure 28 shows operating waveform of SCP (Short-circuit Current Protection) function. Normally, τ(time constant of RC filter of C_{SC}) don't accurately operate due to fast di/dt of I_{SC} (short-circuit current). Therefore, we should consider this kind of situation when decide time constant of RC filter of C_{SC}. (Normally, τ (time constant of RC filter of C_{SC}) accurately operates in Over-Current Protection operation (OCP).

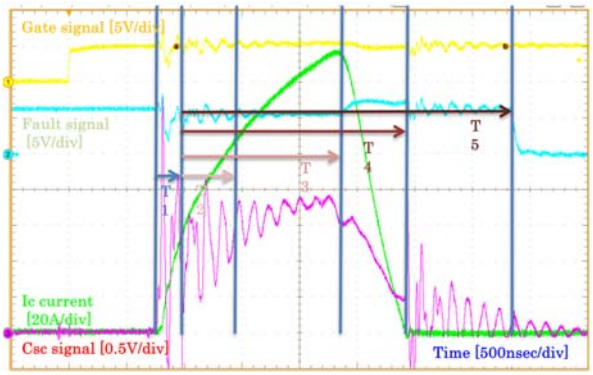


Figure 28. Short Circuit Waveform (FNB33060T, Ref. Condition: V_{DD}=16.5 V, V_{DC}=400 V, T_J=25°C)

Table 14 shows actual real time at short circuit current protection. Each time sections have a distribution, so we have to consider of distribution

Table 14. Time Table on Short Circuit Conditions; V_{CSC} to L_{OUT}, I_{SC}, V_{FO}

Device	Typ. at T_J=25°C	Typ. at T_J=150°C	Max. at T_J=25°C
FNB33060T	T2=0.80μs	T2=0.52μs	Considering ±20% Distribution, T3 and T4
	T3=1.35μs	T3=1.23μs	
	T4=1.95μs	T4=1.81μs	
	T5=2.86μs	T5=2.47μs	

Notes:

39. To guarantee safe short-circuit protection under all operating conditions, CSC should be triggered within 1.0μs after short-circuit occurs. (Recommendation: SCWT < 3.0μs, Conditions: VDC=400V, VDD=16.5 V, TJ=150°C).
40. It is recommended that delay from short-circuit to C_{SC} triggering should be minimized.

6.4. Fault Output Circuit

Because V_{FO} terminal is an open-drain type; it should be pulled up via a pull-up resistor. The resistor must satisfy the above specifications.

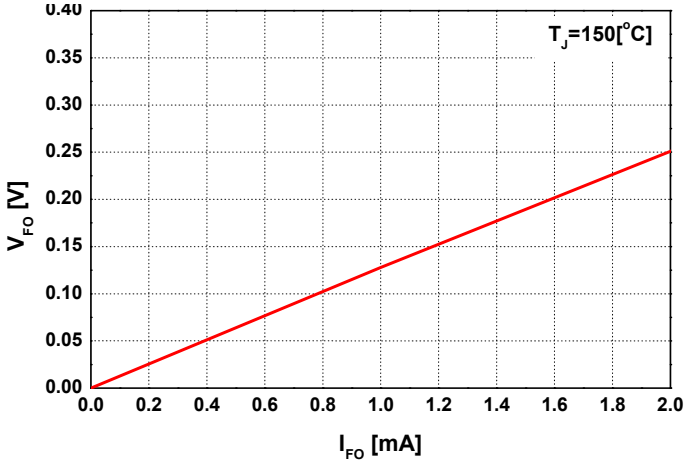


Figure 29. Voltage-Current Characteristics of V_{FO} Terminal

6.5. Bootstrap Circuit Design

6.5.1. Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between $V_{B(U,V,W)}$ and $V_{S(U,V,W)}$, provides the supply to the HVIC within the 600V SPM®3 series. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high-side IGBT. The SPM3 series includes an under-voltage lock out protection function for the V_{BS} to ensure that the HVIC does not drive the high-side IGBT, if the V_{BS} voltage drops below a specified voltage. This function prevents the IGBT from operating in a high dissipation mode. There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 30). This method has the advantage of being simples and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap to ground (either through the low-side or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{DD} supply

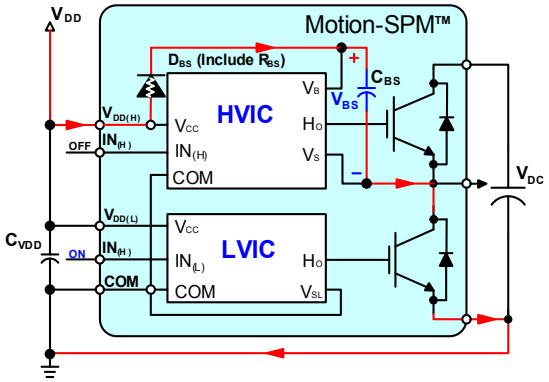


Figure 30. Current Path of Bootstrap Circuit

6.5.2. Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on-time of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln \frac{V_{DD}}{V_{DD} - V_{BS(min)} - V_F - V_{LS}} \quad (1)$$

Where:

V_F = Forward voltage drop across the bootstrap diode;

$V_{BS(min)}$ =The minimum value of the bootstrap capacitor;

V_{LS} = Voltage drop across the low-side IGBT or load; and

Δ = Duty ratio of PWM.

When the bootstrap capacitor is charged initially; V_{DD} drop voltage is generated based on initial charging method, V_{DD} line SMPS output current, V_{DD} source capacitance, and bootstrap capacitance. If V_{DD} drop voltage reaches UV_{DDD} level, the low side is shut down and a fault signal is activated.

To avoid this malfunction, related parameter and initial charging method should be considered. To reduce V_{DD} voltage drop at initial charging, a large V_{DD} source capacitor and selection of optimized low-side turn-on method are recommended. Adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts.

Figure 31 shows an example of initial bootstrap charging sequence. Once V_{DD} establishes, V_{BS} needs to be charged by turning on the low-side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency.

Therefore, it is desired to maintain this structure without creating complementary high-side PWM signals. The capacitance of V_{DD} should be sufficient to supply necessary charge to V_{BS} capacitance in all three phases. If a normal PWM operation starts before VBS reaches VUVLO reset level, the high-side IGBTs

cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over-current protection level.

Therefore, initial charging time for bootstrap capacitors should be separated, as shown in Figure 32. The effect of the bootstrap capacitance factor and charging method (low-side IGBT driving method) is shown in Figure 30.

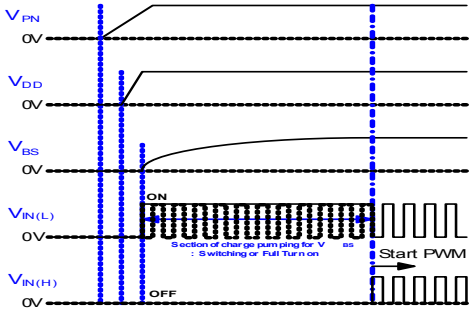


Figure 31. Timing Chart of Initial Bootstrap Charging

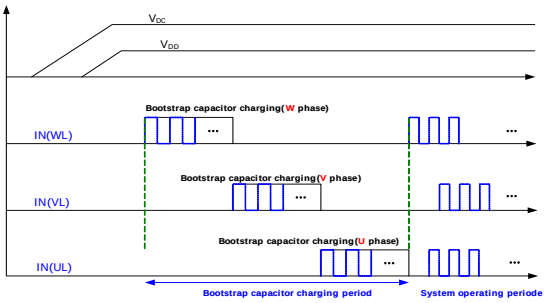


Figure 32. Recommended Initial Bootstrap Capacitors Charging Sequence

Figure 33 and Figure 34 shows waveform initial bootstrap capacitor charging voltage and current.

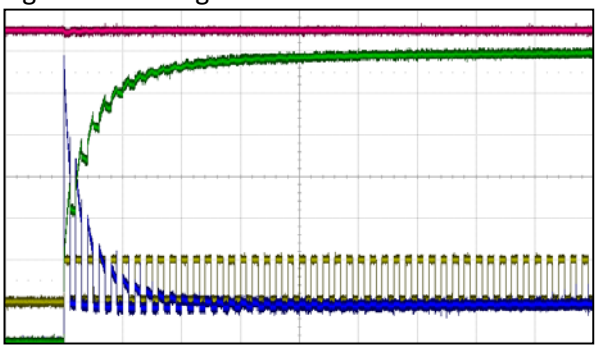


Figure 33. Each Part Initial Operating Waveform of Bootstrap Circuit (Conditions: V_{DC}=300 V, V_{DD}=15 V, C_{BS}=22 µF, LS IGBT Turn-on Duty=200 µsec)

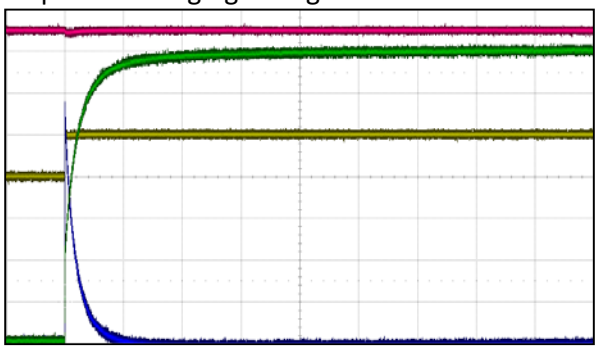


Figure 34. Each Part Operating Waveform of Bootstrap Circuit (Conditions: V_{DC}=300 V, V_{DD}=15 V, C_{BS}=22 µF, LS IGBT Full Turn-on)

6.5.3. Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} \qquad (2)$$

Where:

Δt: maximum on pulse width of high-side IGBT;

ΔVBS: the allowable discharge voltage of the CBS (voltage ripple); and

ILeak: maximum discharge current of the C_{BS}.

Mainly via the following mechanisms:

- Gate charge for turning the high-side IGBT on.
- Quiescent current to the high-side circuit in HVIC.
- Level-shift charge required by level-shifters in HVIC.
- Leakage current in the bootstrap diode.
- C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors).
- Bootstrap diode reverse recovery charge.

Practically, 4.5mA of ILeak is recommended for the 600V SPM3 version 6 series. By considering dispersion and reliability, the capacitance is generally selected to be 2~3 times the calculated one. The CBS is only charged when the high-side IGBT is off and the VS(x) voltage is pulled down to ground.
The on-time of the low-side IGBT must be sufficient to for the charge drawn from the CBS capacitor to be fully replenished. This creates an inherent minimum on-time of the low-side IGBT (or off-time of the high-side IGBT).

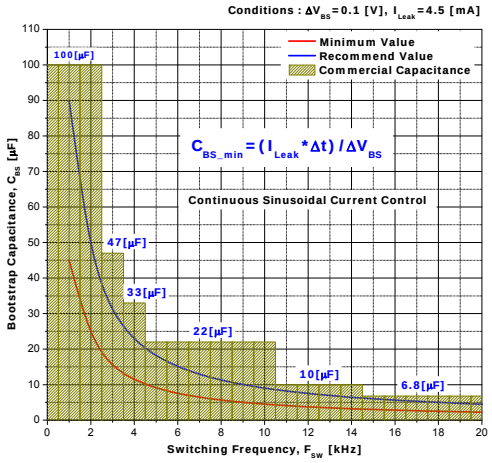


Figure 35. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔV_{BS}.

- I_{Leak}: circuit current = 4.5mA (recommended value)
- ΔV_{BS}: discharged voltage = 1.0 V (recommended value)
- Δt: maximum on pulse width of high-side IGBT = 0.2 ms (depends on application)

$$C_{BS\_min} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} = \frac{2mA \times 4.5ms}{1.0V} = 9.0 \times 10^{-6}$$

→ More than 2 times → 18μF.

Note:

41. The capacitance value can be changed according to the switching frequency, the capacitor selected, and the recommended V_{BS} voltage of 13.0~18.5 V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of the component.

6.5.4. Built-in Bootstrap Diode

When the high-side IGBT or diode conducts, the bootstrap diode (D_{BS}) supports the entire bus voltage. Hence, a diode with withstand voltage of more than 600 V is recommended. It is important that this diode has a fast recovery (recovery time < 100 ns) characteristic to minimize the amount of charge fed back from the bootstrap capacitor into the V_{DD} supply. The bootstrap resistor (R_{BS}) is to slow down the dV_{BS}/dt and limit initial charging current (I_{charge}) of bootstrap capacitor.
Normally, a bootstrap circuit consists of bootstrap diode (D_{BS}), bootstrap resistor (R_{BS}), and bootstrap capacitor (C_{BS}). As shown in Figure 36, the built-in bootstrap diode of SPM®3 version 6 product has special V_F characteristics to be used without additional bootstrap resistor. Therefore, only external bootstrap capacitors are needed to make bootstrap circuit.
The characteristics of the built-in bootstrap diode in the SPM3 products are:

- Fast recovery diode: 600 V/0.5 A
- t_{rr}: 80 ns (typical)
- Resistive characteristic: equivalent resistor of approximately 15 Ω

Error! Reference source not found. shows the absolute maximum ratings of bootstrap diode. **Error! Reference source not found.** shows forward voltage drop and reverse recovery characteristic of the bootstrap diode.

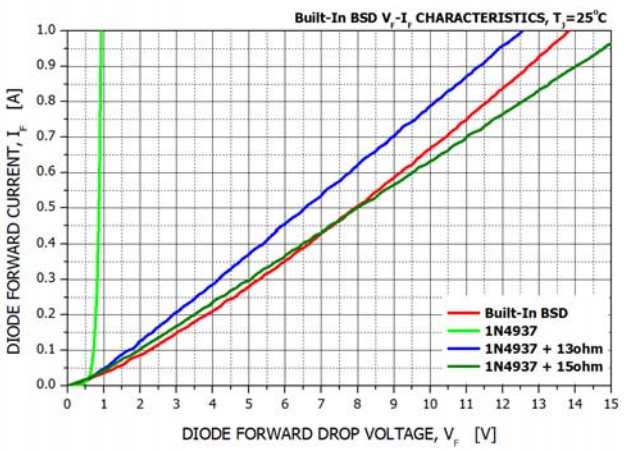


Figure 36. V-I characteristics of Bootstrap Diode in SPM3 Series products

7. Print Circuit Board (PCB) Design

7.1. General Application Circuit Example

Figure 37 shows a general application circuitry of interface schematic with control signals connected directly to a MCU. Figure 38 shows guidance of PCB layout for the 600V SPM®3 version 6 series.

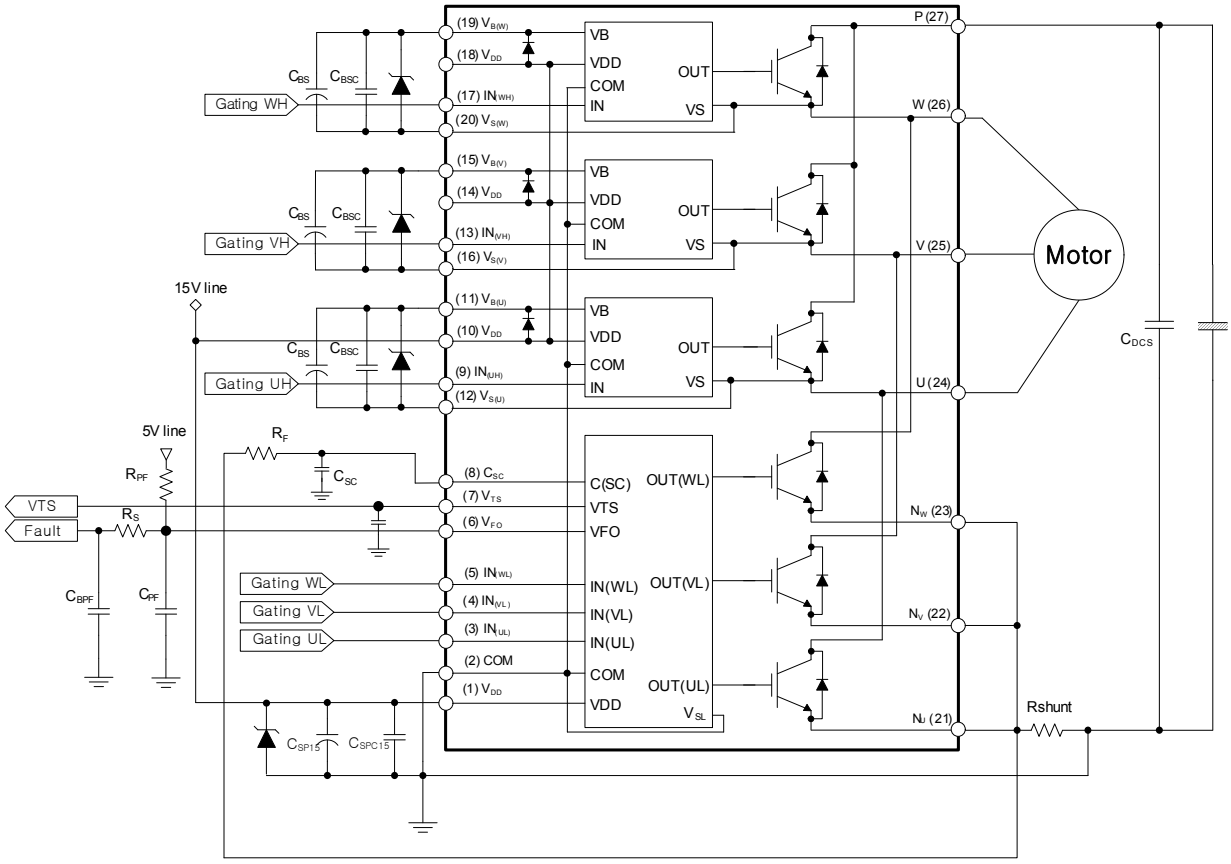


Figure 37. General Application Circuitry for 600V Motion SPM 3 Version 6

7.2. PCB Layout Guidance

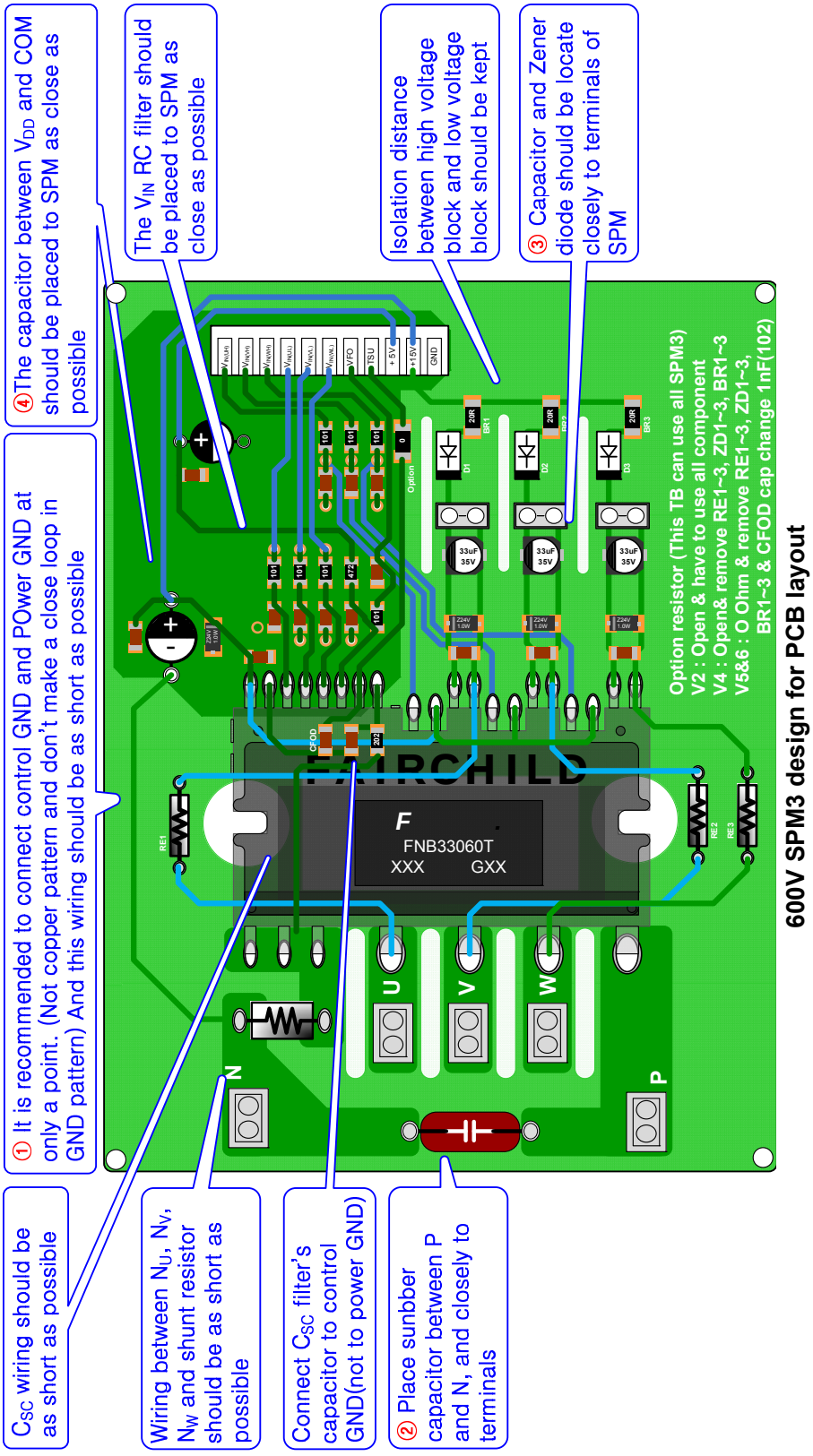
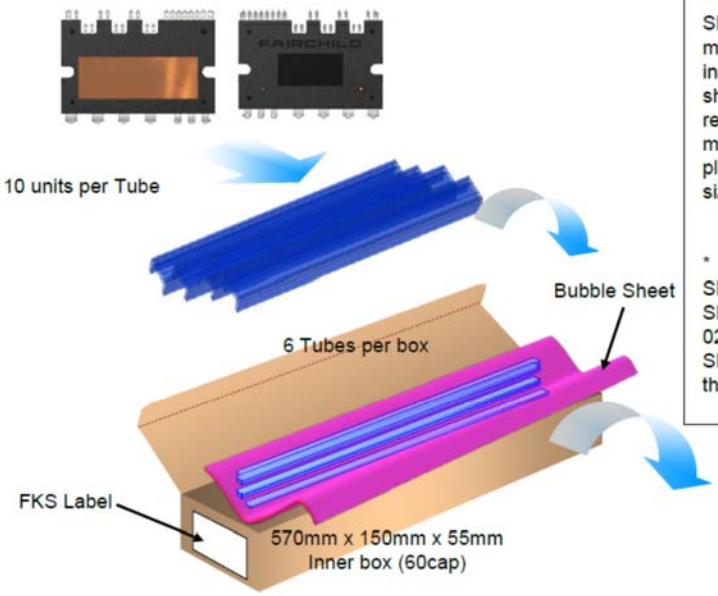


Figure 38. Print Circuit Board (PCB) Layout Guidance for the 600 V Motion SPM®3

8. Packing Information

SPMCA-027 Tube Packing Configuration: Figure 1.0



Packaging Description:

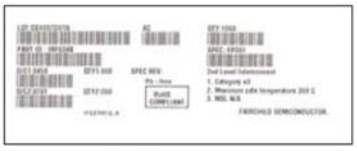
SPMCA-027 parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent.These tubes in standard option are placed inside a dissipative plastic bubble sheet, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains six tubes maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.

* SPMCC-027, SPMCD-027, SPMCE-027, SPMCF-027, SPMCG-027, SPMEA-027, SPMEC-027, SPMGA-027, SPMGC-027, SPMHA-027, SPMHC-027, SPMIA-027, SPMIC-027, SPMMA-027, SPMMB-027, SPMPA-027, SPMQA-027, SPMQB-027, SPMRA-027, SPMRB-027 packages also use this packing spec.

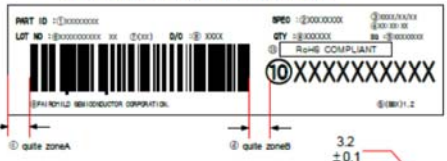
SPMCA-027 Packaging Information: Figure 2.0

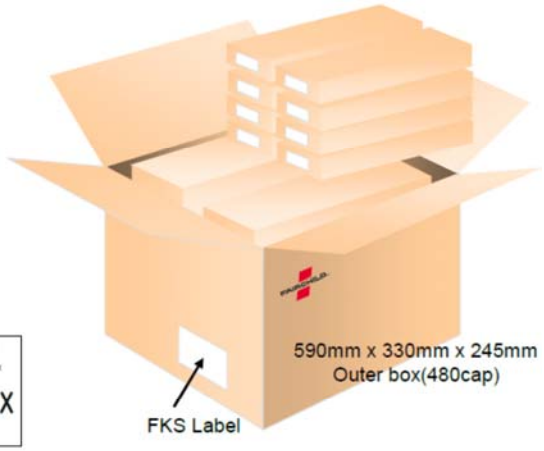
SPMCA-027 Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	10
Inner Box Dimension (mm)	570x150x55
Max qty per Box	60
Outer Box Dimension (mm)	590x330x245
Max qty per Box	480
Weight per unit (gm)	-
Note/Comments	

Inner Box Barcode Label Sample

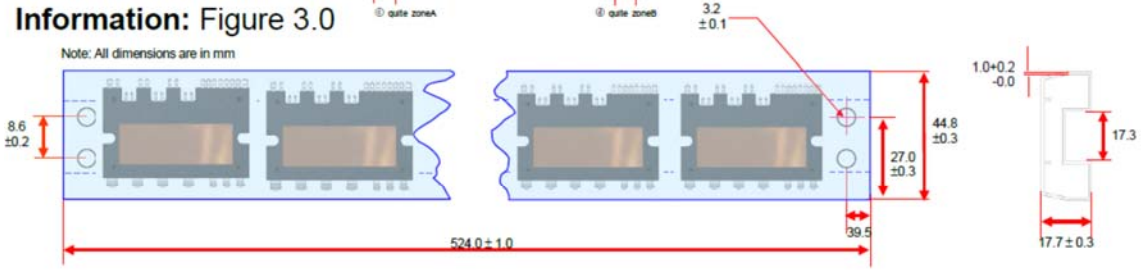


Outer Box Barcode Label Sample





SPMCA-027 Tube Information: Figure 3.0



NOTES:

A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

B : DRAWING FIEL NAME : PKG-MOD27BAREV2

Figure 39. Packing Information

Related Resources

FNB33060T Product Folder

AN-9086 — 600V SPM®3 Series Mounting Guidance

RD-572 — 600V SPM®3 ver6 series Reference Design Guide

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative