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AN-9111

Smart Power Module, Motion SPM® 45 LV series User's Guide

Table of Contents

1. Introduction

This application note supports the Motion SPM® 45 LV-series. It should be used in conjunction with Motion SPM 45 LV datasheets, and Motion SPM design reference *(RD-408).*

1.1. Design Concept

The key design objective of the SPM 45 LV series is to provide a compact and reliable inverter solution for small power motor drive applications. Ongoing efforts have improved the performance, quality, and power rating of SPM 45 LV series products.

The MOSFETs in SPM 45 LV series are specially processed to reduce the amount of body-diode reverse recovery charge to minimize the switching loss and enable fast switching operations. Softness of the reverse-recovery characteristics is managed through advanced MOSFET design with optimized gate resistor selections to contain Electromagnetic Interference (EMI) noise within a reasonable range.

SPM 45 LV series has six fast-recovery MOSFETs (FRFET®), LVIC and three-in-one HVIC. An FRFET-based power module has much better ruggedness and a larger Safe Operation Area (SOA) than MOSFET-based module or Silicon-On-Insulator modules.

The FRFET-based power module has a big advantage in light-load efficiency because the voltage drop across the transistor decreases linearly as current decrease. Some applications require continuous operation at light load except short transients and improving the efficiency in the light-load condition is the key to saving energy. Refrigerators, water circulation pumps, and some fans are good examples.

Motion SPM 45 LV series achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are invert motor drives for industrial use, such as general-purpose inverters, power tool and servo motors.

1.2. Key Features

- UL Certified No.E209204 (UL1557)
- 40 V, Low $R_{DS(ON)}$ 3-Phase MOSFET Inverter Module with Gate Drivers and Protection
- Low Thermal Resistance Using Ceramic Substrate
- Three Separate Open-Emitter Pins from Low-Side MOSFETs for Three-Leg Current Sensing
- Single-Grounded Power Supply for Built-in HVIC
- Isolation Rating: 800 V_{RMS} / min

Figure 1. Package Outline of Motion SPM 45 LV Series

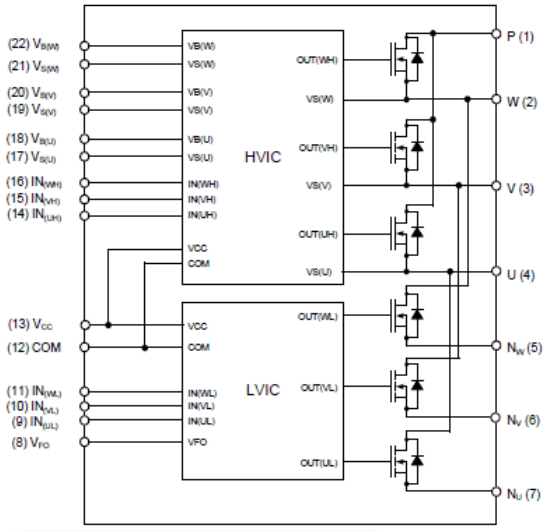


Figure 2. Internal Equivalent Circuit, Input / Output Pins

2. Product Selections

2.1. Ordering information

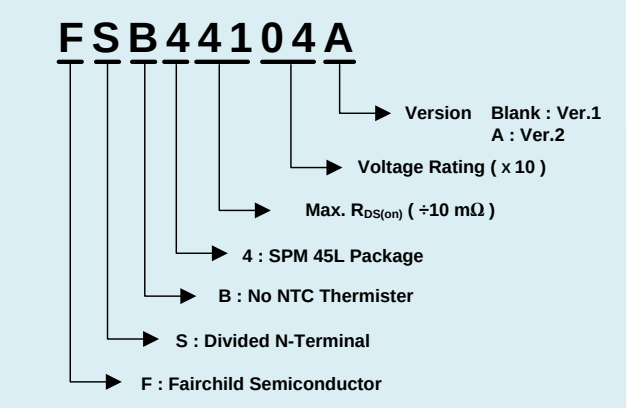


Figure 3. Ordering Information of SPM® 45 LV Series

2.2. Product Line-up

Table 1 shows the basic line up. Online loss & temperature simulation tool, Motion Control Design Tool (Motion-Control-Design-Tool), is recommended to find out the right SPM product for the desired application.

Table 1. Product Line-up

Target Application	Fairchild Device	MOSFET Rating	Motor Rating(Error! Reference source not found.)	Isolation Voltage
Small-Power Inverter, Power Tool	FSB44104A	40 A / 40 V	0.8 kW	V_{ISO} = 800 V_{RMS} (Sine 60 Hz, 1 min. Between all shorted pins and heat sink)
	FSB43004A	60 A / 40 V	1.2 kW	

Note:
1. These motor ratings are general ratings, so may be changed by conditions.

3. Package

Since heat dissipation is an important factor that limits the power module's current capability, the heat dissipation characteristics are critical in determining the SPM package performance. A trade-off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to a good package technology lies in the accomplishment of optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In the SPM package, technology was developed in which bare ceramic with good heat dissipation characteristics is attached directly to the lead frame. This technology already applied in SPM, but was improved through new adhesion methods. This made it possible to achieve improved reliability and heat dissipation, while maintaining cost effectiveness.

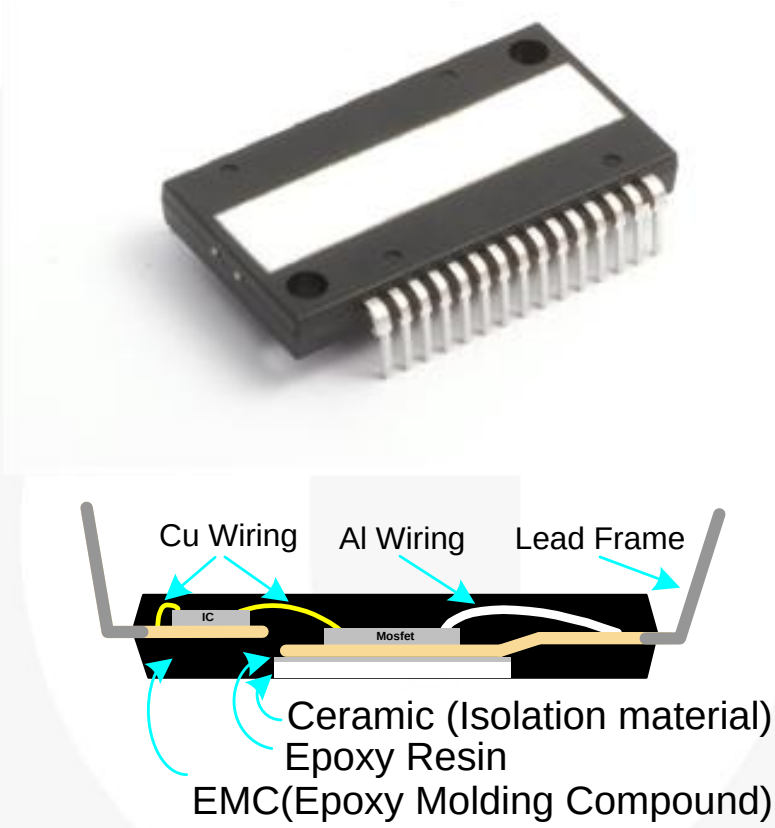


Figure 4. Vertical Structure of SPM Package

3.1. Pin Description

Figure 5 shows the location of pins, the name and dummy pins of SPM 45 LV series.

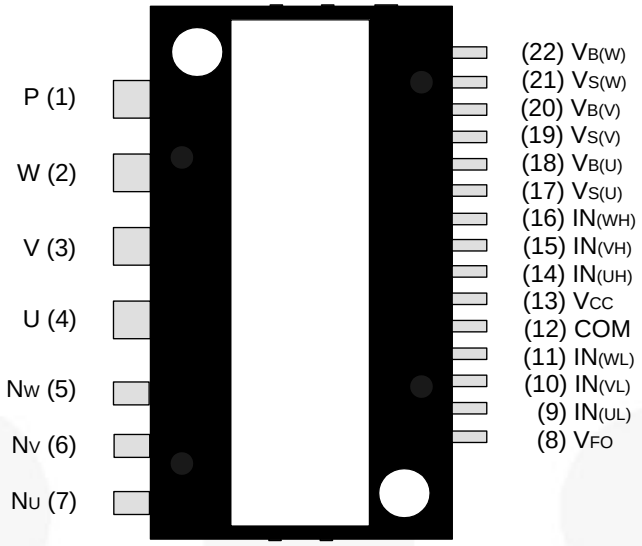


Figure 5. Package Top-View and Pin Assignment

The detail functional descriptions are provided in Table 2.

Table 2. Pin Description

Pin Number	Name	Description
1	P	Positive DC-Link Input
2	W	W Phase Output
3	V	V Phase Output
4	U	U Phase Output
5	N_W	Negative DC-Link Input
6	N_V	Negative DC-Link Input
7	N_U	Negative DC-Link Input
8	V_{FO}	Fault Output
9	$IN_{(UL)}$	PWM Input for Low-Side U-Phase MOSFET Drive
10	$IN_{(VL)}$	PWM Input for Low-Side V-Phase MOSFET Drive
11	$IN_{(WL)}$	PWM Input for Low-Side W-Phase MOSFET Drive
12	COM	Common Supply Ground
13	V_{CC}	Common Supply Voltage for IC and Low-side MOSFET Drive
14	$IN_{(UH)}$	PWM Input for High-Side U-Phase MOSFET Drive
15	$IN_{(VH)}$	PWM Input for High-Side V-Phase MOSFET Drive
16	$IN_{(WH)}$	PWM Input for High-Side W-Phase MOSFET Drive
17	$V_{B(U)}$	Supply Voltage for High-Side U-Phase MOSFET Drive
18	$V_{S(U)}$	Supply Ground for High-Side U-Phase MOSFET Drive
19	$V_{B(V)}$	Supply Voltage for High-Side V-Phase MOSFET Drive
20	$V_{S(V)}$	Supply Ground for High-Side V-Phase MOSFET Drive
21	$V_{B(W)}$	Supply Voltage for High-Side W-Phase MOSFET Drive
22	$V_{S(W)}$	Supply Ground for High-Side W-Phase MOSFET Drive

3.2. Detailed Pin Definition and Notification

- **High-Side Bias Voltage Pins for Driving the MOSFET / High-Side Bias Voltage Ground Pins for Driving the MOSFET**

Pin: $V_{B(U)}$-$V_{S(U)}$, $V_{B(V)}$-$V_{S(V)}$, $V_{B(W)}$-$V_{S(W)}$

- These are drive power supply pins for providing gate drive power to the high-side MOSFETs.
- The external power supplies don't need for the high side MOSFET driving by using bootstrap circuit..
- Each bootstrap capacitor is charged from the V_{CC} supply during ON state of the corresponding low-side MOSFET.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a low-ESR, low-ESL filter capacitor should be mounted very close to these pins.

- **Low-Side Bias Voltage Pin / High-Side Bias Voltage Pins:**

Pin: V_{CC}

- These are control supply pins for the built-in ICs.
- This pin should be connected externally.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a low-ESR, low-ESL filter capacitor should be mounted very close to these pins.

- **Low-Side Common Supply Ground Pins**

Pin: COM

- The common (COM) pin connects to the control ground for the internal ICs.
- Important! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin.

- **Signal Input Pins**

Pin: $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$

- These pins control the operation of the built-in MOSFETs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt-trigger circuit composed of 5 V-class CMOS.
- The signal logic of these pins is active HIGH. The MOSFETs associated with each of these pins are turn-on when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the Motion SPM® 45 LV series against noise influences.
  To prevent signal oscillations, an RC coupling as illustrated in Figure 16 is recommended.

- **Fault Output Pin**

Pin: V_{FO}

- This is the fault output alarm pin. An active LOW output is given on this pin for a fault state condition in the SPM.
- The alarm condition is: low-side bias Under-Voltage Lockout (UVLO).
- The VFO output is open drain configured. The V_{FO} signal line should be pulled to the 5 V logic power supply with approximately 4.7 kΩ resistance.

- **Positive DC-Link Pin**

Pin: P

- This is the DC-link positive power supply pin of the inverter.
- It is internally connected to the drains of the high-side MOSFETs.
- To suppress surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (tip: metal film capacitor is typically used).

- **Negative DC-Link Pins**

Pin: NU, NV, NW

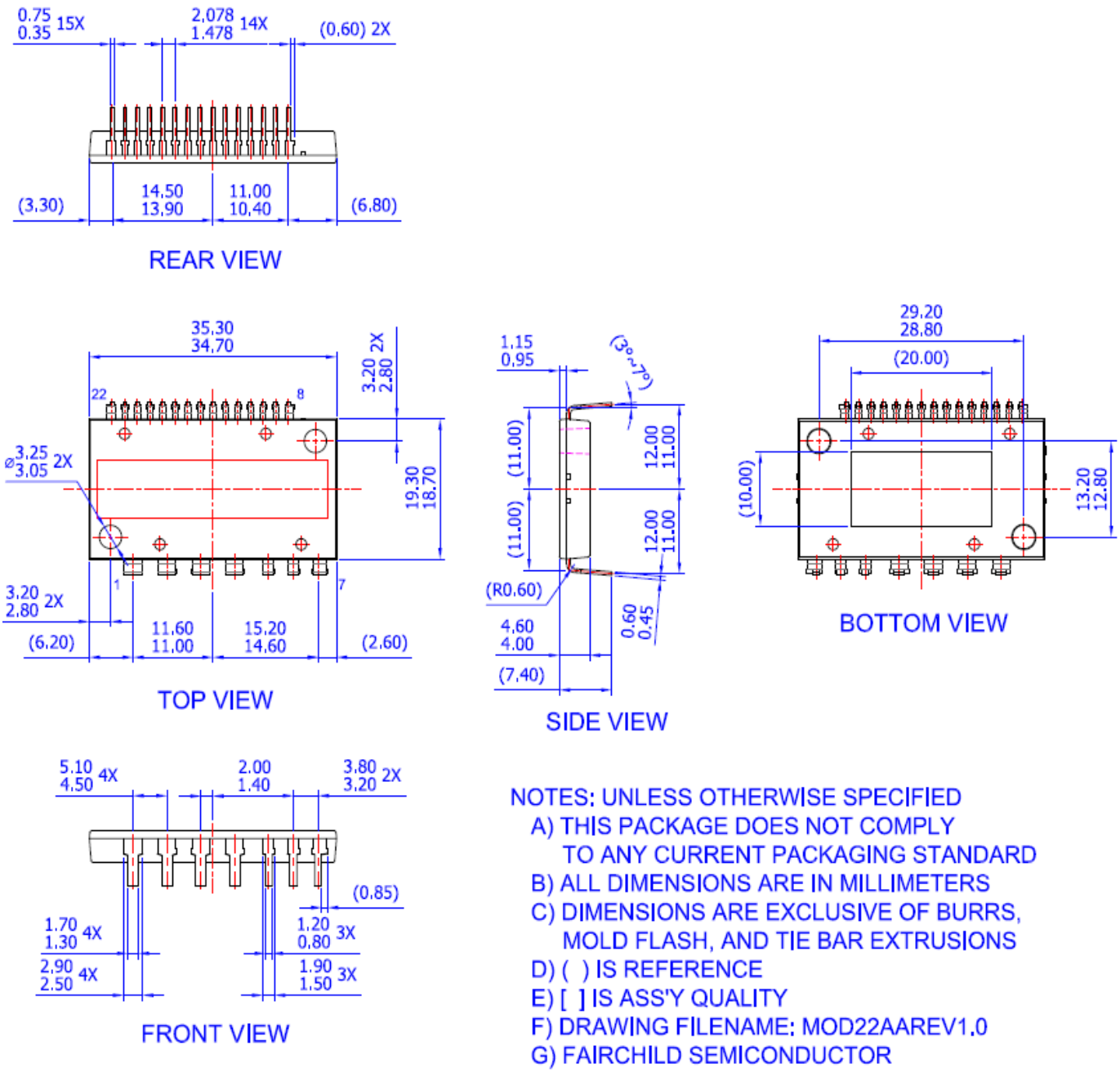
- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side MOSFET source of the each phase.
- These pins are used in connection with one shunt or three shunt resistor

- **Inverter Power Output Pins**

Pin: U, V, W

- Inverter output pins for connecting to the inverter load (e.g. motor).

3.3. Package Outline



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) ( ) IS REFERENCE
E) [ ] IS ASS'Y QUALITY
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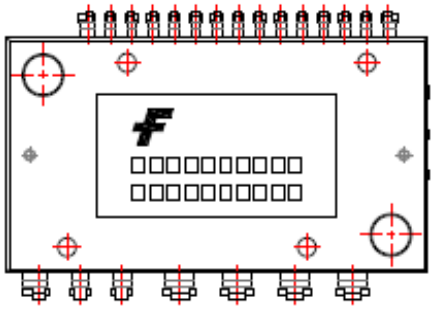
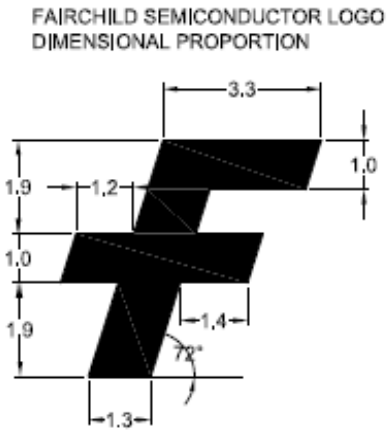
G) FAIRCHILD SEMICONDUCTOR

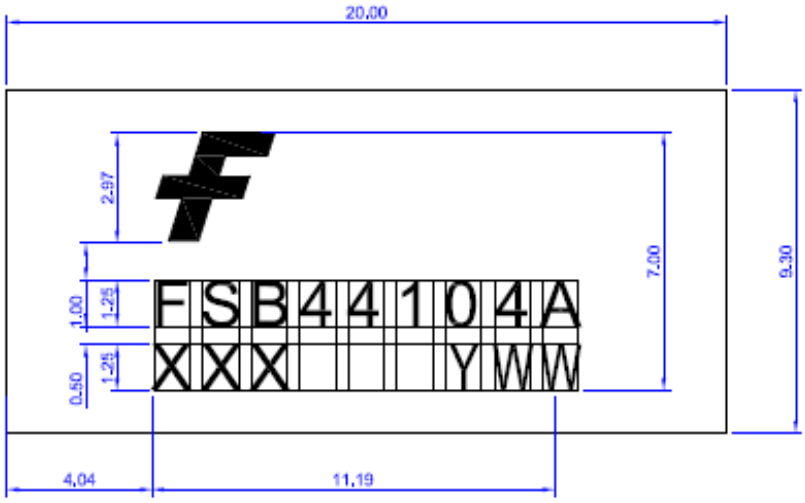
3.4. Marking Specification

* MARKING LAY-OUT





* MARKING DIMENSION



X	Alphabet
2010	A
2011	B
2012	C
2013	D
2014	E
2015	F
2016	G
2017	H
2018	J
2019	K
2020	A

* NOTE
1. F : FAIRCHILD LOGO
2. XXX : LAST 3 DIGITS OF LOT NO(OPTION CODE)
3. YWW : WORK WEEK CODE ("Y" REFERS TO THE RIGHT ALPHABET CHARACTER TABLE)

4. Product Synopsis

This section discuss electrical specification, characteristics and mechanical characteristics

4.1. Absolute Maximum Ratings (T_J = 25°C, unless otherwise specified).

Table 3. Inverter Part

Symbol	Parameter	Conditions		Rating	Unit
V_{PN}	Supply Voltage	Applied between P –Nu, Nv,Nw		40	V
* $\pm I_D$ (2)	Each MOSFET Drain Current	T_C=25°C, $T_J \leq$ 150°C	FSB44104A	57	A
			FSB43004A	71	
* $\pm I_{CP}$ (2)	Each MOSFET Drain Current (Peak)	T_C=25°C, $T_J \leq$ 150°C, Under 1 ms Pulse Width	FSB44104A	110	A
			FSB43004A	180	
* P_D (2)	Maximum Power Dissipation	T_C=25°C, per One Chip, T_J=150°C	FSB44104A	28	W
			FSB43004A	31	
T_J	Operating Junction Temperature			-40 ~ 150	°C

Note:

2. Rating value of marking "*" is calculation value or design factor.

Table 4. Control Part

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Control Supply Voltage	Applied between V_{CC} - COM	20	V
V_{BS}	High-Side Control Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$,$V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$,	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, - COM	-0.3~V_{CC}+0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} – COM	-0.3~V_{CC}+0.3	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} Pin	1	mA

Table 5. Total System

Symbol	Parameter	Conditions	Rating	Unit
T_C	Module Case Operation Temperature	See Figure 6	-40~125	°C
T_{STG}	Storage Temperature		-40~150	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1-Minute, Connect Pins to Heat Sink	800	V_{rms}

Table 6. Thermal Resistance

Symbol	Parameter	Conditions		Max.	Unit
$R_{th(j-c)}$	Junction-to-Case Thermal Resistance (3)	Package center (per MOSFET)	FSB44104A	4.41	°C /W
			FSB43004A	3.92	

Note:

3. For the measurement point of case temperature (T_C), please refer to Figure 6.

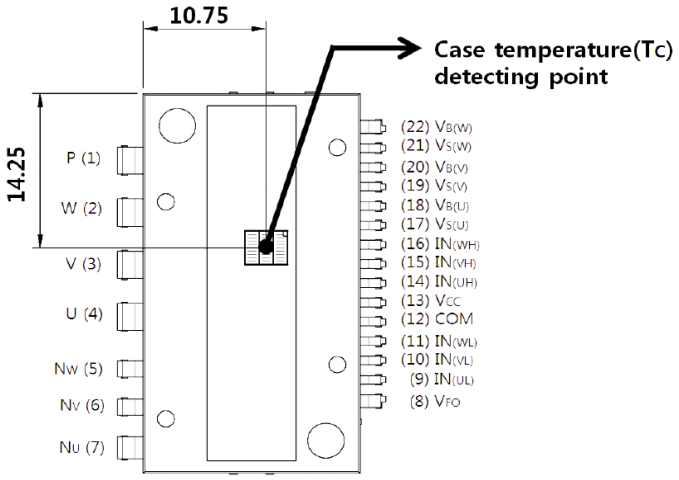


Figure 6. Case Temperature (TC) Detecting Point

4.2. Electrical Characteristic (T_J = 25°C, unless otherwise specified).

Table 7. Inverter Part (Based on FSB44104A)

Symbol		Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}		Drain–Source Breakdown Voltage	V_{IN}=0 V, I_D=250μA(4)	40			V
$R_{DS(ON)}$		Drain - Source Turn-On Resistance	V_{CC} = V_{BS} = 15 V, V_{IN} = 5 V, I_D = 40 A		3.0	4.1	mΩ
V_{SD}		Source - Drain Diode Forward Voltage	V_{CC} = V_{BS} = 15 V, V_{IN} = 0 V, I_{SD} = 40 A		0.8	1.1	V
HS	t_{ON}	Switching Times	V_{PN} = 20 V, V_{CC} = V_{BS} = 15 V, I_D = 40 A, V_{IN} = 0 V ↔ 5 V, Inductive Load, See Figure 7		1200		μs
	$t_{C(ON)}$				1140		
	t_{OFF}				1700		
	$t_{C(OFF)}$				500		
	t_{rr}				70		
	I_{rr}				5		
LS	t_{ON}				1370		
	$t_{C(ON)}$				1000		
	t_{OFF}				1850		
	$t_{C(OFF)}$				600		
	t_{rr}				75		
	I_{rr}				4		
I_{DSS}		Drain - Source Leakage Current	V_{DS}=V_{DSS}			250	μA

Note:

4. BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each MOSFET. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{DS} should not exceed BV_{DSS} in any case.

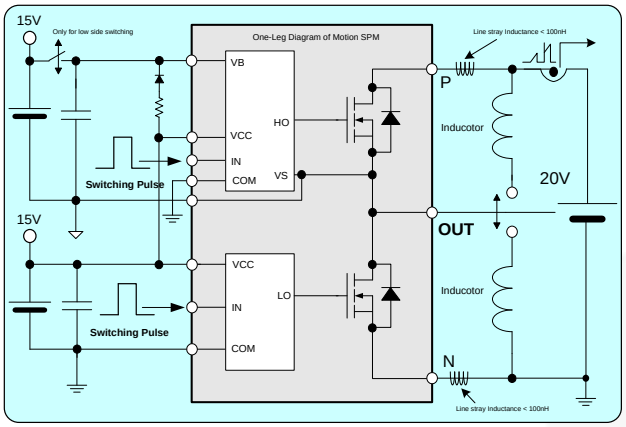


Figure 7. Switching Evaluation Circuit

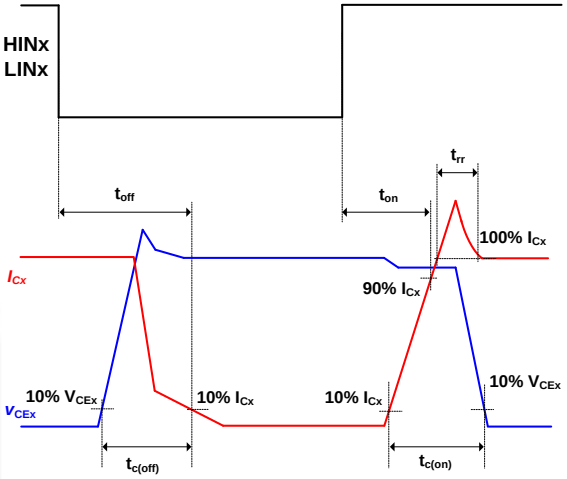


Figure 8. Switching Time Definition

Table 8. Control Part

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{QCC}	Quiescent V_{CC} Supply Current	$V_{CC(H)}$=15 V, $IN_{(UH,VH,WH)}$ = 0 V	$V_{CC(H)}$ - COM			2.75	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS}=15 V, $IN_{(UH,VH,WH)}$=0 V	$V_{B(U)} – V_{S(U)}$ $V_{B(V)} – V_{S(V)}$ $V_{B(W)} – V_{S(W)}$			0.3	mA
V_{FOH}	Fault Output Voltage	V_{CC}=15 V, V_{SC}=0 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up		4.5			V
V_{FOL}		V_{CC}=15 V, V_{SC}=1 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up				0.5	
UV_{CCD}	Supply Circuit, Under-Voltage Protection	Detection Level		7.0	8.2	10.0	V
UV_{CCR}		Reset Level		8.0	9.4	11.0	
UV_{BSD}		Detection Level		7.0	8.0	9.5	
UV_{BSR}		Reset Level		8.0	9.0	10.5	
t_{FOD}	Fault-Out Pulse Width			30			µs
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $IN_{(UH,VH,WH)}$ - COM, $IN_{(UL,VL,WL)}$ - COM				2.6	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8			

4.3. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply Voltage	Applied between P - N_U, N_V, N_W		20		V
V_{CC}	Control Supply Voltage	Applied between $V_{CC(UH,VH,WH)}$ - COM, $V_{CC(L)}$ - COM	13.5	15.0	16.5	
V_{BS}	High-Side Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	13.0	15.0	18.5	V
dV_{CC}/dt, dV_{BS}/dt	Control Supply Variation		-1		1	V/μs
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W – COM (Including Surge Voltage)	-4		4	V

4.4. Mechanical Characteristics

Parameter	Conditions	Value			Unit
		Min.	Typ.	Max.	
Device Flatness	See Figure 9			120	μm
Mounting Torque	Mounting Screw: M3	0.51	0.62	0.72	N·m
Weight	Module weight		8.4		g

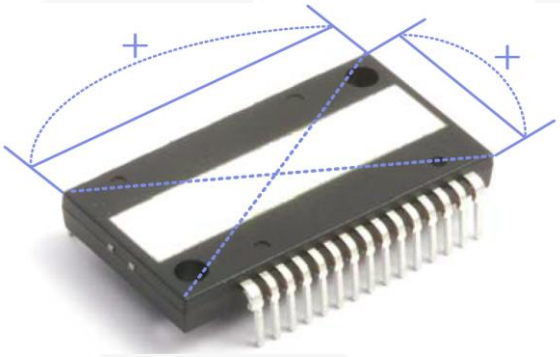


Figure 9. Flatness Measurement Position

5. Operation Sequence for Protections

5.1. Under-Voltage Lockout Protection

The LVIC has an under-voltage lockout protection (UVLO) function to protect the low-side MOSFETs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 10.

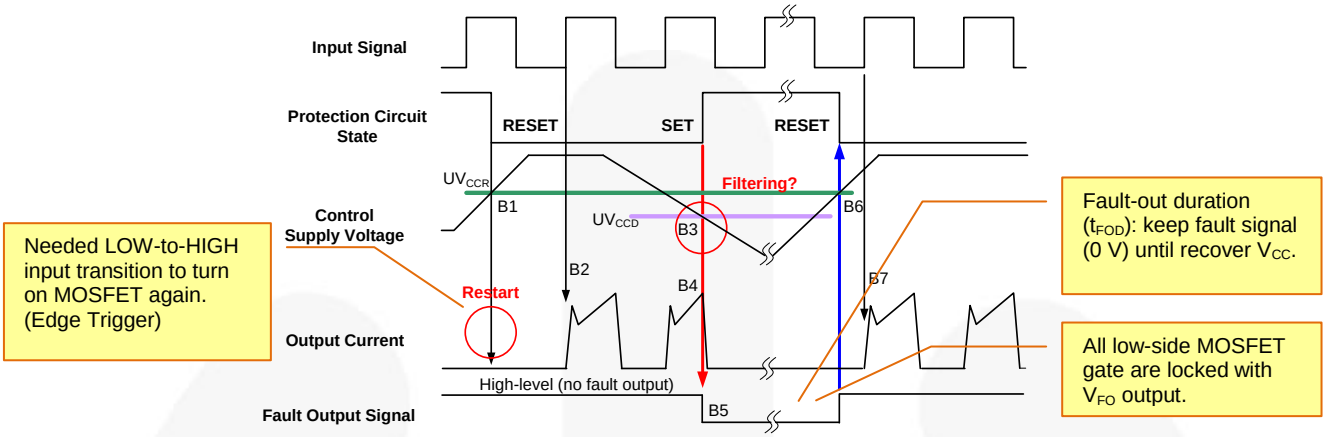


Figure 10. Timing Chart of Low-Side Under-Voltage Protection Function

Notes:

5. B1-control supply voltage rise: after the voltage rises UV_{CCR}, the circuits starts to operate when the next input is applied.
6. B2-normal operation: MOSFET ON and carrying current.
7. B3-under-voltage detection (UV_{CCD}).
8. B4-MOSFET OFF in spite of control input is alive and
9. B5-Fault output signal starts.
10. B6-under-voltage reset (UV_{CCR}).
11. B7-normal operation: MOSFET ON and carrying current..

The HVIC has an under-voltage lockout function to protect the high-side MOSFET from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 11. A fault-out (FO) alarm is not given for low HVIC bias conditions.

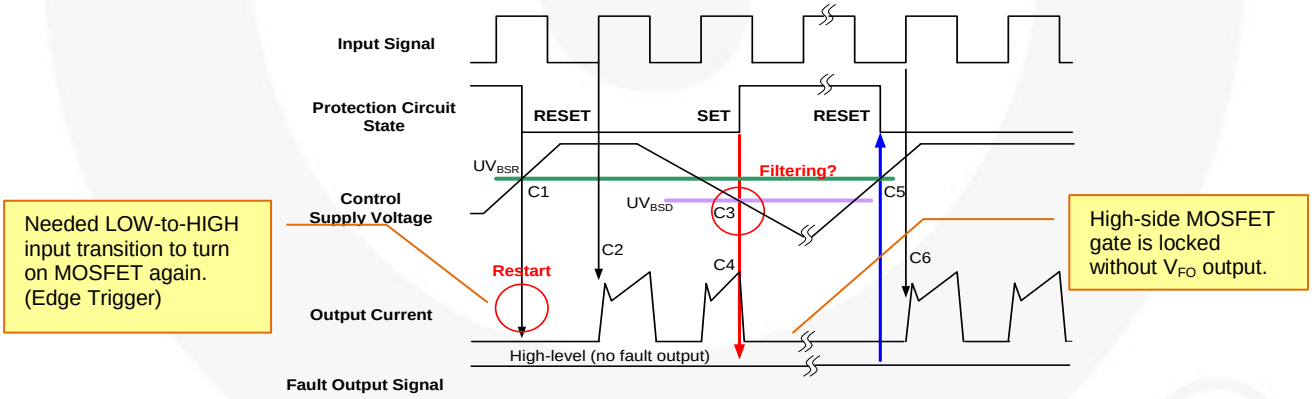


Figure 11. Timing Chart of High-Side Under-Voltage Protection Function

Notes:

12. C1-control supply voltage rises: after the voltage reaches UV_{BSR}, the circuit starts when the next input is applied.
13. C2-normal operation: MOSFET ON and carrying current.
14. C3-under-voltage detection (UV_{BSD}).
15. C4-MOSFET OFF in spite of control input is alive, but there is no fault output signal.
16. C5-under-voltage reset (UV_{BSR}).
17. C6-normal operation: MOSFET ON and carrying current.

6. Key Parameter Design Guidance

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of Motion SPM® 45 LV series.

6.1. Selection of Shunt resistor

Figure 12 shows an example circuit of the SC protection using 1-shunt resistor. The line current on the N side DC-link is detected and the protective operation signal is passed through the RC filter. If the current exceeds the SC reference level, all the gates of the N-side three-phase MOSFETs are switched to the OFF state and the F_O fault signal is transmitted to MCU. Since SC protection is non-repetitive, MOSFET operation should be immediately halted when the F_O fault signal is given.

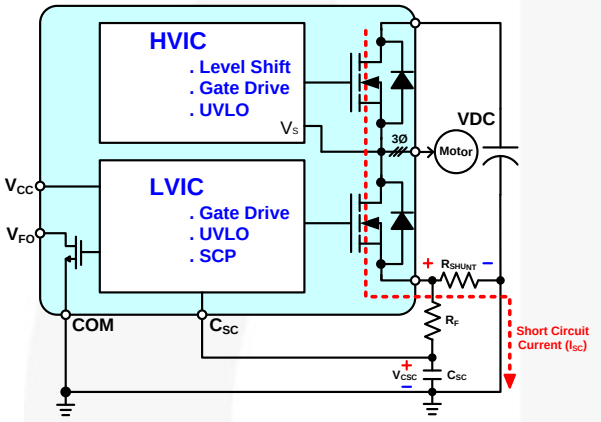


Figure 12. Short circuit current protection circuit with one shunt resistor

The value of shunt resistor is calculated by the following equation.

- Maximum SC current trip level : $I_{SC(max)}$=1.5 * I_C(rated current)
- SC trip referenced voltage (depends on user selection): V_{SC} = min. 0.027 V, typ. 0.03 V, max. 0.033 V (Tolerance 10%, depends on system)
- Shunt resistance : $I_{SC(max)}=V_{SC(max)}/R_{SHUNT(min)}$ →$R_{SHUNT(min)}=V_{SC(max)}/I_{SC(max)}$
- If the deviation of the shunt resistor is limited below ± 1%:

$R_{SHUNT(typ)}=R_{SHUNT(min)}/0.99, R_{SHUNT(max)}=R_{SHUNT(typ)} \times 1.01$

- Actual SC trip current level becomes:

  $I_{SC(typ)}=V_{SC(typ)} / R_{SHUNT(min)}$, $I_{SC(min)} = V_{SC(min)} / R_{SHUNT(max)}$

- Inverter output power:

  $P_{OUT} = \sqrt{3} \times \mathbf{V_{O,LL}} \times \mathbf{I_{RMS}} \times \mathbf{PF}$

  where:

  $V_{O,LL}$= Inverter output line to line voltage

  MI = Modulation Index;

  I_{RMS} = Maximum load current of inverter; and

  PF = Power Factor

- Average DC current

  $I_{DC\_AVG} = V_{DC\_Link} / (P_{out} \times Eff)$

  where:

  Eff = Inverter efficiency

- The power rating of shunt resistor is calculated by the following equation.

  $P_{SHUNT} = (I^2_{DC\_AVG} \times R_{SHUNT} \times Margin)/Derating\ Ratio$

  Where;

  R_{SHUNT} = Shunt resistor typical value at T_C = 25°C

  Derating Ratio = Derating ratio of shunt resistor at T_{SHUNT} = 100°C

  (From datasheet of shunt resistor); and

  Margin = Safety margin (determined by user)

Shunt Resistor Calculation Examples

Calculation Conditions:

- DUT: FSB44104A
- Tolerance of shunt resistor: ±1%
- SC Trip Reference Voltage(V_{SC}) :
- $V_{SC(min)}$ = 0.0297 V, $V_{SC(typ)}$ = 0.03 V, $V_{SC(max)}$ = 0.0303 V
- V_{SC} = Reference voltage of external comparator (refer to the Fig. 3)
- Maximum Load Current of Inverter (I_{RMS}): 28.3 A_{rms}
- Maximum Peak Load Current of Inverter ($I_{C(max)}$): 60 A
- Modulation Index(MI) : 0.9
- DC Link Voltage(V_{DC_Link}): 20 V
- Power Factor(PF): 0.8
- Inverter Efficiency(Eff): 0.95
- Shunt Resistor Value at T_C = 25°C (R_{SHUNT}): 0.5 mΩ
- Derating Ration of Shunt Resistor at T_{SHUNT} = 100°C: 70%
- Safety Margin: 20%

Calculation Results:

- $I_{SC(max)}$: 1.5 × $I_{C(max)}$ = 1.5 x 40 A = 60 A
- $R_{SHUNT(typ)}$: $V_{SC(typ)}$ / $I_{SC(max)}$ = 0.03 V / 60 A = 0.5 mΩ
- $R_{SHUNT(max)}$: $R_{SHUNT(typ)}$ x 1.01 = 0.5 mΩ x 1.01 = 0.505 mΩ
- $R_{SHUNT(min)}$: $R_{SHUNT(typ)}$ x 0.99 = 0.5 mΩ x 0.99 = 0.495 mΩ
- $I_{SC(min)}$: $V_{SC(min)}$ / $R_{SHUNT(max)}$ = 0.0297 V / 0.505 mΩ = 58.8 A
- $I_{SC(typ)}$: $V_{SC(typ)}$ / $R_{SHUNT(typ)}$ = 0.03 V / 0.5 mΩ = 60 A
- $V_{O,LL}=\frac{\sqrt{3}}{\sqrt{2}} \times MI \times \frac{V_{DC\_Link}}{2} = \frac{\sqrt{3}}{\sqrt{2}} \times 0.9 \times 10 = 11.0$ V
- P_{OUT} = $\sqrt{3} \times V_{O,LL} \times I_{RMS} \times PF$ = $\sqrt{3} \times 11.0 \times$ 28.3 × 0.8 = 431.4 W
- I_{DC_AVG} = (P_{OUT}/Eff) / V_{DC_Link} = 22.7 A
- P_{SHUNT} = ($I^2_{DC\_AVG}$ × R_{SHUNT} × Margin) / Derating Ratio = (22.7^2 × 0.0005 × 1.2) / 0.7 = 0.31 W (Therefore, the proper power rating of shunt resistor is over 1.0 W)

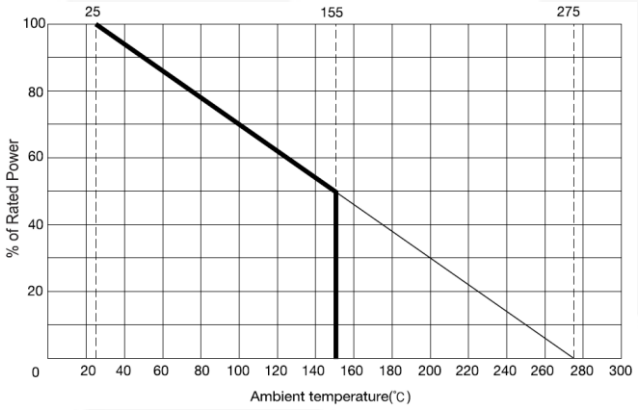


Figure 13. Derating Curve Example of Shunt Resistor (from RARA Elec.)

When over-current events are happened, an external circuit is needed for over-current detection and short circuit protection (SCP).

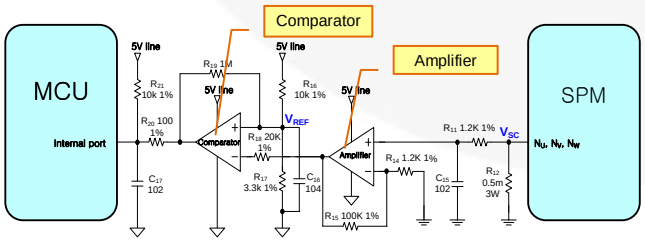


Figure 14. Short-Circuit Protection (SCP) Circuit Using MCU

Figure 14 is typical application circuits for SCP function using MCU, needs external amplifier circuit and comparator circuits. In this reference design, SC trip level (V_{SC}) is 0.3 V ($I_{SC(max)}$=60 A) and V_{REF} level is 2.5 V.

To prevent malfunction, it is recommended that an RC filter be inserted at the C_{SC} pin. To shut down MOSFETs within 3 µs when over-current situation occurs, a time constant of 1.5 ~ 2 µs is recommended.

6.2. Fault Output Circuit

V_{FO} terminal is an open-drain type; it should be pulled up via a pull-up resistor. The resistor must satisfy the above specifications

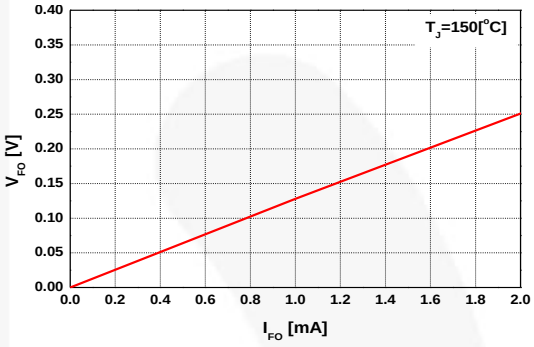


Figure 15. Voltage-Current Characteristics of V_{FO} Terminal

6.3. Circuit of Input Signal (IN(xH), IN(xL))

Figure 17 shows the I/O interface circuit between the MCU and Motion SPM® 45 LV series. Because the Motion SPM 45 LV input logic is active high and there are built-in pull-down resistors, external pull-down resistors are not needed.

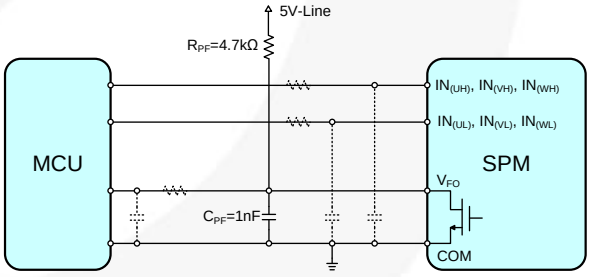


Figure 16. Recommended CPU I/O Interface Circuit

Table 9. Maximum Ratings of Input and VF Pins

Symbol	Item	Condition	Rating	Unit
V_{IN}	Input Signal Voltage	Applied between $IN_{(xH)}$, $IN_{(xL)}$-COM	-0.3 ~ V_{CC} +0.3	V
V_F	Fault Supply Voltage	Applied between VF-COM	-0.3 ~ V_{CC} +0.3	V

The input and fault output maximum rating voltages are shown in Table 9. Since the fault output is open-drain configured, its rating is V_{CC}+0.3 V, 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 5 V logic supply, which is the same

as the input signals. It is also recommended that the de-coupling capacitors be placed at both the MCU and Motion-SPM ends of the VFO and the signal line as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 17 might change depending on the PWM control scheme used in the application and the wiring impedance of the application's PCB layout.

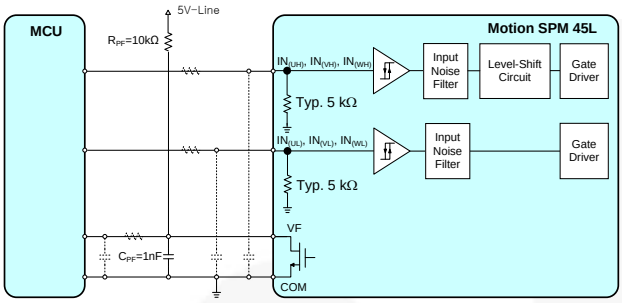


Figure 17. Recommended CPU I/O Interface Circuit

The µMini DIP family of Motion-SPM products employs active-HIGH input logic. This removes the sequence restriction between the control supply and the input signal during startup or shutdown operation. Therefore, it makes the system fail-safe. In addition, pull-down resistors are built-in to each input circuit. External pull-down resistors are not needed, reducing external components. The input noise filter inside the Motion-SPM product suppresses short pulse noise and prevents the MOSFET from malfunction and excessive switching loss. Furthermore, by lowering the turn-on and turn-off threshold voltages of the input signal, as shown in **Error! Reference source not found.**, a direct connection to 3.3 V-class MCU or DSP is possible.

Table 10. Input Threshold Voltage Ratings (V_{DD}=15 V, T_J=25°C)

Symbol	Item	Condition	Min.	Max.	Unit
$V_{IN(ON)}$	Turn-On Threshold Voltage	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$-COM		2.6	V
$V_{IN(OFF)}$	Turn-Off Threshold Voltage	$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$-COM	0.8		V

6.4. Bootstrap Circuit Design

6.4.1. Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between $V_{B(U,V,W)}$ and $V_{S(U,V,W)}$, provides the supply to the HVIC within the motion SPM® 45 LV series. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high-side MOSFET. The SPM 45 LV series includes an under-voltage lock out protection function for the V_{BS} to ensure that the HVIC does not drive the high-side MOSFET, if the V_{BS} voltage drops below a specified voltage (refer to the datasheet). This function prevents the MOSFET from operating in a high dissipation mode.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 18). This method has the advantage of being simples and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap to ground (either through the low-side or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{CC} supply.

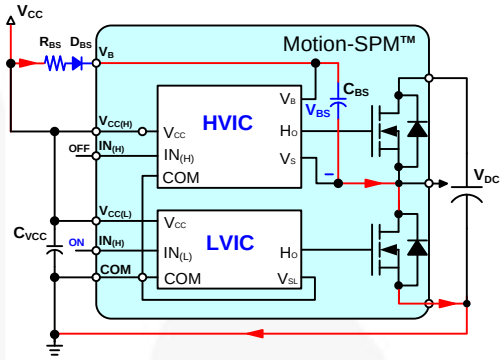


Figure 18. Current path of Bootstrap Circuit

6.4.2. Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on-time of the low-side MOSFET to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln \frac{V_{CC}}{V_{CC}-V_{BS(min)}-V_F-V_{LS}}$$

where:

V_F = Forward voltage drop across the bootstrap diode;

$V_{BS(min)}$ =The minimum value of the bootstrap capacitor;

V_{LS} = Voltage drop across the low-side MOSFET or load; and

δ = Duty ratio of PWM

When the bootstrap capacitor is charged initially; V_{CC} drop voltage is generated based on initial charging method, V_{CC} line SMPS output current, V_{CC} source capacitance, and bootstrap capacitance. If V_{CC} drop voltage reaches UV_{CCD} level, the low side is shut down and a fault signal is activated.

To avoid this malfunction, the related parameter and initial charging method should be considered. To reduce V_{CC} voltage drop at initial charging, a large V_{CC} source capacitor and selection of optimized low-side turn-on method are recommended. Adequate on-time duration of the low-side MOSFET to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts.

Figure 19 shows an example of initial bootstrap charging sequence. Once V_{CC} establishes, V_{BS} needs to be charged by turning on the low-side MOSFETs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency.

Therefore, it is desired to maintain this structure without creating complementary high-side PWM signals. The capacitance of V_{CC} should be sufficient to supply necessary charge to V_{BS} capacitance in all three phases. If a normal PWM operation starts before V_{BS} reaches V_{UVLO} reset level, the high-side MOSFETs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over-current protection level.

Therefore, initial charging time for bootstrap capacitors should be separated, as shown in Figure 20. The effect of the bootstrap capacitance factor and charging method (low-side MOSFET driving method) is shown in Figure 18.

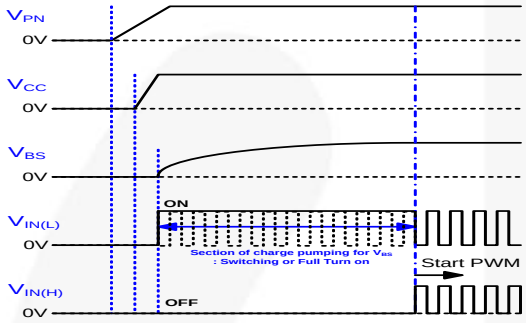


Figure 19. Timing Chart of Initial Bootstrap Charging

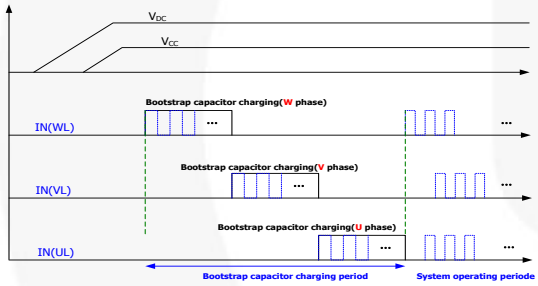


Figure 20. Recommended Initial Bootstrap Capacitors Charging Sequence

Figure 21 and Figure 22 shows waveform initial bootstrap capacitor charging voltage and current.

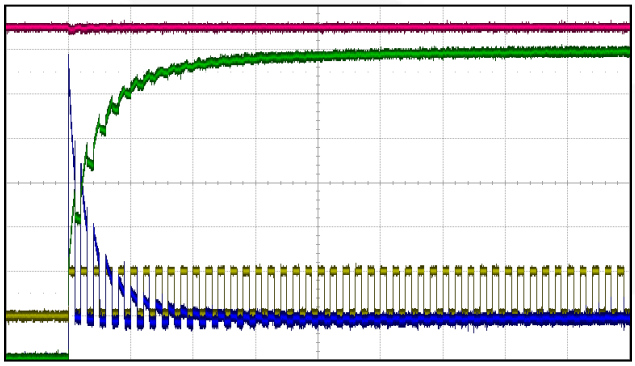


Figure 21. Each Part Initial Operating Waveform of Bootstrap Circuit (Conditions: V_{DC}=20 V, V_{CC}=15 V, C_{BS}=22 µF, LS MOSFET Turn-on Duty=200 µsec)

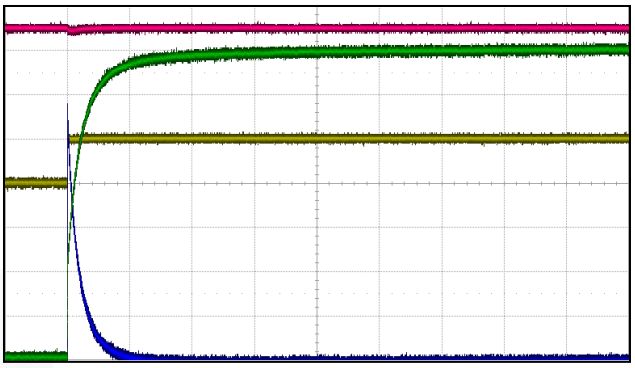


Figure 22. Each Part Operating Waveform of Bootstrap Circuit (Conditions: V_{DC}=20 V, V_{CC}=15 V, C_{BS}=22 µF, LS MOSFET Full Turn-on)

6.4.3. Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}}$$

where:
Δt: maximum on pulse width of high-side MOSFET;
ΔV_{BS}: the allowable discharge voltage of the C_{BS} (voltage ripple); and
I_{Leak}: maximum discharge current of the C_{BS}.

Mainly via the following mechanisms:

- Gate charge for turning the high-side MOSFET on
- Quiescent current to the high-side circuit in HVIC
- Level-shift charge required by level-shifters in HVIC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
- Bootstrap diode reverse recovery charge

Practically, 2 mA of I_{Leak} is recommended for FSB44104A (I_{PBS}, operating V_{BS} supply current at 20 kHz, is max. 2 mA in the datasheet). By considering dispersion and reliability, the capacitance is generally selected to be 2~3 times the calculated one. The C_{BS} is only charged when the high-side MOSFET is off and the $V_{S(x)}$ voltage is pulled down to ground.

The on-time of the low-side MOSFET must be sufficient to for the charge drawn from the C_{BS} capacitor to be fully replenished. This creates an inherent minimum on-time of the low-side MOSFET (or off-time of the high-side MOSFET).

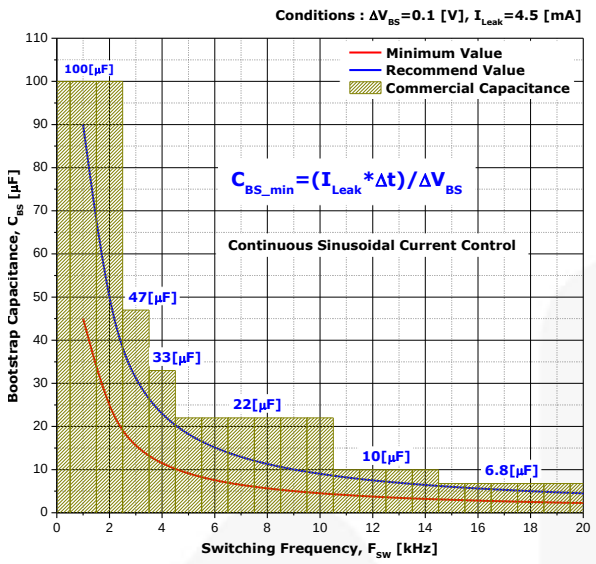


Figure 23. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔV_{BS}

- I_{Leak}: circuit current = 10 mA
- ΔV_{BS}: discharged voltage = 2.0 V (recommended value)
- Δt: maximum on pulse width of high-side MOSFET = 2 ms (depends on user system)

$$C_{BS\_min} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} = \frac{10mA \times 2ms}{2.0V} = 10 \times 10^{-6}$$

→ More than 2~3 times → 20~30 μF.

→ Standard nominal capacitance 22 ~ 35 μF

6.4.4. Selection of Bootstrap Resistor Considering Operating

A resistor must be added in series with the bootstrap diode to slow down the dV_{BS}/dt and determine the time to charge the bootstrap capacitor. If the minimum ON pulse width of low-side MOSFET or the minimum OFF pulse width of high-side MOSFET is t_O; the bootstrap capacitor must be charged to increase the voltage by ΔV during this period. Therefore, the value of bootstrap resistance can be calculated by:

$$R_{BS} = \frac{(V_{CC} - V_{BS}) \times t_o}{C_{BS} \times \Delta V_{BS}}$$

where:

V_{CC} = Supply voltage;

V_{BS} = Minimum bootstrap voltage;

t_O = Minimum ON pulse width;

C_{BS} = Bootstrap capacitor value; and

ΔV_{BS} = Ripple voltage of V_{BS}.

Calculation Examples of R_{BS}:

V_{CC} = 15 V, V_{BS} = 13 V (minimum voltage)

t_O = 200 μs (if carrier frequency is 5 kHz, 1-cylce is 200 μs)

C_{BS} = 20 μF (obtained bootstrap capacitor value)

ΔV_{BS} = 2 V (recommended value)

$$R_{BS} = \frac{(V_{CC} - V_{BS}) \times t_o}{C_{BS} \times \Delta V_{BS}} = \frac{(15-13)V \times 200\mu s}{20\mu F \times 2V} = 10\Omega$$

If the rising dV_{BS}/dt is slowed significantly, it could cause missing pulses during the startup phase due to insufficient V_{BS} voltage.

Note:

18. The capacitance value can be changed according to the switching frequency, the capacitor selected, and the recommended V_{BS} voltage of 13.0~18.5 V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of the component.

7. Print Circuit Board (PCB) Design

7.1. General Application Circuit Example

Figure 24 shows a general application circuitry of interface schematic with control signals connected directly to a MCU. Figure 25 shows guidance of PCB layout for the Motion SPM® 45 LV series.

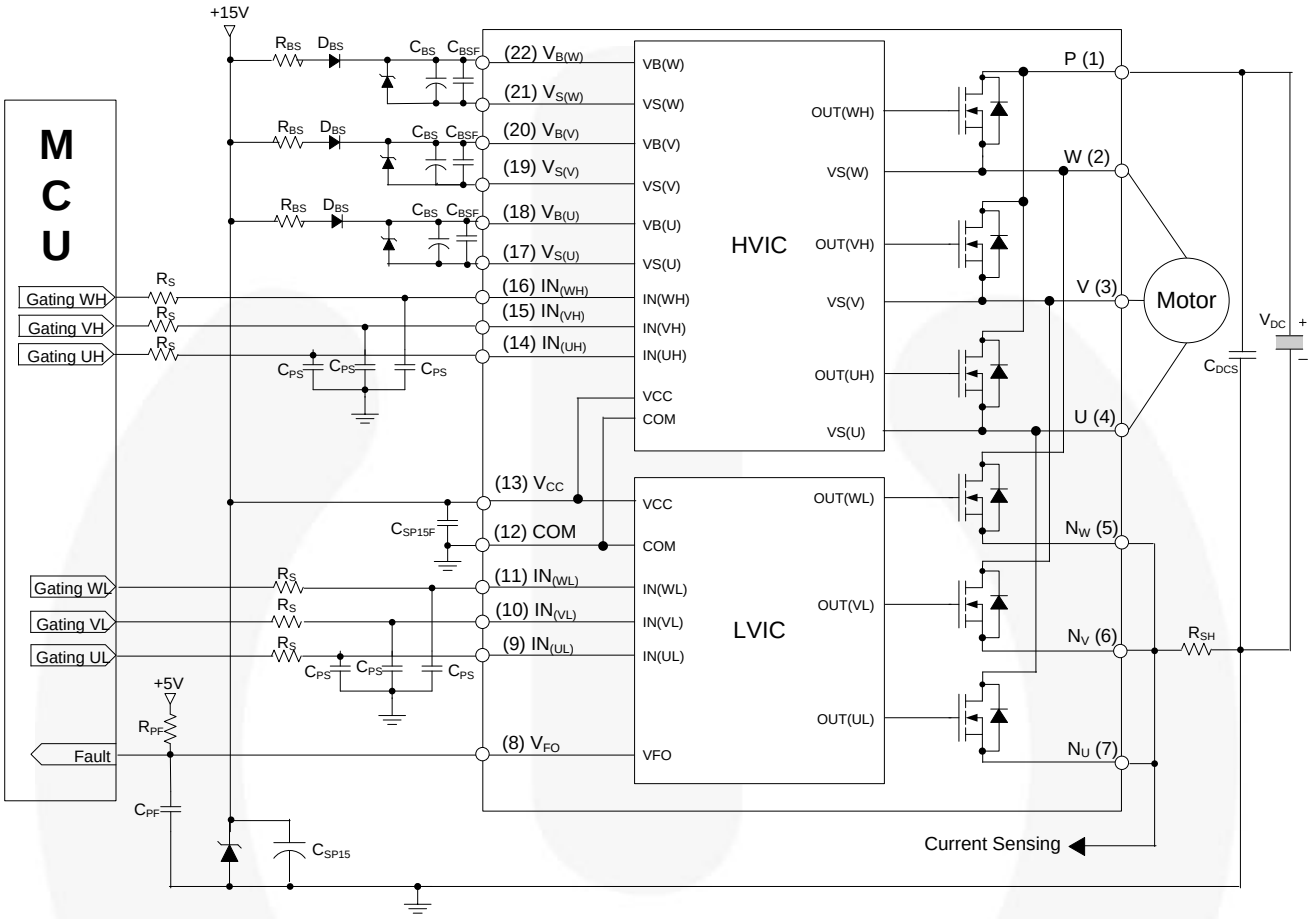


Figure 24. General Application Circuitry for Motion SPM 45 LV series

7.2. PCB Layout Guidance

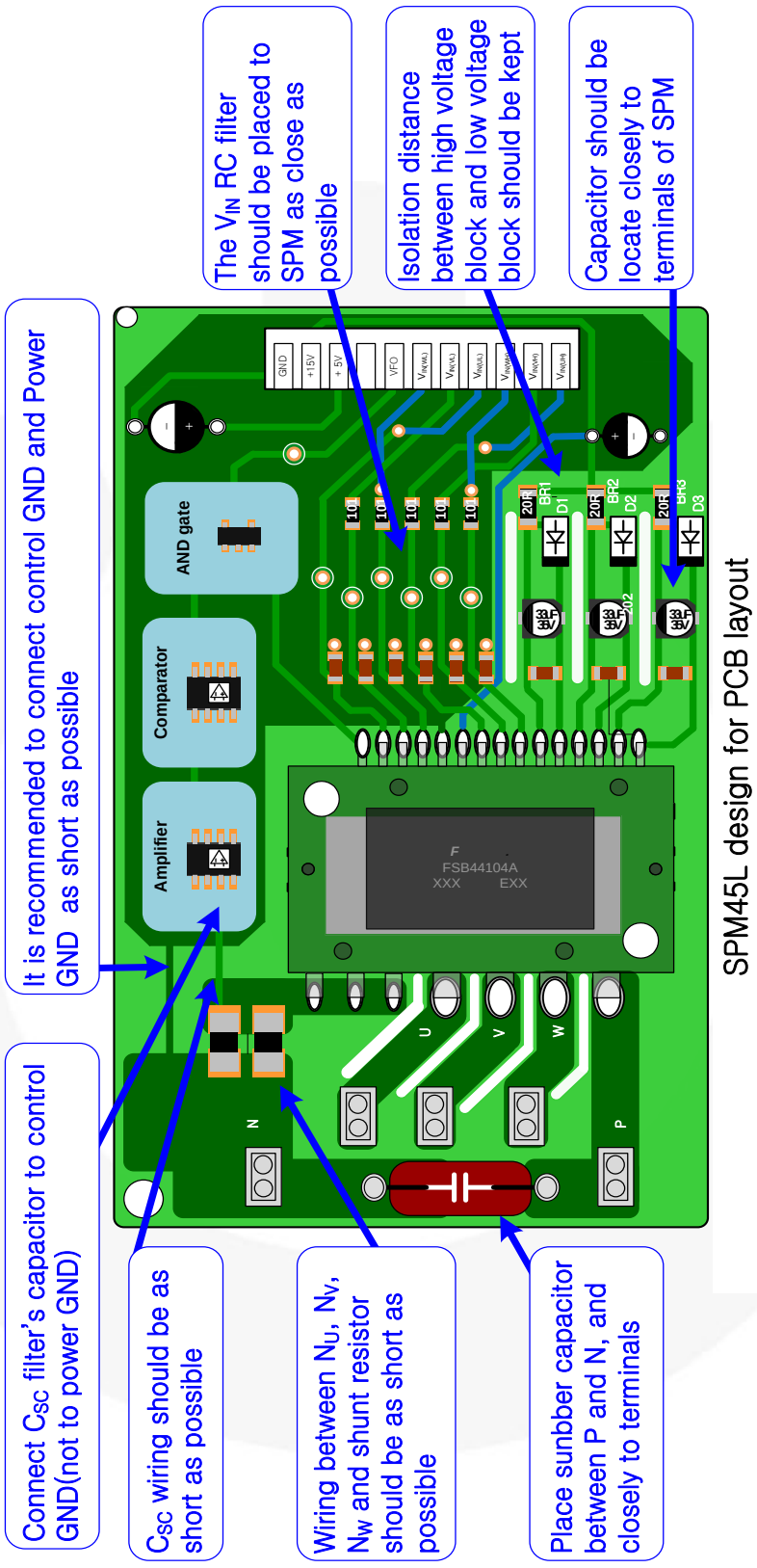
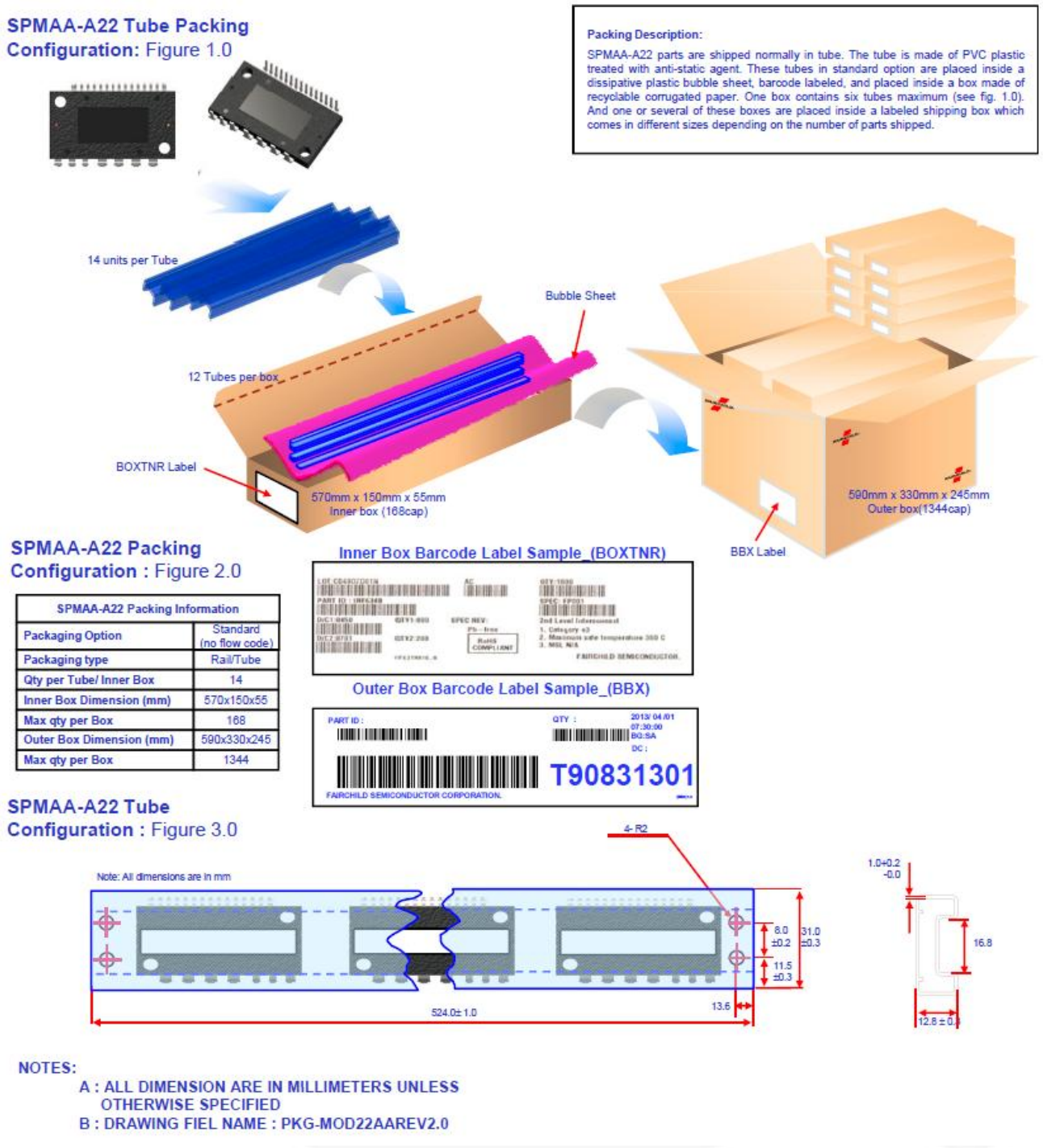


Figure 25. Print Circuit Board (PCB) Layout Guidance for the Motion SPM® 45L series

Packing Information



SPMAA-A22 Packing Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	14
Inner Box Dimension (mm)	570x150x55
Max qty per Box	168
Outer Box Dimension (mm)	590x330x245
Max qty per Box	1344

Figure 26. Packing Information

Related Resources

FSB44104A- Product Folder

RD-408 – Reference Design Guide

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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