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AN-6095 — D-PHY MIPI® Switches in Multi-Camera / Multi-Display Applications

Overview

When choosing an analog switch for use in a multi-camera or multi-display Mobile Industry Processor Interface (MIPI) application, there are several factors to consider, such as:

- Specific Architecture of Implementation
- Number of Data Lanes
- CLK Rate
- Insertion Loss of the Analog Switch
- S-Parameter Characteristics of the Switch S_{DD21}
- Importance of PCB Design

The biggest factor is the insertion loss of the switch. This application note discusses tradeoffs to consider and makes recommendations for choosing an analog switch.

Multi-Camera / Multi-Display Architectures

Today's processors that support MIPI Display Serial Interface (DSI) or Camera Serial Interface Rev2.0 (CSI-2) have multiple ports available, so for many dual-camera (display) end markets, the designs often maintain point-to-point connectivity. However, there are advantages to isolating the paths to minimize signal artifacts that can result in a noisy environment.

If there are more than two sinks, there is likely benefit to utilizing analog switches. Once the architecture is determined, it's time to choose the implementation. Options include cascading devices, sharing busses or device footprint (a single FSA644 can replace up to three switches in typical applications of up to four data lanes). Figure 1 shows a typical dual-camera / dual-display connectivity.

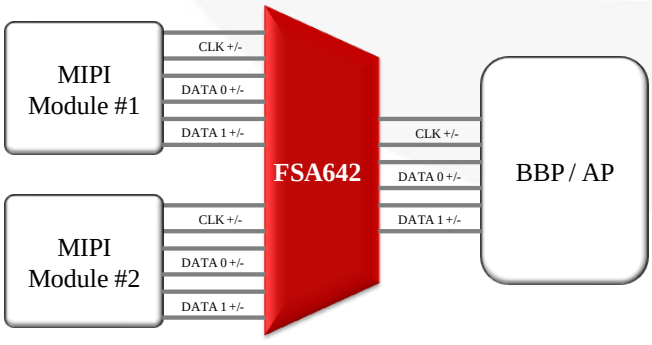


Figure 1. Dual 2-Data-Lane Camera / Display

Data Lanes

Each application is unique and, in the case of cameras, there may be multiple data lanes and / or multiple high-resolution and low-resolution cameras to accommodate.

Figure 2 illustrates the FSA641 connectivity for a 2-data lane and 1-data lane resolution cameras.

Figure 3 illustrates the FSA644 4-data lane configuration.

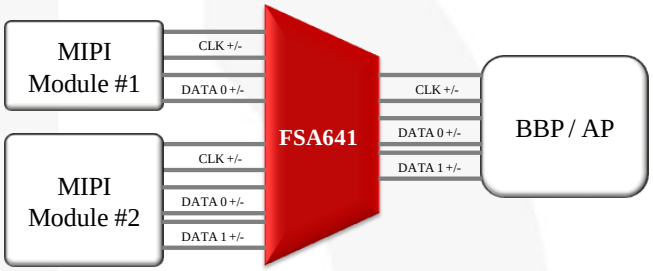


Figure 2. Dual High / Low Resolution Camera

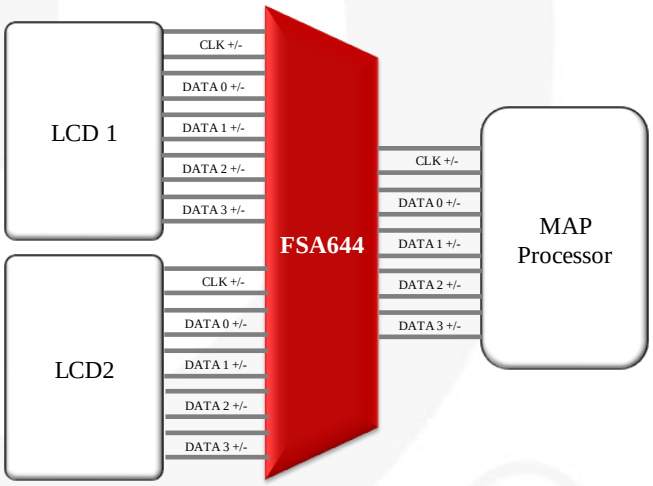


Figure 3. Dual 4- Data-Lane Camera / Display

Clock (CLK) Rate

For the first approximation for a 1.5 Gbps / lane MIPI data rate, consider a switch with a f3 dB point of 750 MHz. This implies that a typical USB2.0 switch is adequate, but that is not necessarily the case in reality. For interoperability testing, there is a specific mask, which is greatly influenced by the insertion loss of the switch, the attached load, and the

interconnect characteristics. If any of these factors are high, the signal edge rate through the switch may not meet the 0.35*UI calculation required for meeting the D-PHY Rev 1.1 specification and passing interoperability. In addition, the mask used to measure for interoperability uses the f2 dB and f5 dB points versus the classic f3 dB bandwidth curve. Approximate the expected data rate by looking at a bandwidth plot and utilizing the following formula:

$$\text{Data Rate} = 2/3 \times f5\ dB \quad (1)$$

CLK rate also approximates to the f2 dB point.

There is danger to relying on this equation alone. Most bandwidth curves in datasheets are specified into a 50 Ω environment without additional load capacitance. Board characteristics and discontinuities modify the bandwidth curve beyond the 3 dB point. Below is an example of how to utilize the bandwidth curve for a first approximation.

Example

Figure 4 illustrates a typical bandwidth curve (FSA642) and the f5 dB is approximately 1.3 GHz, which equates to a data rate of around 860 Mbps.

Interoperability testing adds additional board, connector, and sensor capacitances and resistances that typically reduces data rate by around 150-200 Mbps.

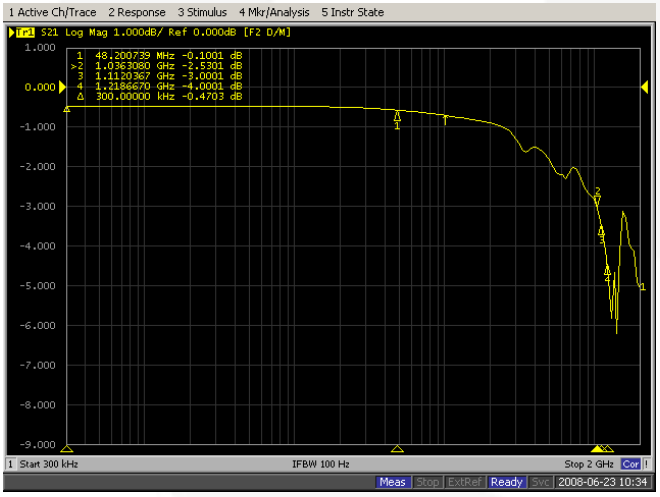


Figure 4. FSA642 Bandwidth Curve

These parametrics can be quantified by determining the insertion loss of the switch.

Switch Insertion Loss

The definition for switch insertion loss is the difference in the MIPI application between a point-to-point connectivity and inserting the analog switch in the path.

The MIPI D-PHY Conformance Test Suite can be used to determine the change due to the addition of the switch by quantifying the insertion loss that the Receiver Termination Board (RTB) sees in response to a typical MIPI HS-Tx signal.

Quantifying the Insertion Loss

To meet the MIPI D-PHY Rev 1.1 specification, the edge rate out of the switch must not exceed 233 ps (0.35*UI) to meet the 1.5 Gbps interoperability mask.

Figure 5 illustrates the analog switch as part of the MIPI Transmission Line Interconnect System (TLIS) scheme to assist in calculating the contribution of the switch through its insertion loss characteristics based on the incident wave response of the switch.

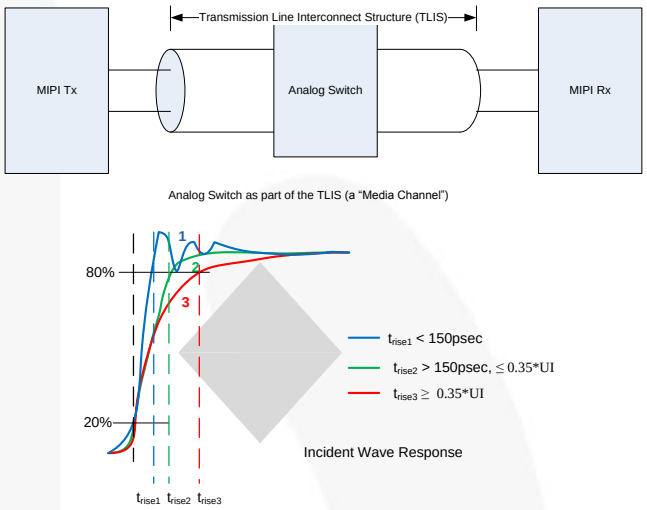


Figure 5. Insertion Loss

The amount of insertion loss is a factor of the R_{ON} and C_{ON} of the switch

Even if the response follows curve 3 /red in Figure 5, the device may perform in the system with no impact to "plug-n–play" interoperability.

By designing a board for interoperability testing that includes a direct calibration path, it is possible to calculate the insertion loss contribution related to the analog switch.

Figure 6 illustrates a board used for interoperability testing of the FSA644.

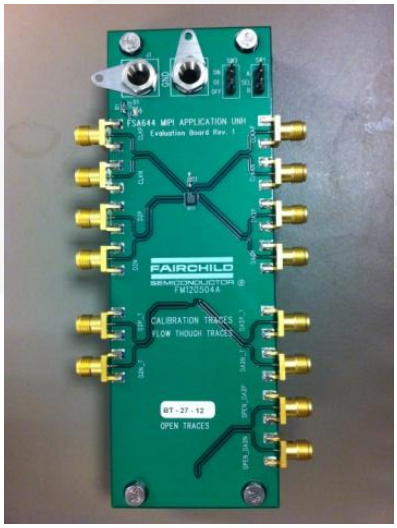


Figure 6. FSA644 Interoperability Board

S-Parameter (S_{DD21})

After performing the D-PHY conformance testing, the FSA644 insertion loss calculation resulted in the performance, to the 1.5 Gbps mask, in Figure 7. Figure 8 shows the FSA644 insertion loss when tested to the 1.2 Gbps mask.

Since the interoperability environment is "harsh" with more discontinuities and long cable lengths, it is very important to pay attention to the PCB design and sensor load to ensure meeting the mask for > 1 Gbps *(see Figure 7 and Figure 8)*.

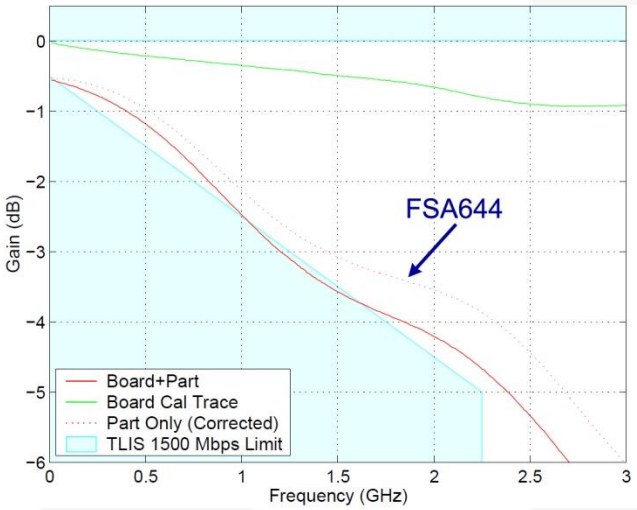


Figure 7. FSA644 Insertion Loss (S_{DD21}) at 1.5 Gbps

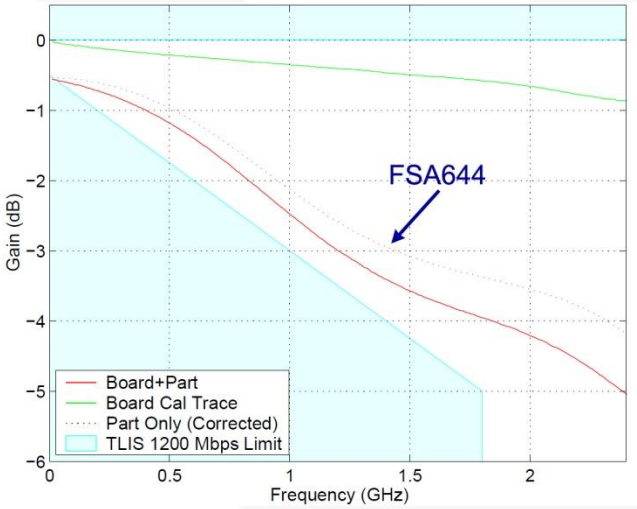


Figure 8. FSA644 Insertion Loss (S_{DD21}) at 1.2 Gbps

Importance of PCB Design

In a mobile product, there are many discontinuities that a signal may encounter on its journey to the display or from the camera (vias, flex cable, connectors) that change the characteristic impedance of the routing and be potential antennas or stubs for reflections.

Figure 9 shows the potential for reflections with a shared point-to-point architecture for multi-display / multi-camera applications. Figure 10 shows actual discontinuities, which can be detrimental to system timing.

By adding the analog switch, the effects of discontinuities can be lessened, as shown in Figure 11 and Figure 12.

Figure 13 shows the discontinuity improvement that can be achieved using MIPI analog switches.

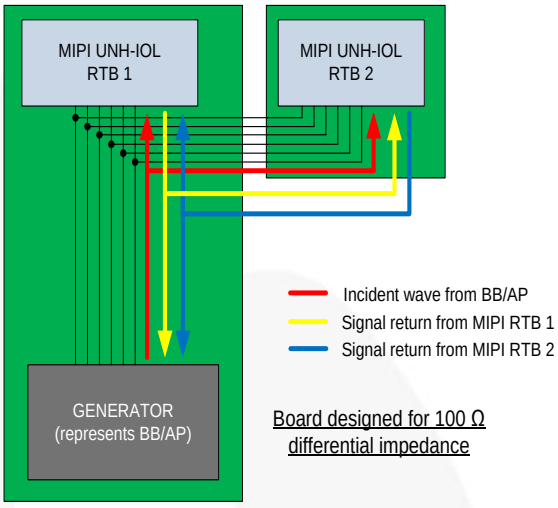


Figure 9. Shared MIPI Bus

HS traffic edge rate and swing is reduced (results in closing "eye")

Figure 10. Shared Bus Discontinuities

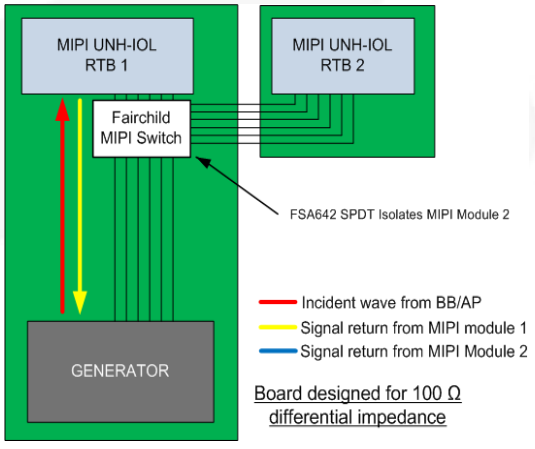
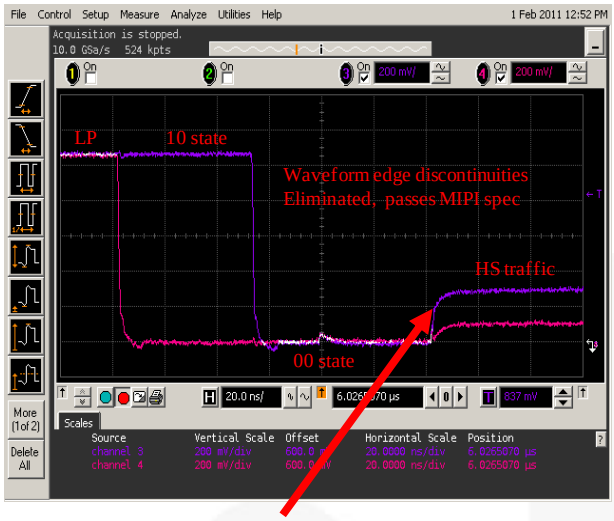
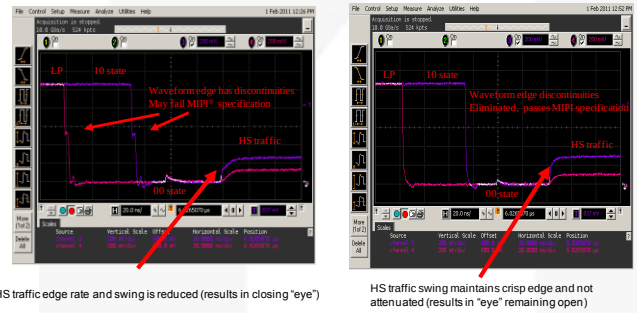


Figure 11. MIPI Switch Isolated Bus



HS traffic swing maintains crisp edge and not attenuated (results in "eye" remaining open)

Figure 12. Isolated Bus Discontinuities



HS traffic edge rate and swing is reduced (results in closing "eye")

HS traffic swing maintains crisp edge and not attenuated (results in "eye" remaining open)

Figure 13. Shared vs. Isolated Bus

The above descriptions discuss the PCB design from the perspective of the functional blocks, but it is necessary to address other aspects, such as:

- Device placement with respect to sensors, displays, TVS or connectors
- Differential impedance matching (100 Ω ±20%)
- Number of devices to implement architecture
- Minimizing vias, stubs, and test points
- Standard high-speed differential signaling criteria for PCB design

As described in the figures above, the artifacts of reflections and discontinuities can degrade performance. Further high-speed differential signaling criteria include:

- Use micro-strip or stripline.
- Do not place noisy signals over or near high-speed differential signals.

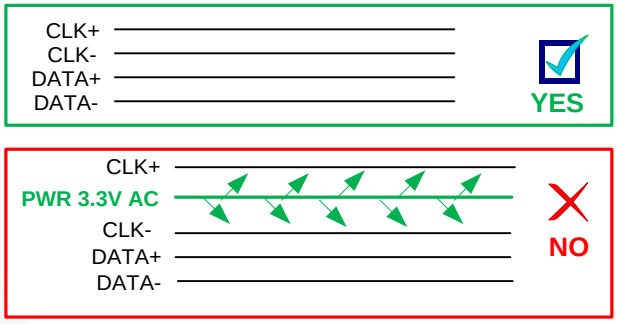


Figure 14. No Noisy Signals Near High-Speed Signals

- Isolate serial lines with adjacent GNDs.

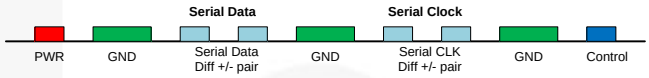


Figure 15. Serial Lines Isolate with Adjacent GNDs

- If a signal line must cross the high-speed lines, ensure it is made perpendicularly.
- Match trace length of high-speed signal lines as closely as possible.

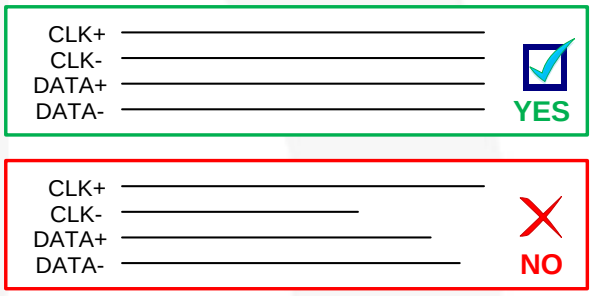


Figure 16. Match Trace Lengths

- If probe points are required, ensure they are inline with the trace and not creating a transmission line stub.

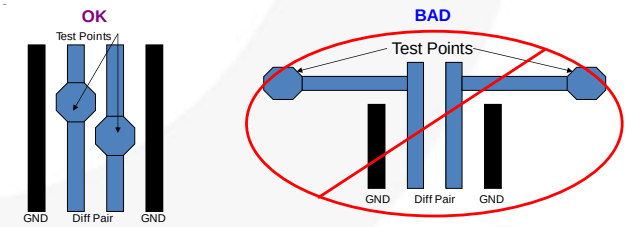


Figure 17. Inline Probe Points

Figure 18 shows how a dual two-lane D-PHY application can be implemented using several USB switches. This requires (typically) > 9 mm^2 of PCB space, has crossovers and vias, and can be space-intensive when migrating up to four-lane architectures.

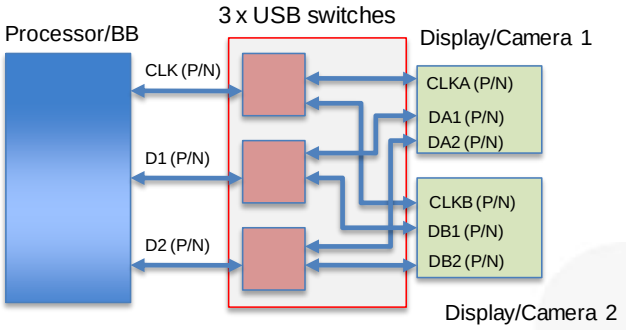


Figure 18. Dual 2-Lane MIPI Using USB Switches

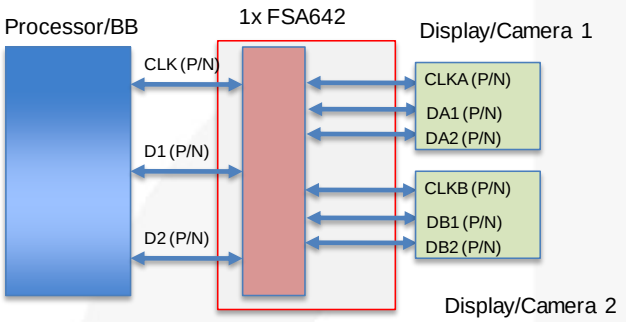


Figure 19. Dual 2-Lane MIPI Using Single FSA642

Figure 19 shows the dual two-lane implementation using the FSA642. This implementation is a little smaller than USB switches (8.5 mm2) and has the advantage of a flow-through PCB design.

When migrating to four-lane (as shown in Figure 3), each of these implementations at least doubles in PCB area. However, using the FSA644 optimizes the PCB footprint (6 mm2), improves signal integrity, and the device has a data rate capability greater than 1.2 Gbps.

Table 1 summarizes the choice by performance and footprint for MIPI switches in D-PHY camera / display applications.

Table 1. MIPI Switch Architecture Options

	Rate	2-Lane (mm)	4-Lane (mm^2)
FSA641	700-800 Mbps	3 x 3	>18
FSA642	700-800 Mbps	2.5 x 3.4	>17
FSA644	>1.2 Gbps	2.4 x 2.4	5.76
USB Switches	800 Mbps	3 Devices + Board Routing / Separation 1.5 x 2.0	>19

Summary

Many factors influence the choice of analog switches in multi-camera and multi-display architectures. Cascading devices is also not preferred, but for today's applications and board area, the FSA644 can be an optimal solution.

References

[1] *Connolly, Graham & Lee, Tony "Analog Switches in D-PHY MIPI Dual-Camera / Dual-Display Applications," Planet Analog, March 2011.*

Related Datasheets

FSA641 — 2:1 MIPI Switch, Featuring 2-Data and 1-Data Lane Configuration

FSA642 — Low-Power, Three-Port, High-Speed MIPI Switch

FSA644 — 2:1 MIPI D-PHY (1.5 Gbps) 4-Data Lane Switch

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