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Low Noise Leadless Packages Advance Portable Designs

Abstract

Portable applications are everywhere in the world today. A vivid illustration is the ubiquitous cell phone. Portability implies small application size, or handheld, and that systems will continue to shrink in order to drive the market. Portables are not only smaller, but continue to add functionality. Consequently, there is an ongoing trend toward less circuit board space in order to accommodate the semiconductors that enable the applications. For portable designs to advance and incorporate more functionality, it follows they must adopt chips in smaller packaging.

Semiconductor die continuously undergo revision, becoming smaller as processes evolve. However, the packages the die reside in are magnitudes larger by comparison. Although package will always determine the size of the end-product, package technology is advancing bringing the ratio of package to die down. Leadless packaging like Depopulated Very-thin Quad Flat-pack No-leads (DQFN) and Micro Leadless Packaging (MLP) in general, provide next generation form factor reductions. DQFN dramatically reduces the hardware footprint area necessary for mounting. DQFN also provides for superior power dissipation with the provision of an exposed Die Attach Paddle (DAP) located under the package. Figure 1 illustrates the significant size difference between TSSOP and DQFN.

The 14-pin TSSOP has a footprint area of 32 square millimeters. The pin extensions comprise 31% of the required mounting area. DQFN requires just 7.5 square millimeters. DQFN is smaller and does not have pin extensions. The DQFN is 75% smaller compared to TSSOP. DQFN is also smaller in height and weighs less too. Indeed, board space savings of MLP is significant; however, there is another benefit to using the leadless solution in a design; this, lower inherent switching noise. The remainder of this paper will address the low noise advantage of leadless packaging.

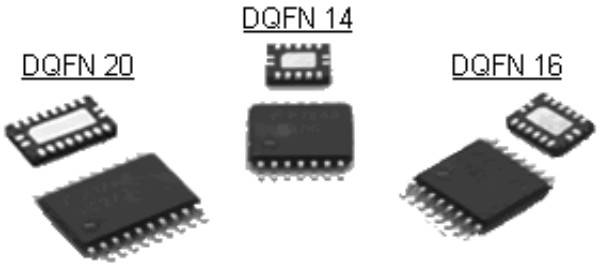

FIGURE 1. Comparison of TSSOP and DQFN Package Sizing

Package Inductance and Switching Noise

The connection from the silicon die to the external circuit consists of bond wires and package pins. The bond wires that connect the die to the lead frame and the pins extending this connection to the external circuit create inductive paths. With MLP, pins may more appropriately be referred to as pads and as such the lead frame creates less related inductance. Albeit critical, these inductive connections contribute noise to the supply rails during output logic state transitions.

Figure 2 represents a model of these inductances as they appear from the die out to the external circuit. L_5, L_6, L_7, and L_8 are the die bonding wire inductances and L_1, L_2, L_3, and L_4 are the pin inductances. C_L represents the output load for the device and is composed of circuit board trace and down-stream receiver input capacitive loading.

The switching noise voltage generated in the connection inductances signified in Figure 2 is given by the expression, $V_n = Ldi/dt$, where L is the inductance in the return or loop current path for the output. The di/dt component is the sum of the output current over time required to switch the output from one state to another. Noise voltage, V_n, generated in these inductances and based on current demand, must be added to the power rail potentials during signal transitions. During a HIGH-to-LOW transition, the current necessary to drive a state change in the output must return to the die ground reference through package inductance. Assuming the device ground pin and load are connected directly to a low inductance, low impedance, continuous ground plane, the current path back to the die is essentially the package lead frame and bond wire inductances, L_1 and L_7 (see Figure 2). These inductances are in series and are added to comprise component L in the noise voltage formula.

When package inductance, transition time, and delta current are known, the expression $V_n = Ldi/dt$ can then be applied to determine the noise voltage. The noise generated in the return loop inductance is added to the die ground reference (see Figure 3). The industry term for the noise voltage associated with the HIGH-to-LOW transition is *ground bounce* or V_{OLP}. For a LOW-to-HIGH transition, current must return through the V_{CC} package connection inductances and is referred to as V_{CC} droop or V_{OHV}. For further clarification, Fairchild application note AN-737 provides definition of noise terms and an overview of noise measurement techniques. It is important to note, the LOW-to-HIGH current transition is usually suppressed using high quality, low inductance chip capacitors connected at the V_{CC} rail where it enters the device. The ground end of the capacitor should be located over a circuit via directly to the ground plane for best results.

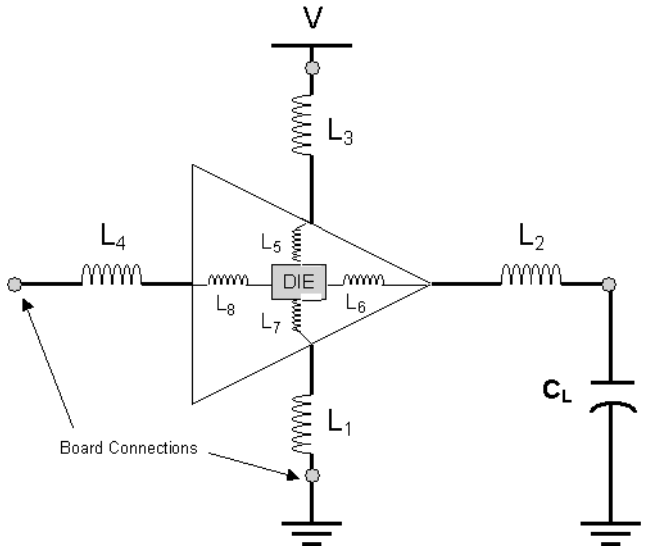

FIGURE 2. Die to Circuit Board Inductance Model

Package Noise in the Application

To illustrate how package inductance contributes to noise in the application, we derive actual noise voltages generated in a TSSOP 20-pin package and compare that to a DQFN 20-pin package. Two high speed logic technologies will be used.

The 74VCX245 and 74LCX245 octal buffer drivers are applied driving 30pF loads at V_{CC} of 2.3V. The formula RC = 0.63(T) is used to compute the resistance of the outputs in order to find transitional current. One RC time constant represents 63% of the output edge transition. Please note that the parameters used in the application illustrate the significant difference in Pin 10 leadframe inductance (L_1) between the two packages in bold below.

Parameters for the LCX application example:

HIGH-to-LOW transition time into 30pF load: 3.64ns

TSSOP Pin 10 ground lead inductance (L_1): 1.86nH

TSSOP ground reference bond wire (L_7): 0.56nH

DQFN Pin 10 ground lead inductance (L_1): 0.030nH

DQFN die ground reference bond wire (L_7): 0.81nH

Computation for LCX in TSSOP:

RC = 0.63(T)

R = 0.63(T)/C

R = 0.63(3.65ns)/30pF

R = 76.65 or 77Ω

I = V/R

I = 2.3/77

I = 29.87mA or 30mA

V_n = L di/dt

V_n = 1.86nH + 0.65nH (30mA/3.64ns)

V_n = 19.95mV

Computation for LCX in DQFN:

Output impedance for the LCX device has not changed. The only difference is in the package ground loop inductance. The noise voltage is computed using the noise voltage formula:

V_n = L di/dt

V_n = 0.81nH + 0.030nH (30mA/3.64ns)

V_n = 6.92mV

In the LCX application above, the DQFN leadless package offers more than 65% reduction in the package related noise voltage.

The VCX buffer driver is faster and drives greater current into the same 30pF load. Also note in the parameters that LCX in TSSOP uses 2 bond wires for connecting the die ground reference to the lead frame (Pin 10). This effectively reduces the bond wire inductance by half. Conversely, VCX in TSSOP uses a single bond wire for connection to Pin 10 and exhibits twice the inductance for L_7 compared to LCX.

Parameters for the VCX application example:

HIGH-to-LOW transition time into 30pF load: 2.83ns

TSSOP Pin 10 ground lead inductance (L_1): 1.86nH

TSSOP ground reference bond wire (L_7): 1.14nH

DQFN Pin 10 ground lead inductance (L_1): 0.030nH

DQFN ground reference bond wire (L_7): 0.81nH

Computation for VCX in TSSOP:

RC = 0.63(T)

R = 0.63(T)/C

R = 0.63(2.83ns)/30pF

R = 59.43 or 59Ω

I = V/R

I = 2.3/59

I = 38.98mA or 39mA

V_n = L di/dt

V_n = 1.86nH + 1.14nH (39mA/2.83ns)

V_n = 41.34mV

Computation for VCX in DQFN:

The output impedance still applies since the only difference is package ground path inductance. The noise voltage formula is applied as follows:

V_n = L di/dt

V_n = 0.81nH + 0.030nH (39mA/2.83ns)

V_n = 11.58mV

VCX technology is higher speed logic versus LCX and so produces greater ground bounce. With VCX, the advantage of using a DQFN package is nearly 72% reduction in the ground reference switching noise voltage.

Representative output waveforms are depicted in Figure 3. The figure shows the HIGH-to-LOW transition with accompanying package related noise riding on the ground reference level. This plot is representative of the VCX buffer driver ground bounce in the 20-pin TSSOP package.

Package Noise in the Application (Continued)

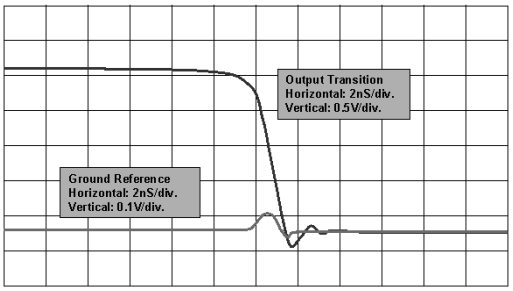

FIGURE 3. Ground Reference Noise Voltage Due to Package Inductance

Summary

MLP offers semiconductor packaging in a new generation of smaller form factors. Leadless packaging offers system designers the opportunity to reduce the board space area requirement. Additionally, the applications in this paper illustrate the distinct electrical advantage the DQFN package has over pin-based packages. The chart in Figure 4 points out the differences in ground bounce noise voltage found after comparing the TSSOP and DQFN packages in the application examples above.

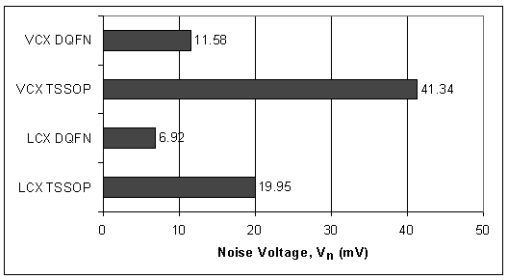

FIGURE 4. Package Noise Comparison

Highlights:

1. Noise voltage or ground bounce is directly proportional to the speed of the logic semiconductor technology.
2. Ground bounce is a result of the current return loop inductance, is coincident with the HIGH-to-LOW edge transition, and appears on the die ground reference.
3. When a minimal inductance, solid ground plane layer exists for the device ground reference pin, ground bounce depends primarily on series die-to-leadframe bond wire and pin-to-circuit board package inductances.
4. DQFN leadless packaging produces 3 to 4 times less ground bounce noise in the application compared to the common TSSOP package.
5. Ground bounce contributes to the overall system noise budget, can increase system EMI, and has the potential to disrupt system timing.

In the applications illustrated, a single output was analyzed for a device that has 8 outputs. It is important to realize that as other outputs on the device switch simultaneously, the additional current required to change the output state must return through the same ground loop path inductances. As additional simultaneous outputs switch a proportional increase in the noise voltage will result. In other words, each additional switching output adds another V_n component to the ground reference level.

With this paper, Fairchild Semiconductor hopes to contribute to the designers' knowledge in understanding the advances in semiconductor packaging. It is our assertion that not only is reduction in size advantageous, but there is a significant electrical benefit for using MLP as well.

Useful references:

AN-737, Device Generated Noise Measurement Techniques

AN-640, Understanding and Minimizing Ground Bounce

AN-680, Dynamic Threshold for Advanced CMOS Logic

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