

Design Approach to Light-Load Effective Power Supply Utilizing the NCP1244/46 PWM Controllers



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APPLICATION NOTE

Introduction

When designing power supplies, the important defining regulations for efficiency and no-load power requirements are the ENERGY STAR® specifications. With the release of the EPS 2.0 standard, the light-load input power consumption and the standby power consumption have become more important. The new specification more accurately reflects the actual usage of a laptop adapter which operates a considerable amount of time in a no-load or a minimal load operating condition (laptop in sleep mode).

The key losses need to be identified when focusing on the light-load efficiency of the adapter design. Switching losses play a major role in determining the light-load efficiency and are directly linked to the control methodology. These losses are caused by the energy stored in the sum of all the capacitances at the drain node (MOSFET output capacitance, stray capacitance of the transformer and other parasitic capacitances on PCB) together with the gate charge losses associated with driving the MOSFET. These losses are also proportional to the switching frequency. Hence reducing the switching frequency reduces the losses and improves the efficiency.

The NCP1244/46 family of PWM controllers are focused on meeting the new stringent ENERGY STAR® requirements. A key part of this architecture is a frequency foldback function, thereby lowering the frequency at lighter loads and reducing the switching losses. The additional feature helping to decrease the switching losses is a fixed current set point under light-loading condition. This feature increases the transferred energy in a single pulse, but also decreases the switching frequency to deliver the required amount of power to the load.

No-load input power of the power supply continues to be an important requirement. This refers to when the power supply or adapter is plugged into the wall outlet and not plugged into the laptop. The requirements for less than 30 mW of no-load input power is quite common in such applications like notebook, Ultrabook™ or printer adapters. Every loss component in the power supply design starts to play a big role when trying to achieve such a small amount

of no-load input power. Two important components of no-load consumption are the controller consumption and the EMI filter X2 capacitor discharge branch.

The NCP1244/46 family of PWM controllers has integrated advanced features which dramatically reduce consumption in no-load mode. These are off-mode and the X2 capacitors discharge sequences which fulfill the safety requirements when the power supply is unplugged from the outlet.

The power supply having no-load consumption below 30 mW can be designed using the NCP1244/46 family of PWM controllers.

Application Note Contents

- The NCP1244/46 Features Brief Description
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65 W ac-dc Adapter Board Specifications

The adapter was designed for the following performance ratings:

Output Power	65 W
Output Voltage	19 Vdc
Output Current	3.42 A
Minimum Input Voltage	85 V
Maximum Input Voltage	265 V
Average Efficiency (as per Energy Star 2.0 guidelines)	> 87%
No-Load Input Power	< 30 mW

Features of NCP1244/46 Family

The usage of current mode PWM controllers from NCP1244/46 family brings an advantage in decreasing the consumption in no-load conditions by dedicated off-mode. This mode is controlled by the FB pin and allows the remote control (or secondary side control) of the power supply to shut down. Most of the device's internal circuitry is unbiased in the low consumption off-mode. Only the FB pin control circuitry and X2 cap discharging circuitry operates in the low consumption off-mode. When the voltage at feedback pin decreases below the 0.4 V, the controller enters the low consumption off-mode. The controller starts if the FB pin voltage increases above the 2.2 V level. Other features include:

- **X2 Capacitor Discharge:** This feature saves approximately 16 mW – 25 mW input power depending on the EMI filter X2 capacitors volume and it saves the external components count as well. The discharge feature is ensured via the start-up current source with a dedicated control circuitry for this function.
- **Current-Mode Control:** Cycle by cycle, primary current sensing helps to prevent any significant overcurrent conditions that would cause transformer core saturation and result in power supply failure.
- **Frequency Foldback:** This advantage lies in decreasing the switching frequency under light-load conditions. This feature is called frequency foldback and significantly helps to reduce switching losses.
- **Frozen Current Setpoint under the Light-Load Conditions:** This feature increases efficiency under the light-load conditions. The light-load condition is detected when the FB pin voltage is below 1.5 V.
- **Dynamic Self-Supply:** This ensures the voltage supply for the IC in applications where the output voltage varies significantly during operation, e.g. during the startup of the power supply or overload conditions. The dynamic self-supply (DSS) also supplies the IC during a latched state and when the switching operation is stopped. The dynamic self-supply operates by means of controlling the charging of the capacitor at V_{CC} pin via a built-in high voltage current source. In order to prevent any damage or overheating of the controller in case of a short in V_{CC} circuitry, the high voltage startup current is limited when the V_{CC} is below 0.6 V.
- **High Voltage Sensing:** The device allows direct high-voltage sensing up to 500 V to enable features such as brown-out protection and input OVP without using extra pins.
- **Brown-Out Protection:** This function is enabled for the NCP1246 device only and protects the application when the main voltage is too low. If the peak voltage at the HV pin V_{HV} is higher than 111 V (typical – see V_{HV(start)} spec in the datasheet) and if the V_{CC} is high enough, the device will start operating. The device runs and produces the DRV pulses if the HV pin voltage is above the V_{HV(stop)} (brown-out protection stop level). There is a 65 ms (typ.) timer before the brown-out protection is activated allowing the converter to ride through a short line drop-out.
- **Timer Based Overcurrent Protection:** The devices NCP1244/46 offer the overcurrent protection which is activated when the voltage at CS pin is above the internal threshold of 0.7 V (typ.) for a longer time than the overcurrent fault timer duration time (typ. 128 ms).
- **Current Stop Protection:** A special additional current stop protection senses the voltage at the current sensing pin. If this voltage is higher than 150% of the maximum internal current set point, the protection fault mode is immediately activated. This feature protects application against the winding short-circuit or the shorts at the output of the application.
- **Overpower Compensation:** The primary peak current value varies with the value of the input voltage. The reason is the propagation delay between the internal current set point detection and the power MOSFET switch-off and dependence of the primary current slope on the input voltage. In order to eliminate this phenomenon, the peak voltage at HV pin is sensed and converted into a current flowing out of the CS pin. By the external resistor R_{OPP} a voltage offset to V_{sense} voltage is created providing the overpower compensation as a result.
- **Built-In Internal Slope Compensation:** In order to avoid the sub-harmonic oscillations during the CCM operation with the duty ratio D higher than 50%, internal slope compensation is applied.
- **Latch Input:** The LATCH pin feature allows the additional external OVP and OTP protections. If this pin is between 0.8 V and 2.5 V (when not connected, it is at 1.2 V), the output drive pulses are active. An external NTC can be used to pull it below 0.8 V for OTP and a Zener diode to the bias voltage can be used to detect output OVP condition and shut down the pulses. A decoupling capacitor C100 can be used to filter an induced noise to node where the latch pin is connected. A precharge current I_{NTC(SSSTART)} is applied to the C1 during the soft-start period to charge the decoupling capacitor and avoid false triggering of the OTP protection. Maximum recommended value of C1 is 1.04 µF. It is important to note that during soft-start period the OTP is not activated.
- **Skip Mode:** This burst mode is used under no-load conditions or light-load conditions to increase the total efficiency and no-load input power.
- **Off-Mode:** If the voltage at feedback pin decreases below 0.4 V, the controller enters the off-mode, which allows reaching extremely low no-load input power. This feature enables the remote shut-down as well.

Low No-Load Mode Input Consumption of the Adapter Utilizing NCP1236

Firstly, let us analyze no-load power losses of notebook adapter using the NCP1236 controller without any energy saving feature. This analysis helps to understand the design space for improvements to achieve the low no-load input consumption. The schematic of this adapter is shown in Figure 1. The typical no-load input power consumption is 70 to 80 mW at high input line 230 V_{ac,rms}/50 Hz for such a design. The following analysis will show the main losses contributors under high line conditions 230 V_{ac,rms}/50 Hz:

- **Primary Controller Consumption:** The controller usually runs in skip mode in no-load, thus its consumption is around 0.9 mA from the V_{CC} supply. Then the primary control consumption can be easily calculated:

$$P_{PC} = V_{CC} \cdot I_{CC3} = 13.7 \cdot 0.9 \cdot 10^{-6} = 12.3 \text{ mW} \quad (\text{eq. 1})$$

- **Primary HV Sensing Consumption:** This part of no-load consumption can be divided in two parts. The first one is the high voltage sensor consumption which has resistive character and the second one is the bias consumption which has the character of the current sink.

$$P_{HV\text{sense}} = \frac{V_{HV,rms}^2}{R_{HV}} = \frac{230^2}{30 \cdot 10^6} = 1.76 \text{ mW} \quad (\text{eq. 2})$$

$$P_{HV\text{bias}} = V_{HV,av} \cdot I_{bias} = \frac{2\sqrt{2}}{\pi} \cdot V_{HV,rms} \cdot I_{bias} = \frac{2\sqrt{2}}{\pi} \cdot 230 \cdot 10 \cdot 10^{-6} = 2.1 \text{ mW} \quad (\text{eq. 3})$$

The primary controller is analyzed. The following part will examine other components of the primary no-load consumption, this time, from the front-end side.

- **Leakages:** The leakage of all the branch components (between the L and N) should not be neglected. It can affect the no-load consumption. Let us consider the varistor R5 leakage power loss $P_{leakVAR}$. The EPCOS type B72210P2301K101 is used and the datasheet provides information about its isolation resistance 100 MΩ.

$$P_{leakVAR} = \frac{V_{ac,rms}^2}{R_{var}} = \frac{230^2}{100 \cdot 10^6} = 0.53 \text{ mW} \quad (\text{eq. 4})$$

- **Input EMI Filter Consumption:** The losses in the input EMI filter are caused by the dielectric polarization losses in the X2 capacitors and losses caused by flow of the X2 capacitors reactive current through their equivalent serial resistance ESR and the dc resistances of the common mode choke R_{DC} . The loss in the X2 capacitor can be calculated using the dissipation factor $tg\delta$. The EMI suppression capacitors from EPCOS which are used are of the B32922C3104K type with dissipation factor $tg\delta \cdot 10^{-3}$. The loss in one X2 capacitor is:

$$P_{loss,X2} = tg\delta \omega C_{X2} V_{ac,rms}^2 = 1 \cdot 10^{-3} \cdot 2 \cdot \pi \cdot 50 \cdot 100 \cdot 10^{-9} \cdot 230^2 = 1.66 \text{ mW} \quad (\text{eq. 5})$$

The values of reactive current I_{CX2} and reactive power $P_{react,X2}$ are also important.

$$I_{CX2} = \omega C_{X2} V_{ac,rms} = 2 \cdot \pi \cdot 50 \cdot 100 \cdot 10^{-9} \cdot 230 = 7.23 \text{ mA} \quad (\text{eq. 6})$$

$$P_{react,X2} = \omega C_{X2} V_{ac,rms}^2 = 2 \cdot \pi \cdot 50 \cdot 100 \cdot 10^{-9} \cdot 230^2 = 1.66 \text{ VAR} \quad (\text{eq. 7})$$

Loss on DC resistance R_{DC} of the used common choke L2 type B82734W2202B030 from EPCOS are:

$$P_{loss,L2} = 2R_{DC} I_{CX2}^2 = 2 \cdot 0.24 \cdot 0.0723^2 = 0.025 \text{ mW} \quad (\text{eq. 8})$$

But its reactive power $P_{react,L2}$ caused by the stray inductance is negligible:

$$P_{react,L2} = \omega L_{stray} I_{CX2}^2 = 2 \cdot \pi \cdot 50 \cdot 105 \cdot 10^{-6} \cdot 0.0723^2 = 1.7 \text{ μVAR} \quad (\text{eq. 9})$$

- **Primary X2 Capacitor Discharge Branch**

Consumption: This branch consists of the serial resistors RD100, RD101, and RD102.

This consumption can be simply derived.

$$P_{disch} = \frac{V_{ac,rms}^2}{R_{dis}} = \frac{230^2}{2.46 \cdot 10^6} = 21.5 \text{ mW} \quad (\text{eq. 10})$$

- **Leakage of the Bulk Capacitor:** The dc leakage of the bulk capacitor on the primary side is a quite important topic. The aluminum electrolytic capacitors are often used as a bulk capacitor. Many vendors specifies its maximum dc leakage current I_{leak} at a temperature of 20°C after 5 minutes of biasing at nominal voltage by following formula: (it is valid for aluminum electrolytic capacitor with maximum voltage higher than 100 V)

$$I_{leak} = 0.02CV + 15 [\mu A; \mu F, V] \quad (\text{eq. 11})$$

The last term in the formula can differ from vendor to vendor. The bulk capacitor CB1 value 100 μF/400 V was designed. The selected one was the aluminum electrolytic type EKXG401ELL101MMN3S from Nippon Chemi-Con. The dc leakage I_{leak} value of this capacitor was calculated 82 μA, based on its datasheet. A similar type for replacement B43044A9107M000 from EPCOS has 815 μA.

$$P_{leakBulk} = V_{HVmax} I_{leak} = \sqrt{2} V_{HVrms} I_{leak} = \sqrt{2} \cdot 230 \cdot 825 \cdot 10^{-6} = 268 \text{ mW} \quad (\text{eq. 12})$$

This calculated consumption is the worst case with a huge margin. The real measurements show the dissipation at bulk capacitor around 1 mW.

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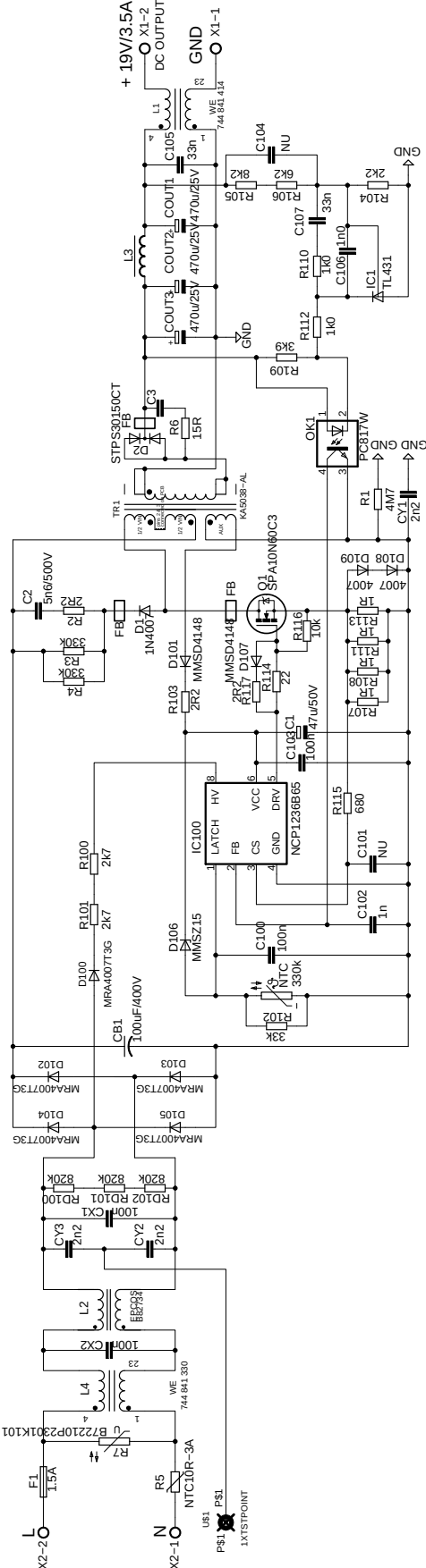


Figure 1. The Notebook Adapter Schematic using the NCP1236 Controller

- **Leakage of the Primary Switch:** The primary switch Q1 leakage dissipation loss calculation is shown to complete this detailed analysis. The maximum DC leakage of the used type SPP11N60C3 from Infineon is 1 μ A, so the primary switch Q1 power dissipation caused by leakage is negligible.

$$P_{\text{leakQ1}} = V_{\text{HVmax}} I_{\text{leak}} = 325 \cdot 1 \cdot 10^{-6} = 0.33 \text{ mW} \quad (\text{eq. 13})$$

The analysis further continues with the secondary consumption.

- **Secondary Control Consumption:** The first part of the secondary consumption in no-load mode is the secondary controller current. It is given by the TL431 bias current and the opto-coupler LED current needed to pull down the primary controller FB pin. Let us assume the CTR of this opto-coupler is 50% and typical FB pin pull-up current 250 μ A, then the needed secondary opto-coupler LED current is 0.5 mA. Consumption of secondary control is:

$$P_{431} = V_{\text{OUT}} \cdot \left(\frac{V_{\text{LED}}}{R_{\text{bias}}} + I_{\text{LED}} \right) \cdot \frac{V_{\text{LED}}}{R_{\text{bias}}} =$$

$$= 19 \cdot \left(\frac{0.9}{3.9 \cdot 10^3} + 0.5 \cdot 10^{-3} \right) = 13.88 \text{ mW} \quad (\text{eq. 14})$$

The second component of the secondary consumption in no-load mode is the branch current through the feedback divider.

$$P_{\text{OUTdiv}} = \frac{V_{\text{OUT}}^2}{R_{\text{div}}} = \frac{19^2}{16.6 \cdot 10^3} = 21.74 \text{ mW} \quad (\text{eq. 15})$$

NOTE: The indicating LED is not used in many adapters due to its huge consumption if it is supplied by the steady dc current. Let us assume 5 mA of the dc LED current.

$$P_{\text{LED}} = V_{\text{OUT}} \cdot I_{\text{LED}} = 19 \cdot 5 \cdot 10^{-3} = 95 \text{ mW} \quad (\text{eq. 16})$$

This is a huge number. This needs to be recalculated to the primary side considering the efficiency of the power supply. The additional component 158 mW of the no-load input power consumption appears. The purpose which is to reach the minimum no-load consumption is diminished by the usage of such LED driving. It is possible to use dedicated secondary controllers to drive the LED by current pulses only, and thus significantly decrease the consumption. ON Semiconductor offers a dedicated family of the secondary controllers with such a built-in LED driver of the NCP435X devices family.

The following part will provide a summary of all previously calculated numbers and obtain the expected no-load input power consumption.

Table 1. SUMMARY OF THE NO-LOAD CONSUMPTION ANALYSIS FOR THE ADAPTER USING NCP1236 CONTROLLER

Component	Consumption	
Varistor	P_{leakVAR} [mW]	0.53
EMI Filter - X2 Capacitors	$2 \times P_{\text{loss,X2}}$ [mW]	3.32
EMI Filter - L2 Common Choke	$P_{\text{loss,L2}}$ [mW]	0.025
X2 Discharge Branch	P_{disch} [mW]	21.5
Bulk Capacitor DC Leakage Loss	P_{leakBulk} [mW]	1
Q1 Leakage Loss	P_{leakQ1} [mW]	0.33
Primary Controller - HV Bias	P_{HVbias} [mW]	2.1
Primary Controller - HV Sense	P_{HVsense} [mW]	1.76
Primary Controller - V_{CC} Consumption	P_{PC} [mW]	12.3
Secondary Controller - TL431	P_{431} [mW]	13.88
Secondary Divider	P_{div} [mW]	21.74
Transfer Efficiency	η [%]	60
Transfer to Primary	P_{prim} [mW]	79.9
Total No-Load Input Power	P_{in} [mW]	110.4

Having consulted Table 1, the major contributors to the no-load input power can be identified. They are the X2 capacitor discharging resistive branch, primary controller consumption, secondary controller consumption, and branch current through the secondary voltage feedback divider. The optimization for the low no-load input power was performed at these fields:

- **The X2 Capacitor Discharging** resistive branch was totally removed from application and was replaced by the primary controller device integrated feature.
- **The Primary Controller** was optimized for the lowest consumption from the V_{CC} circuitry and the dedicated off-mode was added.
- **The Energy Saving Hiccup Mode** was chosen for the secondary control under the no-load condition to save the input power and keep the ability to detect the load connected to output and restart the primary controller.
- **The Secondary Voltage Feedback Divider** branch current was optimized to obtain the low consumption and still keep the reasonable transient responses and herewith noise and EMC immunity.

The total no-load input power calculated value 110 mW noticeably differs from the measured value 87.9 mW under the same high input line conditions. The root cause of the difference lies in the analysis approach because all the calculations were done for the worst cases values from datasheets (the typical values are not usually mentioned for such parameters as leakages or isolation resistances).

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Description of the Design Solution Utilizing NCP1246

The solution was implemented utilizing a flyback topology, granting the advantage of a quite high density power design. The design operates in both CCM (continuous conduction mode) and DCM (discontinuous conduction mode) allowing it to accept a wide universal input voltage range.

The CCM operation provides a desired full load performance with good efficiency and a low ripple of primary current. The DCM operation permits an increase of efficiency under the light-load conditions by decreasing the switching losses. The device switches at 65 kHz, which represents a good trade-off between switching losses, magnetic size and the EMI.

The NCP1246 fixed frequency controller was selected to achieve the design requirements. This device is housed in a SOIC 7 leads that includes multiple features including input ac line sensing. The electrical schematic of the adapter board is shown in Figure 2.

The adapter consists of several important sections. The first one is an **input EMI filter** which reduces the conducted EMI to the ac line at the input of the adapter. The EMI filter is formed by 2 common-mode inductors L4 and L2 and capacitors CX1, CX2. The varistor R5 is used to protect the adapter against the line overvoltage peaks and NTC R6 is not used to increase the full load efficiency. The L4 inductor is used to filter the RF components of the conducted EMI.

The next block is the **rectifier** with a bulk capacitor. The HV pin of the controller NCP1244/46 is sensing the voltage in front of the rectifier. HV pin must observe full wave rectified ac signal to ensure the correct functionality of built-in X2 capacitors discharge circuitry. The HV pin must not be connected to dc voltage. It will cause activation of X2 capacitors discharge circuitry and a consequent outbreak of the device by long term overheating.

The main power stage of the **flyback converter** utilizes the SPP11N60C3 MOSFET from Infineon along with a custom designed transformer TR1 type KA5038-BL from Coilcraft company. **Secondary rectification** is provided by a low drop Schottky diode NTST30100SG from ON Semiconductor. A simple RC snubber across the secondary rectifier damps any high frequency ringing caused by the unclamped leakage inductance at secondary side of the transformer.

The programmable reference NCP431 from ON Semiconductor ensures the output voltage regulation. The NCP431 output is coupled via the opto-coupler to the controller of the NCP1246B 65 kHz version. The last stage of the adapter is the output filter consisting of primary filter capacitors COUT2 and COUT3, and secondary filter made up of L3, and COUT1. The output common choke L1 decreases the radiated EMI by preventing the flow of asymmetric radiating current into the floating load.

The Off-Mode Principle

If the voltage at feedback pin decreases below 0.4 V, the controller enters the off-mode allowing reaching extremely low no-load input power consumption. The internal V_{CC} is turned-off, the IC consumes extremely low V_{CC} current and only the voltage at external V_{CC} capacitor is maintained by the Self-Supply circuit. The Self-Supply circuit keeps the V_{CC} voltage at the $V_{CC(Reg)}$ level. The supply for the FB pin watch dog circuitry and FB pin bias is provided via the low consumption current sources from the external V_{CC} capacitor. The controller can start only if the FB pin voltage increases above the 2.2 V level.

The protection timer GoToOffMode t_{GTOM} is used to protect the application against the false activation of the low consumption off-mode by the fast drop outs of the FB pin voltage below the 0.4 V level e.g. in case the high FB pin voltage ripple is present during the skip mode.

The secondary circuitry regulates the primary controller so that it can enter off-mode or leave this mode via the feedback opto-coupler. The additional circuitry is needed to detect the no-load condition and control the opto-coupler so that the primary controller can enter off-mode or rouse the primary controller.

The no-load condition is detected via the peak detector formed by diode D102, capacitor C2, and the load consisting of R111 and R112. The time constant given by the capacitor C2, and its load R111, and R112 defines the time detection level from which the hiccup mode starts. The voltage across capacitor C2 is dropping while no positive voltage pulses are present at secondary winding for a set time period. This time period is set by the time constant of circuitry consisting of C2, R105, R107, R111, and R112. The voltage across C2 drops and causes the closing of the switch Q100 and consequently turning-on of the current source Q101. The current source Q101 forces a permanent lighting of the opto-coupler LED and consequently pulls down the FB pin. GoToOffMode timer t_{GTOM} (inside the primary controller) starts to count down when the pulled-down FB voltage crosses the 0.4 V level. The off-mode starts when this timer elapses. The primary controller is kept off now, zero energy is transferred via the transformer and the output voltage starts to fall down slowly. Its decreasing is caused by the self consumption of the secondary control circuitry.

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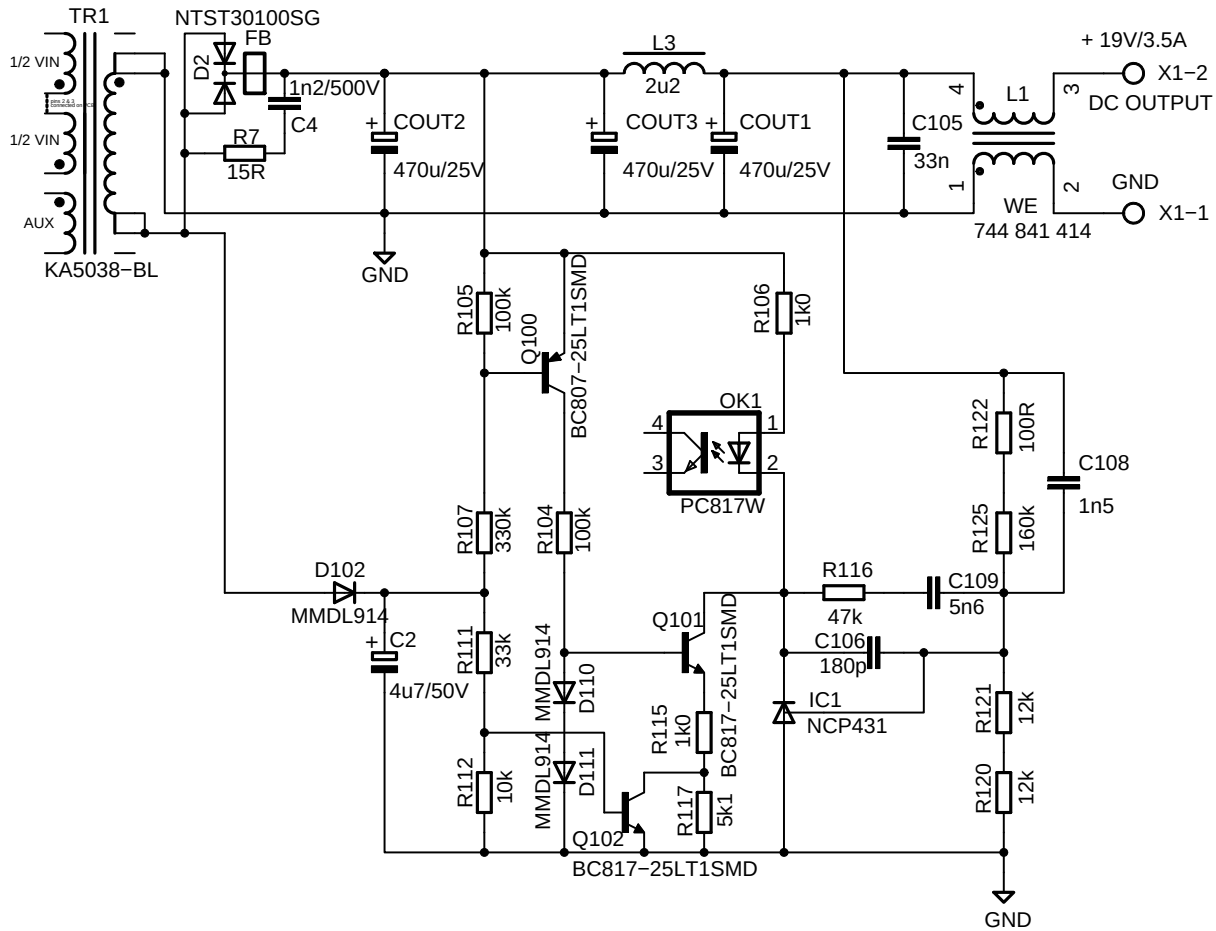


Figure 3. Secondary Control Circuitry

The switch Q102 is used to decrease the opto-coupler LED current in case it is in off-mode when the FB pin is pulled up by 5 μ A current only. More energy is saved at the secondary side now. The circuitry created by diode D101, capacitor C107 and resistor R114 forms the secondary voltage regulator NCP431 dynamic biasing, but it is not used in this design. It has to stop the biasing of the secondary voltage regulator NCP431 under the skip mode and save the power consumption in skip modes and off-modes. The NCP431 has good dynamic performance so that the additional bias at normal operation is not needed. Hence this type of circuitry was not assembled.

The hiccup cycle ends when the output voltage is so small that the LED current fades away. When the opto-coupler LED current fades away the FB is no longer pulled down by closed transistor inside the opto-coupler and FB pin voltage starts to rise up being pulled up by the internal 5 μ A current source. When the FB pin voltage crosses the 2.2 V level, the primary controller restarts and recharges the secondary capacitors tank. This cycling repeats in the hiccup mode. If any load is connected, the discharge of the output capacitors tank is faster and after recharge of the output capacitors, the application enters the regulated mode and keeps the output voltage at the required level set by the voltage feedback loop.

The X2 Capacitor Discharge Principle

This feature saves approximately 16–25 mW of input power depending on the EMI filter X2 capacitors volume and it saves the external components count as well. The discharge feature is ensured via the start-up current source with a dedicated control circuitry for this function.

The dedicated structure called ac line unplug detector is used inside the X2 capacitor discharge control circuitry. See Figure 5 for the block diagram of this structure and Figure 6 for the timing diagram. The basic idea of ac line unplug detector lies in comparison of the direct sample of the high voltage obtained via the high voltage sensing structure with the delayed sample of the high voltage. The delayed signal is created by the sample & hold structure.

One can ask why such a complicated method is used. Why is the regular crossing of the voltage level close to zero not simply detected? See the following picture showing the rectified ac signal in the power supply loaded by high impedance.

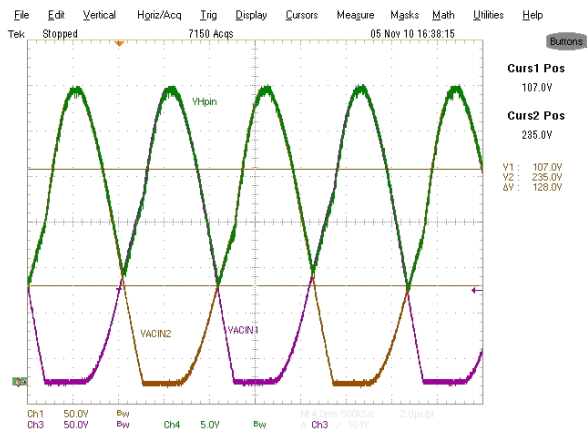


Figure 4. Full Wave Rectified ac Line Voltage at High Impedance HV Pin

The problem is that the rectified voltage at a high impedance HV pin never reaches zero level. This situation is even worse if a small capacitance is present at the HV pin. The no zero reaching is caused by the floating of the primary controller common node GND. The floating is caused by the charging and discharging of the CY1, CY2 and CY3 capacitors. The actual status of charging and discharging those capacitors forms the actual slope of signal at HV pin.

The comparator used for the comparison of these signals is without a hysteresis inside. The resolution between the slopes of the ac signal and dc signal is defined by the sampling time T_{SAMPLE} and additional internal offset N_{OS} . These parameters ensure the noise immunity as well. The additional offset is added to the signal sampled and divided from HV pin and its analog sum is stored in the C_1 storage capacitor. If the voltage level of the HV sensing structure output crosses this level, the comparator CMP output signal resets the detection timer which provides the low level of DC detect signal. It means that ac signal is present at the HV pin and the X2 discharge sequence is disabled.

The additional offset N_{OS} can be measured as the $V_{HV(hyst)}$ at the HV pin. If the comparator output produces pulses, it means that the slope of input signal is higher than the set resolution level and the slope is positive. If the comparator output produces a low level, it means that the slope of input signal is lower than the set resolution level or the slope is negative. The detection timer is used which is reset by any edge of the comparator output. It means that if no edge comes before the timer elapses, there is only a dc signal present or a signal with a small ac ripple at the HV pin. This type of ac detector detects only the positive slope which fulfils the requirements for the ac line presence detection.

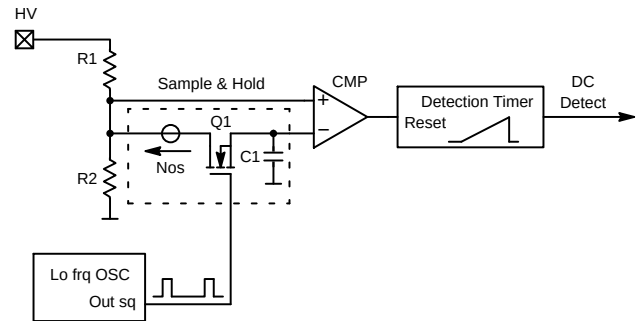


Figure 5. The ac Line Unplug Detector Structure Used for X2 Capacitor Discharge System

The X2 capacitor discharge feature is enabled in any controller operation mode to ensure the compliance with the safety requirement. The detection timer is reused to limit the time of the discharge phase, which protects the device against overheating. The discharging process is cyclic and continues until the ac line is detected again or the voltage across the X2 capacitor is lower than $V_{HV(min)}$. **It is important to note that it is not allowed to connect the HV pin to any dc voltage e.g. directly to bulk capacitor.** Please refer to the NCP1244 or NCP1246 datasheets if more details are needed.

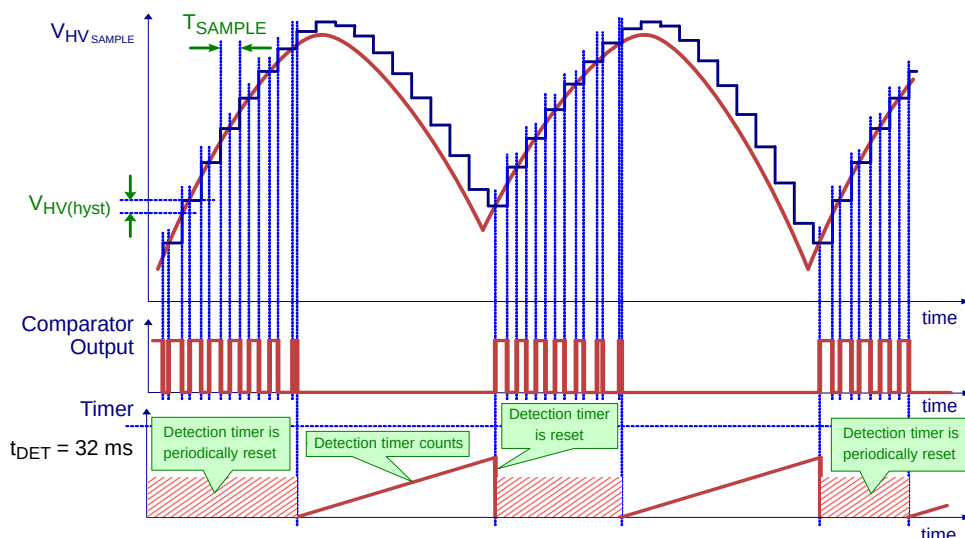


Figure 6. The ac Line Unplug Detector Timing Diagram

The X2 Capacitor Discharge System Capability

The time needed to discharge the X2 capacitors in the EMI filter is very important from the safety point of view. The safety standards can vary from country to country and one of the very common ones is to discharge the X2 capacitors bank at least to 50 Vdc in 500 ms. The X2 capacitors are discharged by the HV startup circuitry by I_{start2} current. The discharge process is periodic with the 32 ms detection period and 32 ms discharge period to prevent the overheating of the device and a fault when the whole application is plugged into mains again.

The time t_{dis} needed to discharge a certain amount of capacitance can be calculated by the following formula:

$$t_{dis} = \frac{C_{X2} \cdot \Delta V}{I_{start2}} \quad (\text{eq. 17})$$

ΔV means the difference between the mains maximum peak voltage and residual voltage at X2 capacitors bank allowed by safety standard. The maximum allowed capacitance, which could be discharged in the specified time period, can be calculated by the following formula:

$$C_{X2} = \frac{I_{start2} \cdot t_{dis}}{\Delta V} \quad (\text{eq. 18})$$

The minimum voltage to which the X2 capacitors can be discharged is given by $V_{HV(min)}$. It is the minimum level for HV startup current source functionality.

Estimated No-Load Mode Input Consumption in Solution Utilizing NCP1246

Let us analyze the consumption of the whole adapter again. The adapter using hiccup mode for no-load loading condition has been analyzed. The consumption of the secondary control circuitry can be modeled as composition of the current sink and resistor. The current sink models consumption of the branch with the opto-coupler LED which is supplied by the current source formed by the Q101. The resistor models the consumption of all the resistive branches in the secondary control. The first branch is formed by R112, R111, R107 and R105. The second branch is R104 because the drop across D110, D111 and Q100 is neglected due to the simplicity. The last branch consists of the feedback divider R120, R121, R125 and R122. All these branches in parallel give the resistance $R = 56.99 \text{ k}\Omega$.

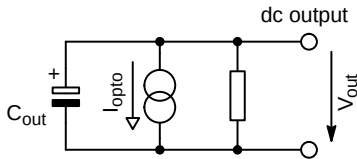


Figure 7. Simplified Diagram of the Output for the Consumption Analysis

The I_{opto} sink current is calculated by the following formula:

$$I_{opto} = \frac{V_{D111} + V_{D110} - V_{be,Q101}}{R_{115} + R_{117}} = \frac{0.7 + 0.7 - 0.7}{1 \cdot 10^3 + 5.1 \cdot 10^3} = 115 \mu\text{A} \quad (\text{eq. 19})$$

The hiccup mode period can be, this time, calculated by the following formula:

$$t_{hiccup} = -RC_{out} \ln \left(\frac{V_{out,min} + RI_{opto}}{V_{out} + RI_{opto}} \right) \quad (\text{eq. 20})$$

$$t_{hiccup} = -56.99 \cdot 10^3 \cdot 1.5 \cdot 10^3 \cdot \ln \left(\frac{2 + 56.99 \cdot 10^3 \cdot 115 \cdot 10^{-6}}{19 + 56.99 \cdot 10^3 \cdot 115 \cdot 10^{-6}} \right) = 93.6 \text{ s} \quad (\text{eq. 21})$$

The required no-load power for the secondary circuitry will be calculated by the energy law. The energy stored in the output capacitor tank (when it is fully charged to nominal output voltage) is:

$$E_1 = \frac{1}{2} C_{out} V_{out}^2 = \frac{1}{2} \cdot 1.5 \cdot 10^{-3} \cdot 19^2 = 0.270 \text{ J} \quad (\text{eq. 22})$$

The rest of energy stored in the output capacitor tank (when it is discharged to minimum output voltage) is:

$$E_2 = \frac{1}{2} C_{out} V_{out,min}^2 = \frac{1}{2} \cdot 1.5 \cdot 10^{-3} \cdot 2^2 = 0.003 \text{ J} \quad (\text{eq. 23})$$

Thus the required power for charging the output capacitor tank is:

$$P_{sec} = \frac{E_1 - E_2}{t_{hiccup}} = \frac{0.270 - 0.003}{93.6} = 2.85 \text{ mW} \quad (\text{eq. 24})$$

This amount of power contributes to input power of the adapter. Nevertheless it appears at input increased by the transfer losses. Let us assume the efficiency of 60% for the transfer from the primary circuitry, thus the contribution of the secondary circuitry to no-load consumption is 4.8 mW. Then the estimated total no-load input power is around 19 mW.

Table 2. SUMMARY OF THE NO-LOAD CONSUMPTION ANALYSIS FOR THE ADAPTER USING NCP1246 CONTROLLER

Component	Consumption	
Varistor	$P_{leakVAR} \text{ [mW]}$	0.53
EMI Filter - X2 Capacitors	$2 \times P_{loss,X2} \text{ [mW]}$	3.32
EMI Filter - L2 Common Choke	$P_{loss,L2} \text{ [mW]}$	0.025
X2 Discharge Branch	$P_{disch} \text{ [mW]}$	0
Bulk Capacitor DC Leakage Loss	$P_{leakBulk} \text{ [mW]}$	1
Q1 Leakage Loss	$P_{leakQ1} \text{ [mW]}$	0.33
Primary Controller - HV Bias	$P_{HVbias} \text{ [mW]}$	2.1
Primary Controller - HV Sense	$P_{HVsense} \text{ [mW]}$	1.76
Primary Controller - Vcc Consumption	$P_{PC} \text{ [mW]}$	5.17
Secondary Control	$P_{sec} \text{ [mW]}$	2.85
Transfer Efficiency	$\eta \text{ [%]}$	60
Transfer to Primary	$P_{prim} \text{ [mW]}$	4.8
Total No-Load Input Power	$P_{in} \text{ [mW]}$	19.0

The total no-load input power calculated value is 19 mW. The previous solution utilizing NCP1236 flyback controller has no-load input power of 110 mW. The major power saving contributors are:

- The X2 Discharge Resistor Branch was Removed
- The Hiccup Mode at Output Stage when the Adapter is Unloaded was Implemented
- The Off-mode Inside Primary Controller was Implemented

Power Meter YOKOGAWA WT210 Analysis of Measurement Precision

The efficiency and no-load input power consumption were measured by the YOKOGAWA WT210 power meter. However, a significant error appeared during the no-load input power measurement due to high input reactive power of the input EMC filter (3.32 VAR). This effect can cause a significant error at read value of no-load input power. How significant can such an error be?

The YOKOGAWA WT210 Power Meter Specification Declares:

Active Power Accuracy:

- $\pm(0.1\% \text{ rdg} + 0.1\% \text{ rng})$ for $45 \text{ Hz} \leq f \leq 66 \text{ Hz}$

Influence of Power Factor PF:

- $\pm 0.2\%$ of VA for $45 \text{ Hz} \leq f \leq 66 \text{ Hz}$ when $PF = 0$
- $\pm(\tan\Phi \times \text{influence when } PF = 0)\%$ rdg when $0 < PF < 1$

Where Φ is the phase angle of the voltage and current.

Let us assume the voltage range setting of 300 V and the current range setting of 20 mA. It gives the power range of 6 W. Assuming that the read value will be around 30 mW, the error given by the reading precision is negligible. The next analysis takes into account only the measurement range precision and influence of the power factor.

Active Power Accuracy for Given Example:

- $\pm 6 \text{ mW}$ for $45 \text{ Hz} \leq f \leq 66 \text{ Hz}$

Influence of Power Factor PF:

- $\pm 0.2\%$ of 3.32 VAR means $\pm 6.64 \text{ mW}$

Then, the maximum total error is 12.2 mW in a 6 W measurement range if the no-load input power is directly measured. The relative precision of such a measurement

defined by the YOKOGAWA WT210 power meter specification is $\pm 61\%$ when we measure no-load input power in range of 20 mW. The results of such a direct no-load input power measurement vary quite a lot and provide a wrong result in the hiccup mode because the output capacitor charging bursts are hardly measurable that way. In addition, the measurement range of the current has to be increased to measure the correct active power value.

A more precise method for the hiccup mode uses an integration approach. The YOKOGAWA WT210 power meter allows measuring consumed energy in the no-load mode using the long integration time. The usual approach is to start the measured adapter or the power supply first, let it warm up approximately for one hour and then start the measurement. The set integration time is from 20 minutes to 10 hours. This method provides more repeatable results; with the spread of measured values up to $\pm 2 \text{ mW}$. This is one of the generally used and accepted ways how to evaluate very low value of no-load active input power. The best way how to evaluate the no-load input power consumption in a hiccup mode could be the dynamic and fast change of current range. This feature can ensure that the wattmeter measures precisely when the controller is in off-mode and the power meter is not overloaded during the bursts.

Let us analyze the precision of power meter YOKOGAWA WT210 specified by the manufacturer.

Accuracy of Integration:

- $\pm(\text{power (current) accuracy} + 0.1\% \text{ of reading})$

Accuracy fo Timer:

- $\pm 0.02\%$

It is necessary to increase the current range to 2 A to catch the bursts of the input consumption when the output capacitor tank is being recharged in the hiccup mode. The power range increases to 600 W as well and the power accuracy is now 600 mW. This number is 30 times higher than the measured value, thus the measured value can be affected by a significant error. The maximum possible value of the error can exceed the regulators' requirements. It means that the measurement which was performed by the world-wide standard and used the power meter YOKOGAWA WT210 has only an informative value. The results can significantly differ from one power meter to another.

Efficiency and No-Load Consumption

Table 3. EFFICIENCY VS. OUTPUT POWER AND INPUT LINE VOLTAGE

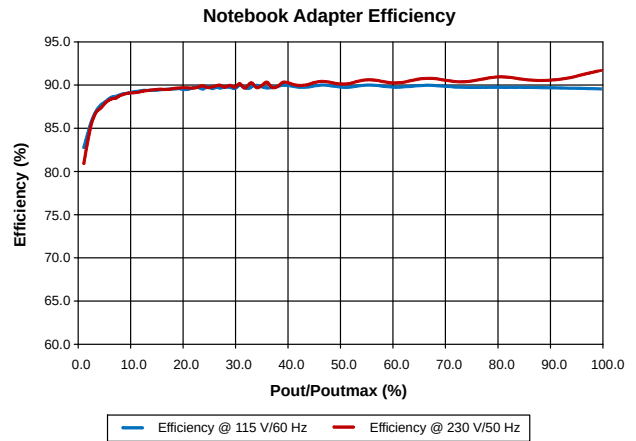
$V_{in} = 115 V_{ac}/60 \text{ Hz}$			
P_{out}/P_{outmax} [%]	P_{out} [W]	P_{in} [W]	Efficiency [%]
100.7	65.43	73.10	89.51
75.5	49.05	54.68	89.71
50.1	32.58	36.31	89.74
25.7	16.69	18.63	89.57
10.6	6.90	7.74	89.19
5.4	3.52	4.00	89.12
1.5	0.97	1.15	83.97
0.7	0.48	0.60	80.19
$V_{in} = 230 V_{ac}/50 \text{ Hz}$			
P_{out}/P_{outmax} [%]	P_{out} [W]	P_{in} [W]	Efficiency [%]
100.7	65.43	71.20	91.89
75.4	49.04	54.17	90.53
50.1	32.57	36.14	90.13
25.7	16.69	28.58	89.81
10.6	6.91	7.75	89.11
5.4	3.54	4.02	88.03
1.5	0.97	1.16	83.12
0.7	0.49	0.63	77.44

Table 4. AVERAGE EFFICIENCY AND NO-LOAD INPUT POWER

Input Line	115 $V_{ac}/60 \text{ Hz}$	230 $V_{ac}/50 \text{ Hz}$
Average Efficiency	89.6%	90.6%
No-Load Input Power	8.41 mW	16.22 mW

The total input power is lower than the goal 30 mW. The difference between the calculated value and the measured value is 2.78 mW at high line, which means 17.1% from the measured value. The results are adequately similar, if all effects affecting the measurement precision are considered. The extremely low no-load input power is obtained thanks to an output voltage hiccup mode when there is no-load connected. The loading current borderline values to detect the no-load condition are the following:

- 3.1 mA Going to Hiccup Mode
- 36.9 mA Leaving the Hiccup Mode

**Figure 8. Efficiency vs. Output Power and Input Line Voltage**

The observed “waves” at the efficiency curves in the range from 25% of loading are caused by the fact that the primary switch is turned on in case the voltage values at the drain node are different. If the controller switches in the valley of the drain voltage in the DCM mode, the efficiency of the adapter is higher. When the controller switches in the peak, the total efficiency decreases in opposite case.

The High Voltage Pin Sensitivity to Noise

The high voltage sensing pin HV has a big internal impedance to reach the extremely low input power consumption while the power supply is in idle mode. The input impedance of the HV pin is typically 30 MΩ and the typical leakage current 10 μA is present as well. Such high impedance creates a small power loss and helps to decrease no-load input power. On the other hand, the high impedance pin is a disadvantage. It has high sensitivity to coupled noise. The noise can be coupled from the power stage or from the mains. The noise from the power stage is mainly coupled by the capacitive way. The noise from the mains comes through the unmatched EMI filter. There is a question, though, why the EMI filter is unmatched?

The EMI filter is usually designed/selected to decouple the switching frequency current noise and its higher harmonic components from the power stage to the mains. Every filter works well if it is properly matched at its both ports. The EMI filters in power supplies are matched well when the supply current flows through them. These filters are unmatched when its output connected to bridge rectifier is unloaded, which simply means that the diodes are not conducting any current. The noise from the mains can freely come through the filter this time.

The excessive noise coupled to the HV pin can cause the overpower compensation system to partially fail. The partial fail means that the overpower compensating current sourced by the CS pin will not be in line with the current peak voltage of the mains. A 3-bit A/D converter with the peak detector senses the ac input, and its output is periodically sampled and reset in order to follow closely the input voltage variations. The sample and reset events are given by the output from the ac line unplug detector. It can simply provide the information that the peak of input voltage passes. It will pass after the positive slope of input voltage has ceased. The sensed HV pin voltage peak value is validated when no HV edges from the comparator are present after the last falling edge during 2 sample clocks. Peak detector is reset by the first edge of the HV comparator. See Figure 11 and device datasheet [1] for details.

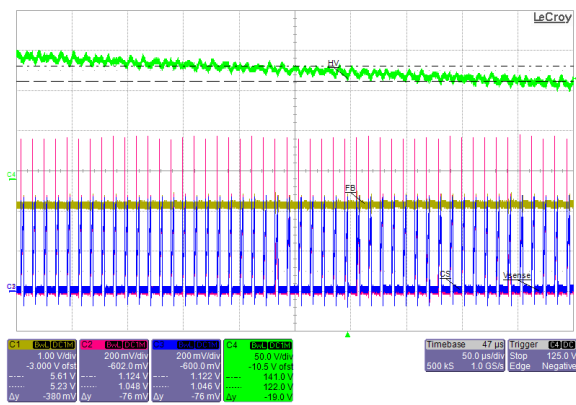


Figure 9. The Noise Coupled to HV Pin when the Diodes in Bridge Rectifier are not Conducting. EMI Filter is Unmatched.

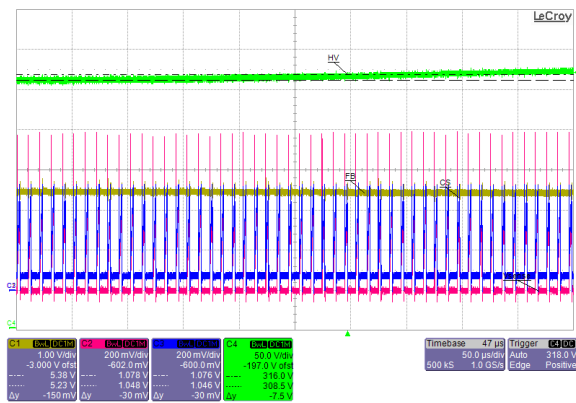


Figure 10. The Noise Coupled to HV Pin when the Diodes in Bridge Rectifier are Conducting. EMI Filter is Matched as Works Well.

The coupled noise to the HV pin can affect the overpower compensating system when its instantaneous value is higher than the sampled value in the ac detector system. The worst case that creates such an effect is the falling slope of the

voltage at the HV pin. The HV pin is connected via diodes D107, D108 to an unmatched EMC filter. It has an open output. All impedances connected to the HV pin are high and the amount of the coupled noise is the highest. The comparator output in the ac line detection system goes high and resets the peak detector when the instantaneous voltage value at the HV pin is higher than the HV sampled value. The watch dog signal generates the false maximum of the mains after 2 sample clocks. Consequently, the false overpower compensating current starts to be sourced out of the CS pin. Its value usually drops. See Figure 12 for your reference. The undesirable change of the overpower compensating current greatly depends on the phase shift between the sample clock and the HV pin voltage ripple/noise and the amount of the coupled noise.

The easiest way to decrease the noise coupling factor to the HV pin is to add the parallel decoupling capacitor. Such a capacitor is also increasing the surge immunity when it is a part of the T topology damping structure. The T topology filter damps the surge pulse by the serial and parallel branches and protects the HV pin structure against the high peak current from the decoupling capacitor when the breakdown voltage appears on it.

Overpower compensating current can decrease or even drop during the falling slope of voltage at the HV pin when the noise coupling is strong and the T topology filter is not used. The application will run for short periods without overpower compensation in such cases. The consequences of such a false incorrect overpower compensation were evaluated:

- The fault timer duration fluctuation was observed up to 5%
- Missing overpower compensation could cause transformer core saturation and a primary peak current increase in case of a tight design of the transformer. CSstop protection should stop the application in such a case. Please see [1], [2] for more details about CSstop protection
- The overpower compensating current causes output voltage overshoots/undershoots up to 50 mV. These overshoots/undershoots are heavily dependent on the input voltage and the transformer primary inductance
- The application always securely stops in case of overload thanks to the implementation of CSstop protection

Attention: The effect of the noise coupled to the HV pin described above is greatly dependant on the NCP1244/46 application schematic, PCB layout pattern, and overall application configurations. This effect was observed only in application with a stronger coupling of the noise to the HV pin.

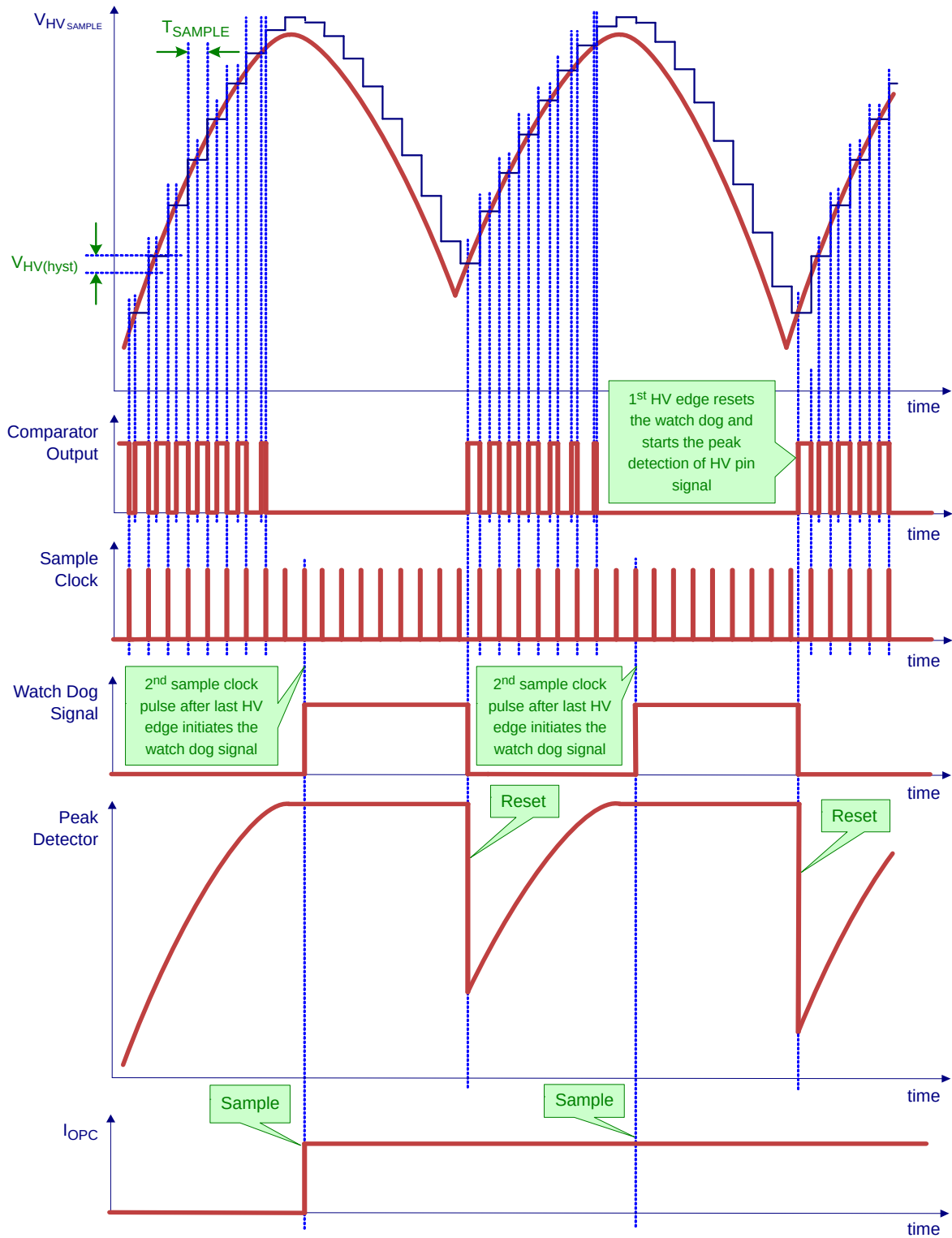


Figure 11. Overpower Compensation System Timing Diagram

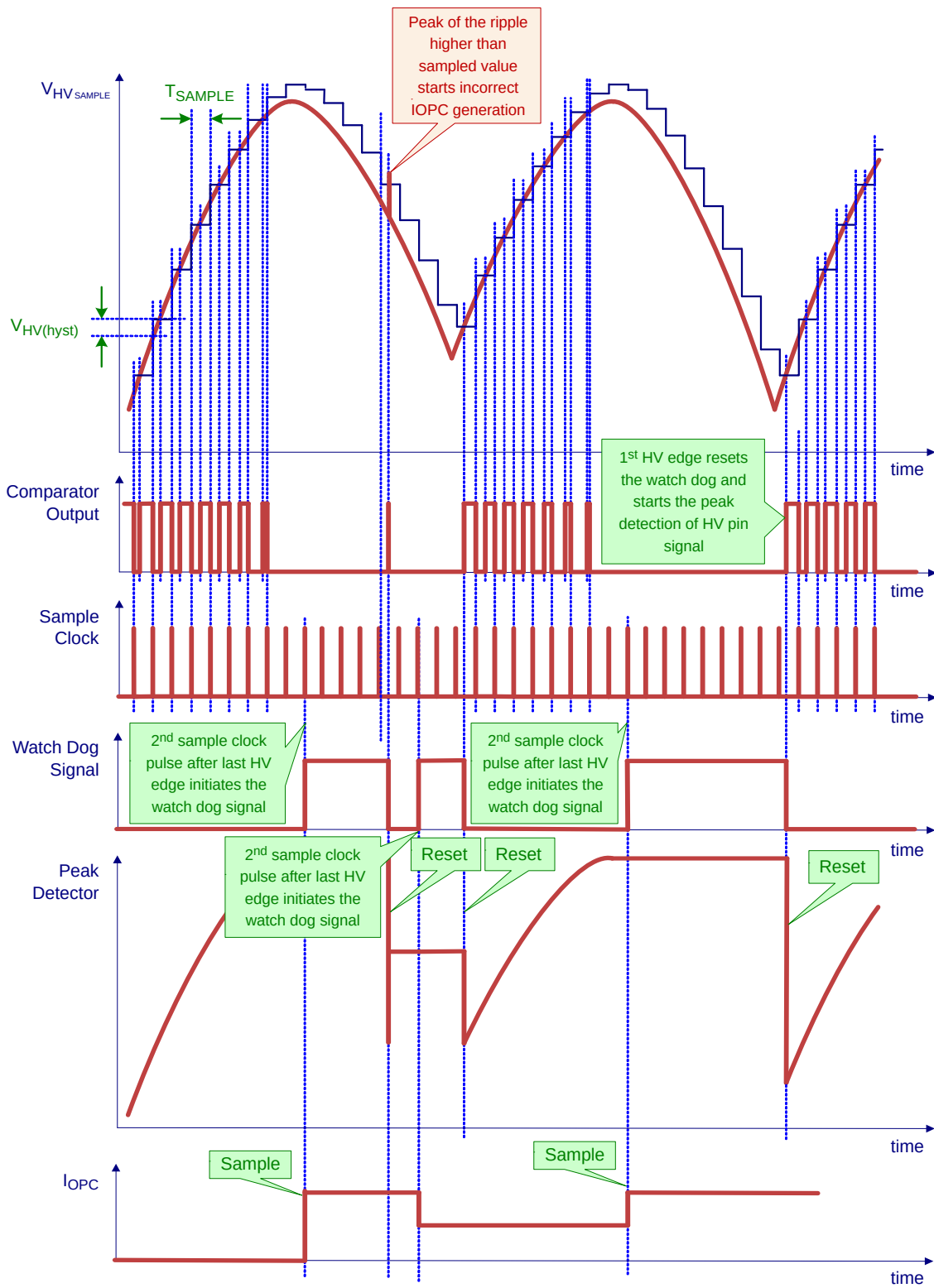


Figure 12. Overpower Compensation System is Affected by the Noise Coupled to the HV Pin

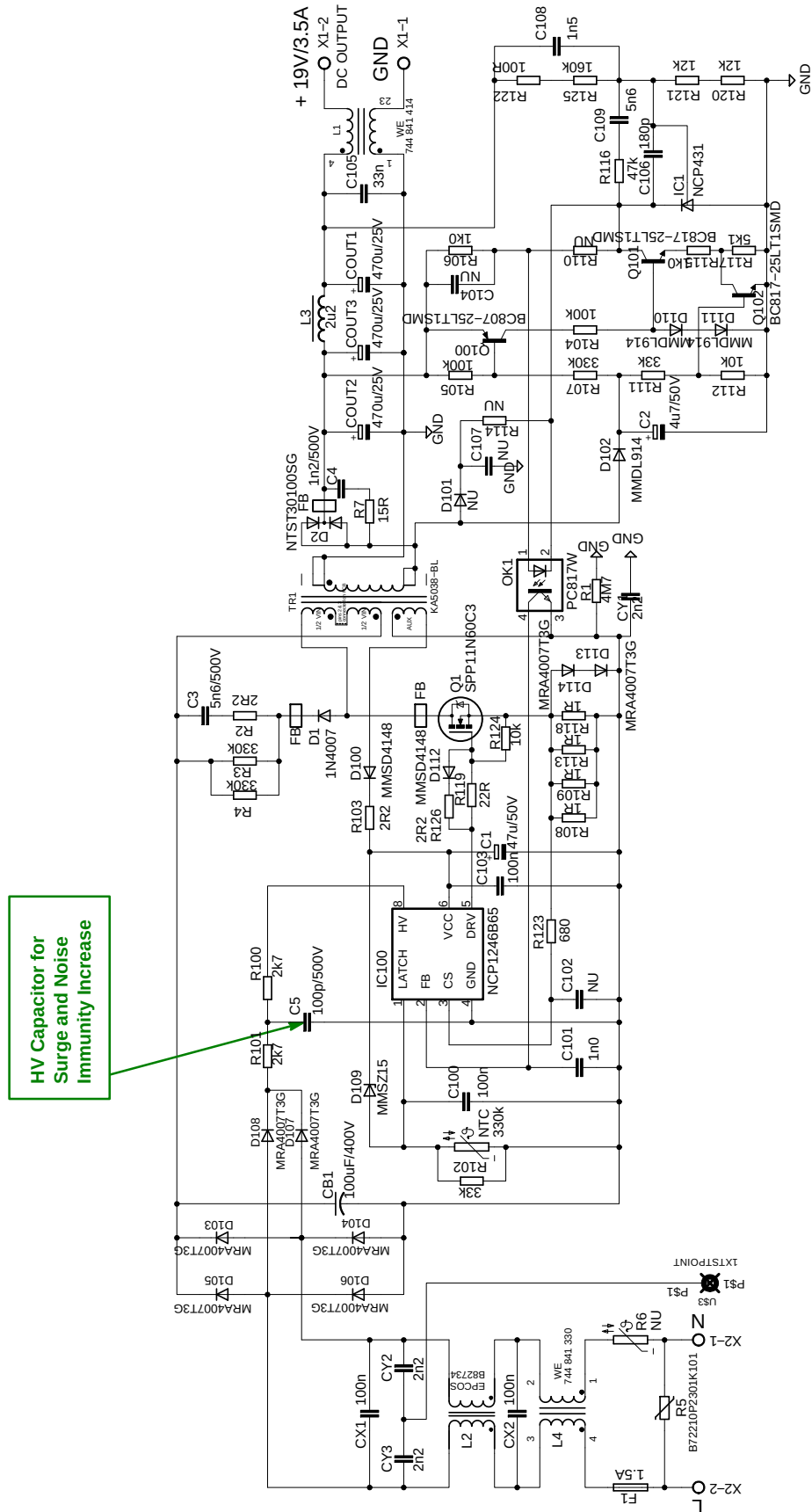


Figure 13. Recommended Schematic of the Notebook Adapter Using NCP1246 with Optimized Surge and Noise Immunity

Performance of the Designed 65 W Notebook Adapter

The following figures demonstrate the operation of the converter under different operating conditions and highlight various features such as a transition from CCM to DCM,

frequency foldback, pulse skipping, transient load response, stability in CCM, frequency jitter, overload protection, X2 capacitor discharge feature, etc. under both 115 V and 230 V input conditions as appropriate.

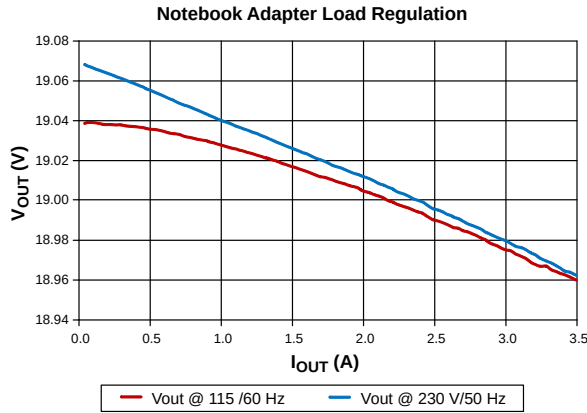


Figure 14. Load Regulation for Low and High Input Line

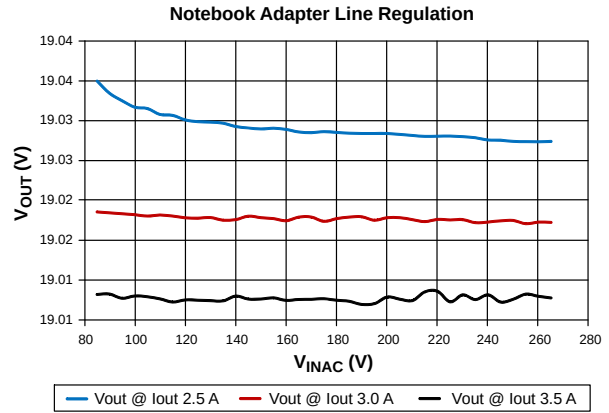


Figure 15. Line Regulation for High Output Loads

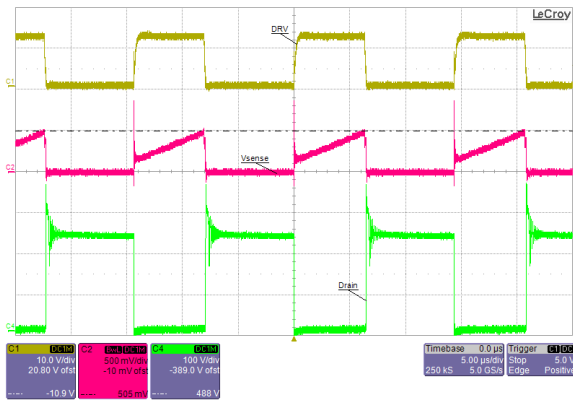


Figure 16. CCM Operation at Full Load (3.5 A) and 115 V/60 Hz Input

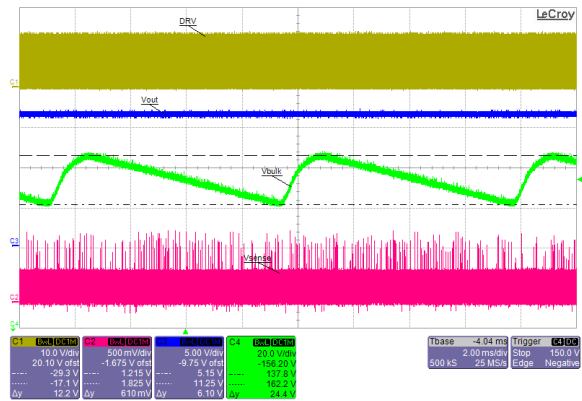


Figure 17. Ripple at Bulk Capacitor at Full Load (3.5 A) and 115 V/60 Hz Input Supply

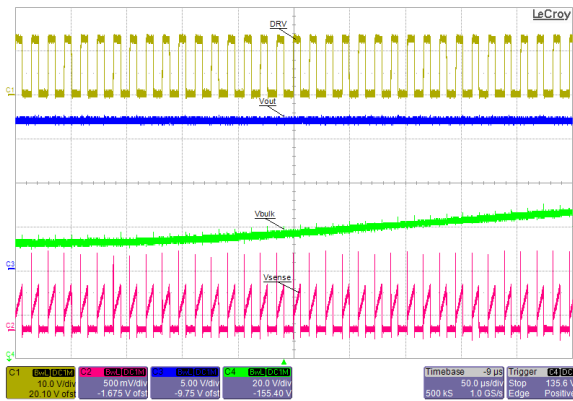


Figure 18. No Subharmonic Oscillations Appear under Full Load (3.5 A) and CCM Operation, with $D > 50\%$, 110 V/45 Hz Input

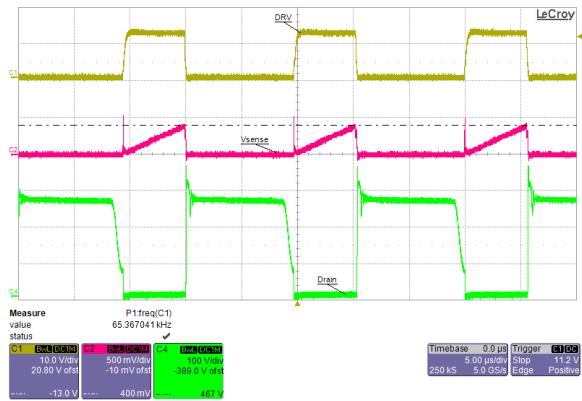


Figure 19. The DCM Mode Starts at 2.27 A of Load Current at 115 V/60 Hz Input

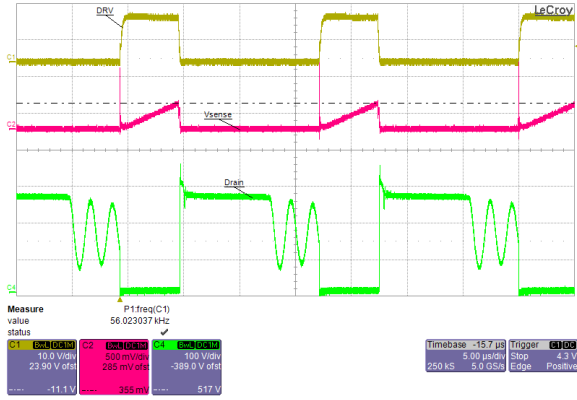


Figure 20. The Frequency Foldback Mode Starts at 1.60 A of Load Current at 115 V/60 Hz Input

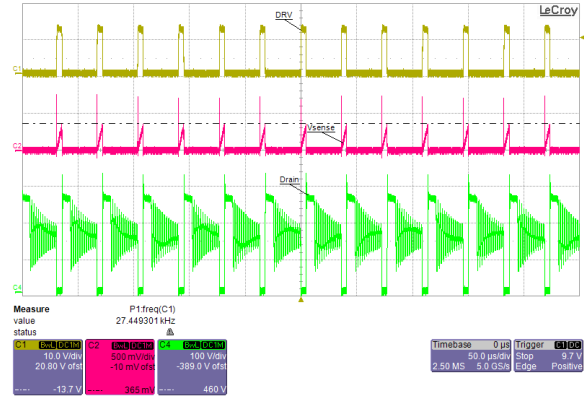


Figure 21. The Lowest Frequency at 0.65 A of Load Current at 115 V/60 Hz Input – Frequency Foldback is Finished

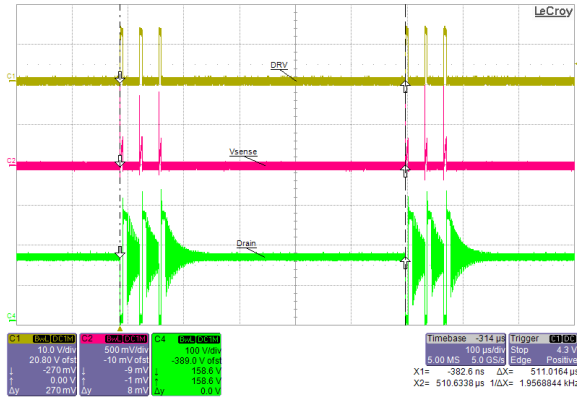


Figure 22. The Skip Mode at 137 mA of Load Current at 115 V/60 Hz Input

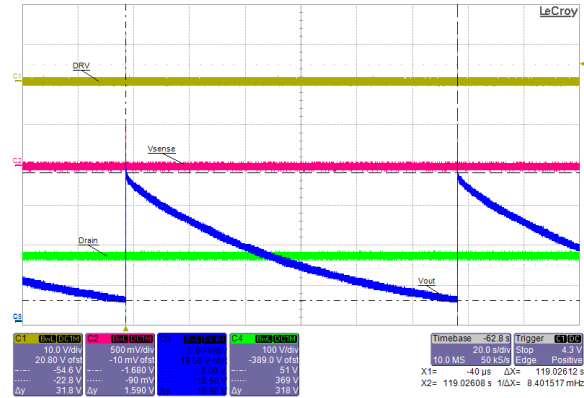


Figure 23. The Hiccup Mode and Output Voltage Waveform without any Load at Output and 115 V/60 Hz Input

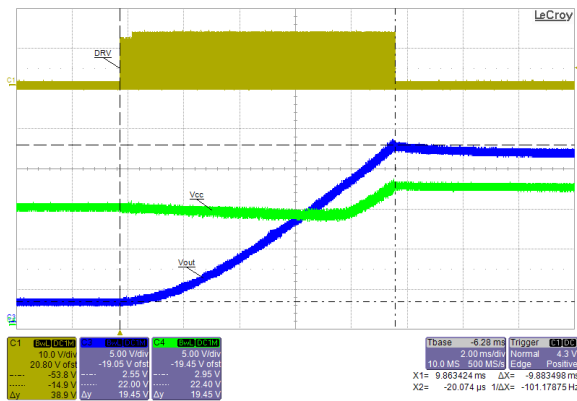


Figure 24. The Recharge Burst of DRV Pulses in the Hiccup Mode without any Load at Output and 115 V/60 Hz Input

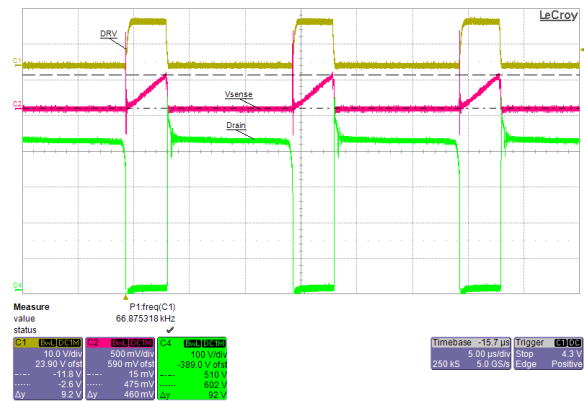


Figure 25. CCM/DCM Borderline Operation at Full Load (3.5 A) and 230 V/50 Hz Input

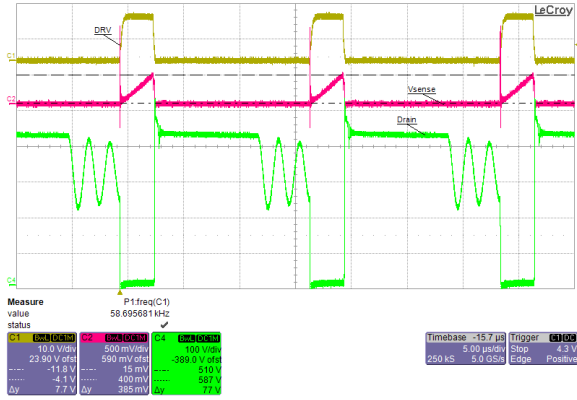


Figure 26. The Frequency Foldback Mode Starts at 2.62 A of Load Current at 230 V/50 Hz Input

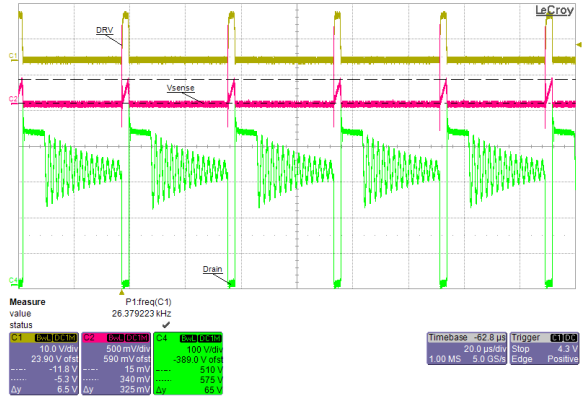


Figure 27. The Lowest Frequency at 0.70 A of Load Current at 230 V/50 Hz Input – Frequency Foldback is Finished

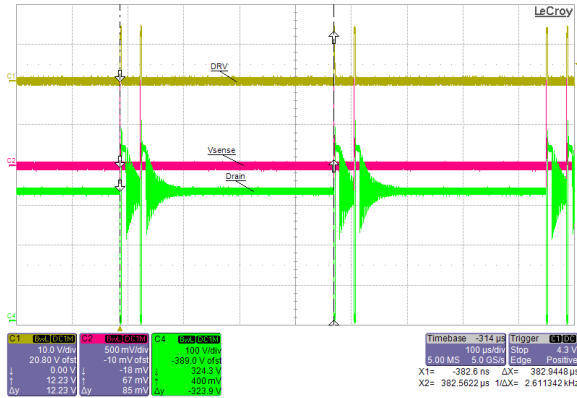


Figure 28. The Skip Mode at 137 mA of Load Current at 230 V/50 Hz Input

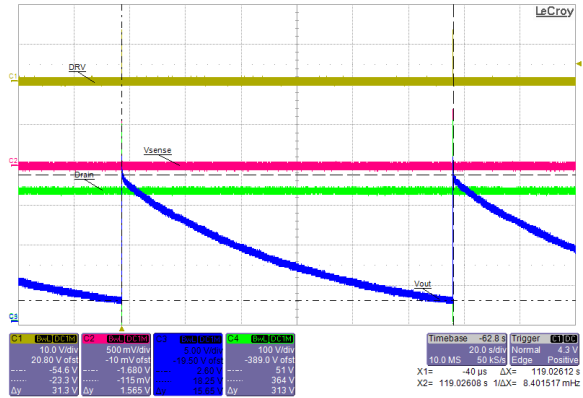


Figure 29. The Hiccup Mode and Output Voltage Waveform without any Load at Output and 230 V/50 Hz Input

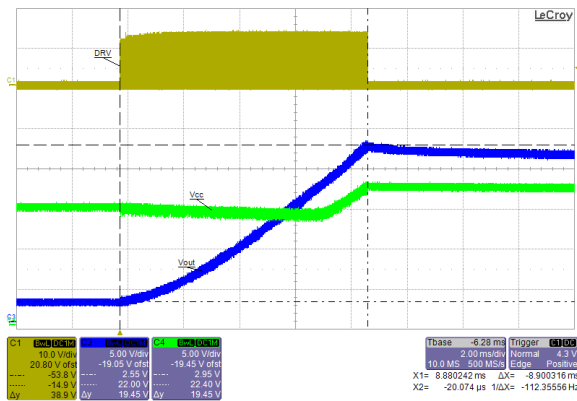


Figure 30. The Recharge Burst of DRV Pulses in the Hiccup Mode without any Load at Output and 230 V/50 Hz Input

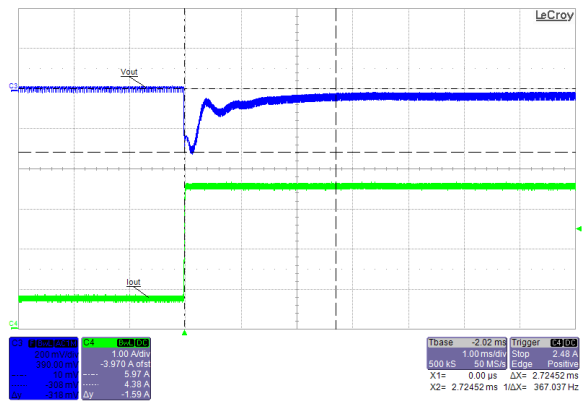


Figure 31. The Load Transient Step from 20% of Load to 100% of Load at 115 V/60 Hz Input

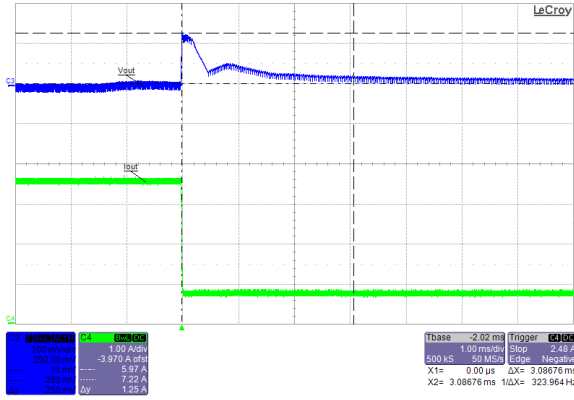


Figure 32. The Load Transient Step from 100% of Load to 20% of Load at 115 V/60 Hz Input

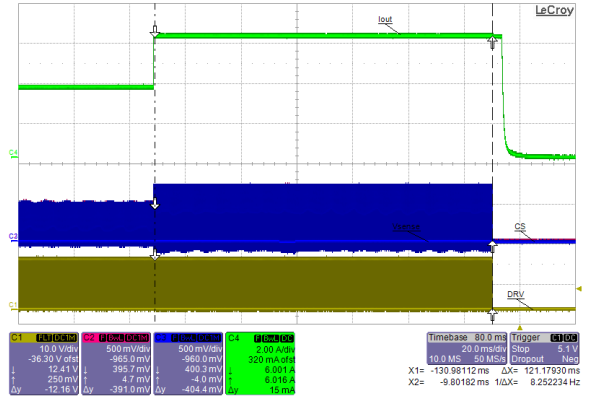


Figure 33. The Overcurrent Protection Timer Duration is 121 ms when the Adapter was Overloaded from 3.5 A to 6 A at 115 V/60 Hz Input. No OPP is Observable at these Conditions

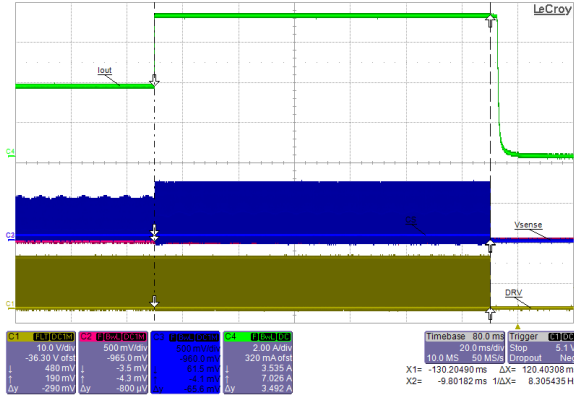


Figure 34. The Overcurrent Protection Timer Duration is 121 ms when the Adapter was Overloaded from 3.5 A to 7 A at 230 V/50 Hz Input. The OPP Current is Observable as a Shift of Minimum Levels between the Signal V_{sense} from R_{sense} and the Signal at the CS Pin

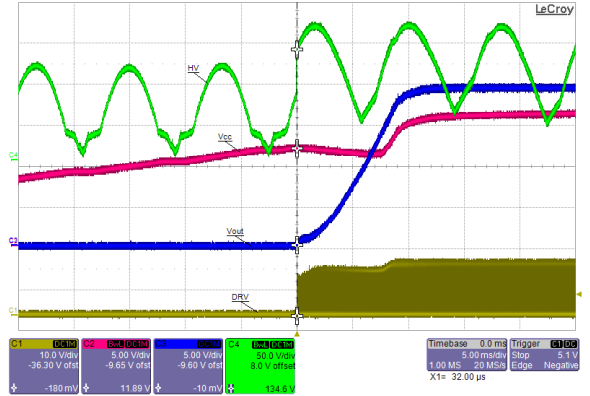


Figure 35. Adapter Start Up at 115 V/60 Hz Input and 1 A Output Current Load

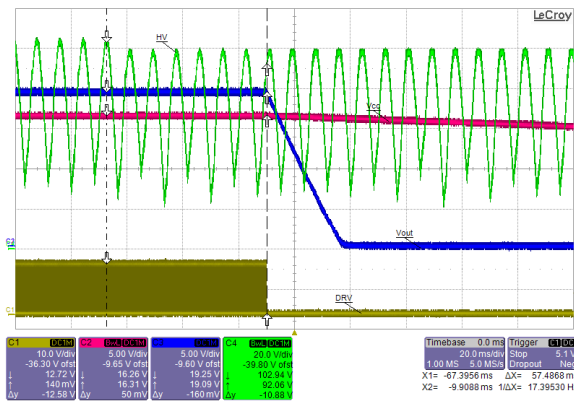


Figure 36. Brown-out Protection Reaction when the rms ac Input Voltage Drops Down from 80 V to 70 V under 1 A Output Current Loading

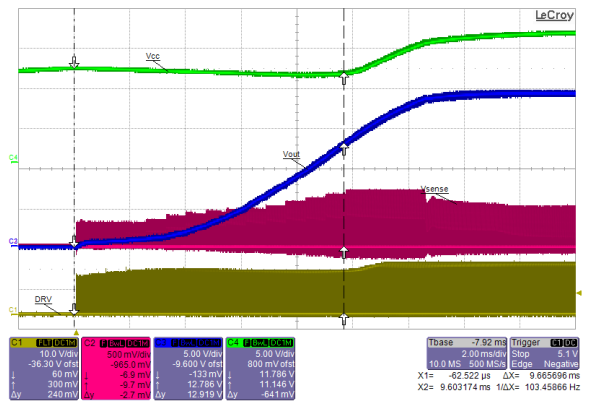


Figure 37. The Soft Start at 115 V/60 Hz Input with 3.5 A Output Current Loading

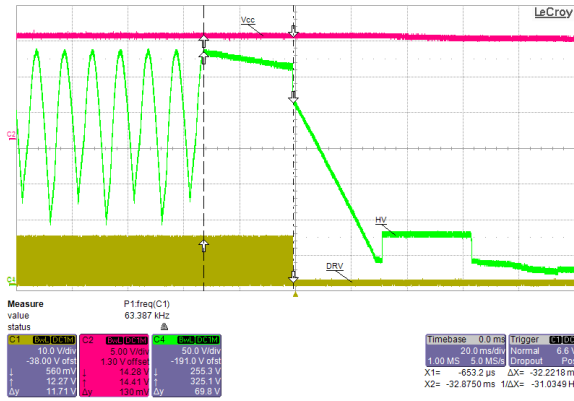


Figure 38. The X2 Capacitors Bank was Discharged after Application Unplug from 230 V/50 Hz Mains

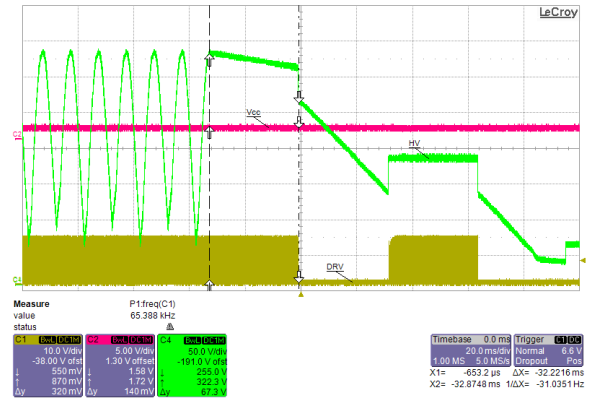


Figure 39. The 2 µF X2 Capacitors Bank was Discharged after Application Unplug from 230 V/50 Hz Mains (Extra Added X2 Capacitors to Demonstrate System Feature)

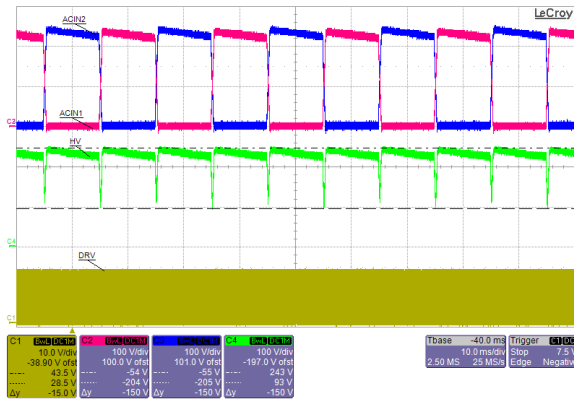


Figure 40. The X2 Discharge Feature Works Properly (is not False Activated) while the Application is Supplied by Cheap UPS, Using Square Wave

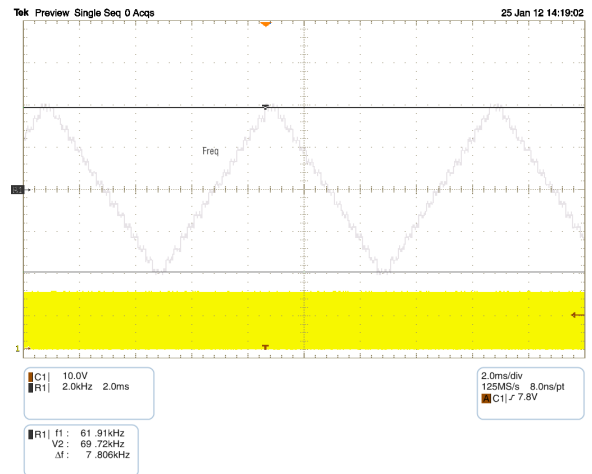


Figure 41. Frequency Deviation of the Frequency Jittering

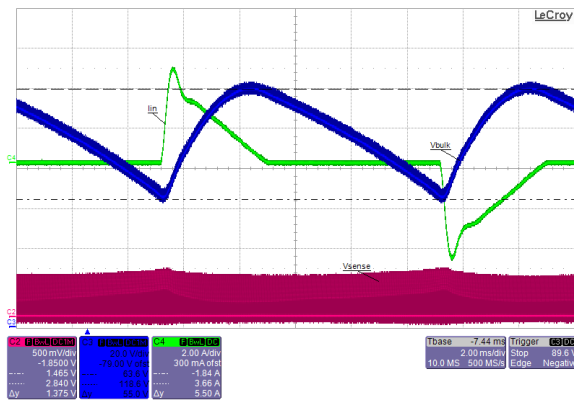


Figure 42. Ripple Observable at Bulk Capacitor at 85 V/50 Hz Input and 3.5 A Continuous Output Loading Current

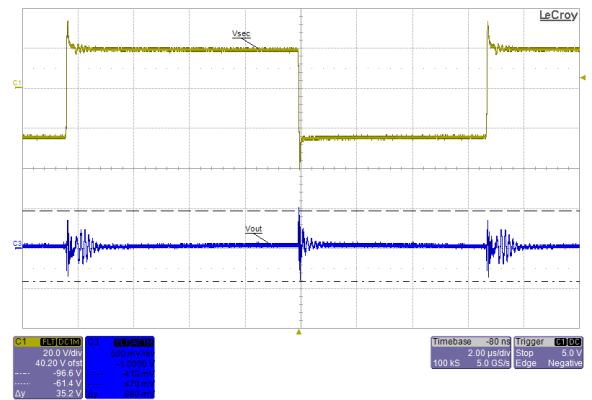


Figure 43. Detail of the Output Voltage Ripple and Voltage across Secondary Winding of Transformer at 115 V/60 Hz Input with 3.5 A Output Current Loading (the Ringing is Caused by the Secondary Diode Reverse Recovery)

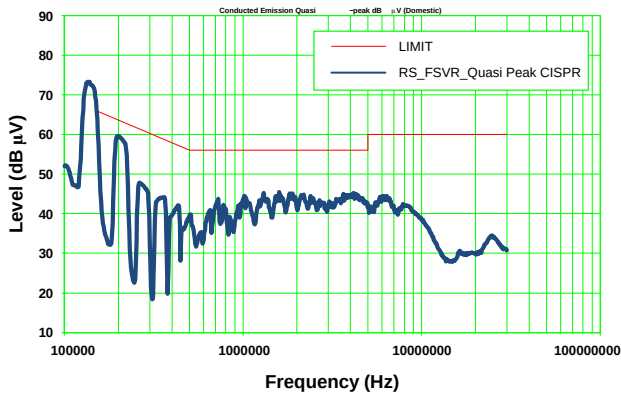


Figure 44. Harmonic Components of the Input Current at 230 V/50 Hz Input and 3.5 A Continuous Output Loading Current

Results Summary

The goal of this design is to show the extremely no-load input power solution which is cost effective and whose measured value is always below 20 mW. The frequency foldback and frozen current setpoint features offer the advantage of designing power supplies whose efficiency at light-loads are above 80%. Measured efficiency at 0.5 W of output power is always higher than 75%. Meeting these specs will enable our customers to meet the latest ENERGY STAR® requirements.

The designed wide input range adapter fulfils the requirement of having no-load input power lower than 30 mW over the wide input voltage range. While the complete design of the adapter must focus on achieving the low no-load input power, the controller facilitates this result by a frequency foldback and off-mode features. The family of controllers NCP1244/46 allows building cost effective, easy-to-design and extremely low no-load input power consumption power supplies.

The obtained average efficiency is 89.6% for the low line conditions (115 V/60 Hz) and 90.6% at high line conditions (230 V/50 Hz). This excellent result provides enough margins to fulfill the EPS 2.0 specification of 87% for the average efficiency. The high efficiency is obtained thanks to the low forward drop diode NTS30100SG from ON Semiconductor, transformer KA5038-BL from COILCRAFT with dedicated design for this application and the low loss EMI filters.

Thanks

Thanks to the COILCRAFT Company for providing the samples, custom design of the flyback transformer used in this board and their support.

Another thank belongs to the EPCOS Company for providing the samples of their components used in this design.

Caution

This demo board is intended for demonstration and evaluation purposes only.

References

- [1] [NCP1244A/B Datasheet](#)
- [2] [NCP1246A/B Datasheet](#)
- [3] Christophe P. Basso: *Switch-Mode Power Supplies, SPICE Simulations and Practical Designs*, McGraw-Hill, new York, 2008
- [4] Dr. Ray Ridley: *A New Continuous-Time Model for Current-Mode Control*, (<http://www.ridleyengineering.com/books.html>)
- [5] Application Note [AND8461/D](#)
- [6] Application Note [AN1679/D](#)
- [7] Application Note [AND8393/D](#)
- [8] Application Note [AND8154/D](#)

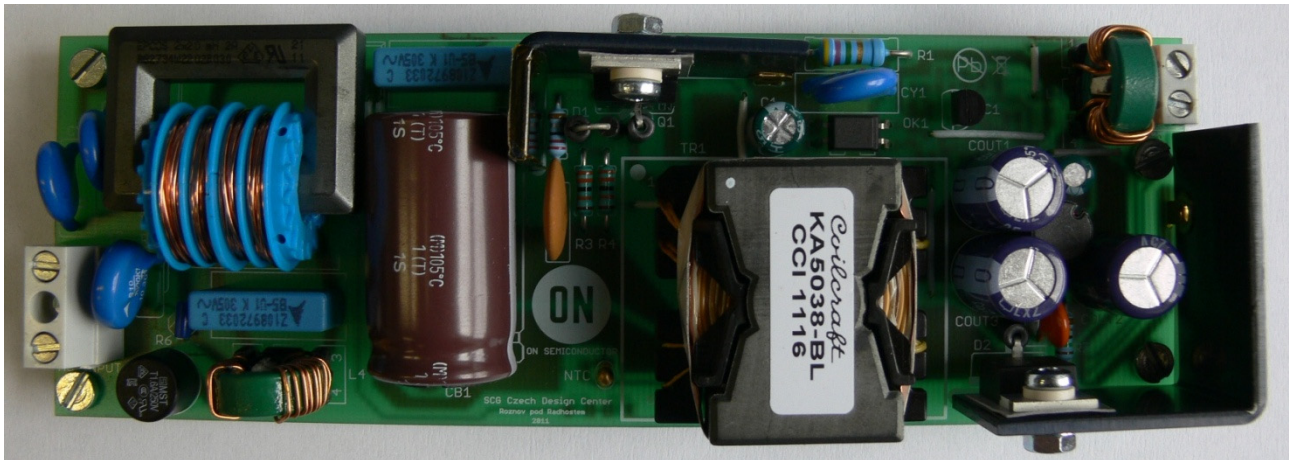


Figure 45. Photograph of the Designed Prototype (Real Dimensions are 150 × 51 mm)

AND9170/D

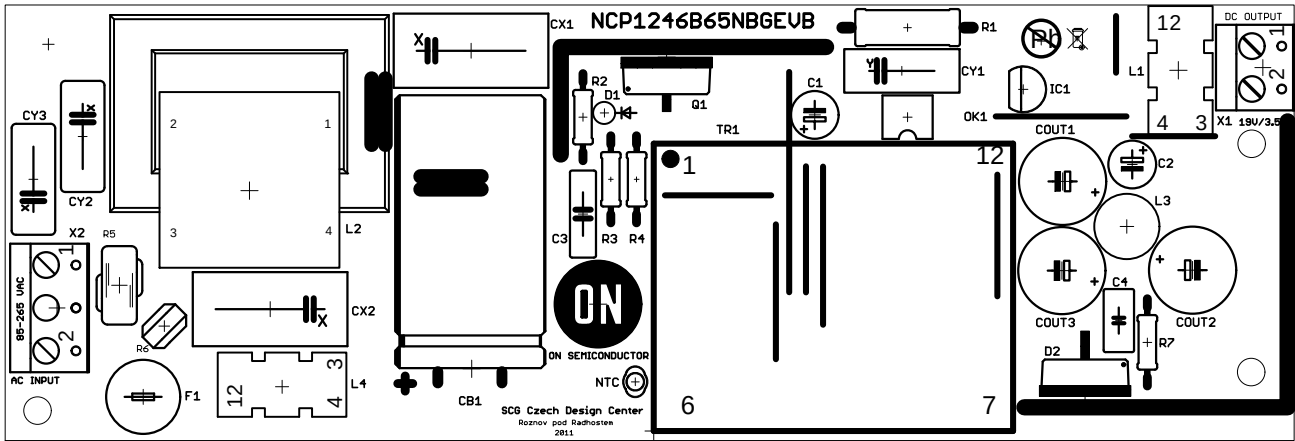


Figure 46. Component Placement on the Top Side (Top View)

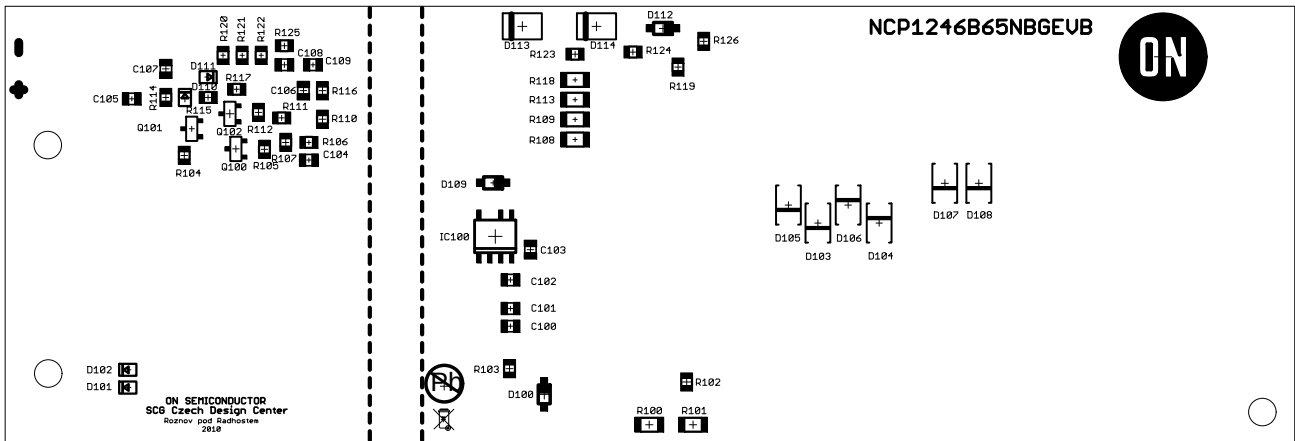


Figure 47. Component Placement on the Bottom Side (Bottom View)

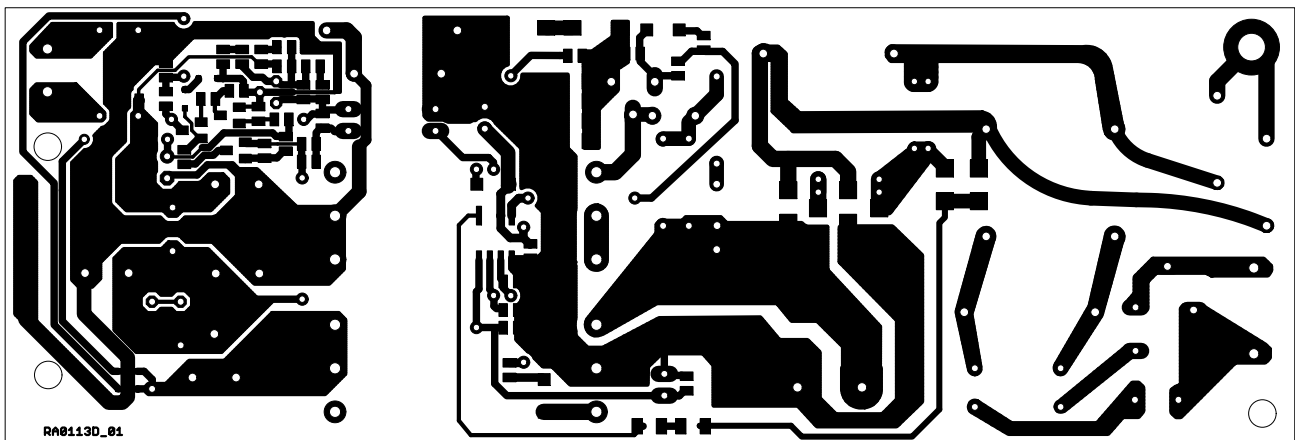


Figure 48. Bottom Side PCB Pattern (Bottom View)

Table 5. BILL OF MATERIALS

Designator	Qty.	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer's Part Number	Substitution Allowed
C1	1	Electrolytic Capacitor	47 μ F/50 V	20%	Radial	Koshin	KLH-050V470ME110	Yes
C2	1	Electrolytic Capacitor	4.7 μ F/50 V	20%	Radial	Koshin	KLH-50V4U7	Yes
C3	1	Ceramic Capacitor	5.6 nF/630 V	5%	Radial	TDK Corporation	FK20C0G2J562J	Yes
C4	1	Ceramic Capacitor	1.2 nF/630 V	5%	Radial	TDK Corporation	FK26C0G2J122J	Yes
C100, C103	2	Ceramic Capacitor	100 nF	10%	0805	Kemet	C0805C104K5RAC	Yes
C101	1	Ceramic Capacitor	1.0 nF	10%	0805	Kemet	C0805C102K5RAC	Yes
C102, C107	2	Ceramic Capacitor	NU	–	0805	–	–	–
C105	1	Ceramic Capacitor	33 nF	10%	0805	Kemet	C0805C333K5RAC	Yes
C106	1	Ceramic Capacitor	180 pF	10%	0805	Kemet	C0805C181K5RAC	Yes
C109	1	Ceramic Capacitor	5.6 nF	10%	0805	Kemet	C0805C560K5GAC	Yes
CB1	1	Bulk Capacitor	100 μ F/400 V	20%	Through Hole	United Chemi-Con	EKXG401ELL101MMN3S	Yes
COUT1, COUT2, COUT3	3	Electrolytic Capacitor	470 μ F/25 V	20%	Radial	Panasonic – ECG	ECA-1EHG471	Yes
CX1, CX2	2	Suppression Film Capacitors	100 nF	10%	Through Hole	Epcos	B32922C3104K	No
CY1, CY2, CY3	3	Ceramic Capacitor	2.2 nF/X1/Y1	20%	Disc – Radial	Murata	DE1E3KX222MA5B	Yes
D1	1	Standard Recovery Rectifier	1N4007	–	DO41-10B	ON Semiconductor	1N4007G	No
D2	1	Diode Schottky 100 V 30 A	NTST30100SG	–	TO220	ON Semiconductor	NTST30100SG	No
D100, D112	2	Diode	MMSD4148	–	SOD123	ON Semiconductor	MMSD4148T3G	No
D101	1	Diode	NU	–	SOD323-2	–	–	–
D102, D110, D111	4	Diode	MMDL914T1G	–	SOD323-2	ON Semiconductor	MMDL914T1G	No
D103, D104, D105, D106, D107, D108, D113, D114	8	Standard Recovery Rectifier	MRA4007T3G	–	SMA	ON Semiconductor	MRA4007T3G	No
D109	1	Zener Diode	MMSZ15	5%	SOD123	ON Semiconductor	MMSZ15T3G	No
F1	1	Fuse (MST ser.)	1.6 A	–	Through Hole	Schurter Inc	0034.6617	Yes
IC1	1	Programmable Precision Reference	NCP431	–	TO-92	ON Semiconductor	NCP431AVLPRAG	No
IC100	1	SMPS Controller	NCP1246B65	–	SOIC-08	ON Semiconductor	NCP1246B65	No
L1	1	Inductor	744 841 414	–	744 841 414	Würth Elektronik	744 841 414	No
L2	1	Inductor	B82734L	–	B82734L	Epcos	B82734W2202B030	No
L3	1	Inductor	2.2 μ H	10%	RFB0807	CoilCraft	RFB0807-2R2L	No
L4	1	Inductor	744 841 330	–	744 841 330	Würth Elektronik	744 841 330	No
–	2	EMI Suppression Ferrite Bead	74270073	–	74270073	Würth Elektronik	74270073	Yes

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Table 5. BILL OF MATERIALS (continued)

Designator	Qty.	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer's Part Number	Substitution Allowed
NTC	1	Sensing NTC Thermistor	330 kΩ	5%	Disc – Radial	Vishay	NTCLE100E3334JB0	Yes
OK1	1	Opto-coupler	PC817	–	4-DIP	Sharp	PC817X2J000F	Yes
Q1	1	N MOSFET Transistor	SPP11N60C3	–	TO220	Infineon	SPP11N60C3	Yes
Q100	1	PNP Bipolar Transistor	BC807-25LT1G	–	SOT-23	ON Semiconductor	BC807-25LT1G	Yes
Q101, Q102	2	NPN Bipolar Transistor	BC817-25LT1G	–	SOT-23	ON Semiconductor	BC817-25LT1G	Yes
R1	1	Resistor Through Hole, High Voltage	4.7 MΩ	5%	Axial Lead	Welwyn	VRW37-4M7JI	Yes
R2	1	Resistor	2.2 Ω	1%	0207	Vishay	MBB02070C2208FRP00	Yes
R3, R4	2	Resistor	330 kΩ	1%	0207	Vishay	HVR2500003303FR500	Yes
R5	1	Surge Protecting Varistor	B72210P2301K101	20%	Disc – Radial	Epcos	B72210P2301K101	No
R6	1	NTC Thermistor	Wire Strap	–	Disc – Radial	–	–	Yes
R7	1	Resistor	15 Ω	1%	0207	Vishay	MRS25000C1509FRP00	Yes
R100, R101	2	Resistor SMD	2.7 kΩ	1%	1206	Rohm	MCR18EZH2F2701	Yes
R102, R111	2	Resistor SMD	33 kΩ	1%	0805	Rohm	MCR10EZPF3302	Yes
R103, R126	2	Resistor SMD	2.2 Ω	1%	0805	Rohm	MCR10EZHFL2R20	Yes
R104, R105	2	Resistor SMD	100 kΩ	1%	0805	Rohm	MCR10EZPF1003	Yes
R106, R115	2	Resistor SMD	1.0 kΩ	1%	0805	Rohm	MCR10EZPF1001	Yes
R107	1	Resistor SMD	330 kΩ	1%	0805	Rohm	MCR10EZPF3303	Yes
R108, R109, R113, R118	4	Resistor SMD	1.0 Ω	1%	1206	Rohm	MCR18EZHFL1R00	Yes
R110, R114	2	Resistor SMD	NU	–	0805	–	–	–
R112, R124	2	Resistor SMD	10 kΩ	1%	0805	Rohm	MCR10EZPF1002	Yes
R116	1	Resistor SMD	5.6 kΩ	1%	0805	Rohm	MCR10EZPF5601	Yes
R117	1	Resistor SMD	5.1 kΩ	1%	0805	Rohm	MCR10EZPF5101	Yes
R119	1	Resistor SMD	22 Ω	1%	0805	Rohm	MCR10EZPF22R0	Yes
R120, R121	2	Resistor SMD	12 kΩ	1%	0805	Rohm	MCR10EZPF1202	Yes
R122	1	Resistor SMD	100 Ω	1%	0805	Rohm	MCR10EZPF1000	Yes
R123	1	Resistor SMD	680 Ω	1%	0805	Rohm	MCR10EZPF6800	Yes
R125	1	Resistor SMD	160 kΩ	1%	0805	Rohm	MCR10EZPF1603	Yes
TR1	1	Transformer	KA5038-AL	–	KA5038-AL	CoilCraft	KA5037-AL	No
X1	1	Terminal Block, 2 Way	CTB5000/2	–	W237-102	Cadem El.	CTB5000/2	Yes
X2	1	Terminal Block, 3 Way	CTB5000/3	–	W237-113	Cadem El.	CTB5000/3	Yes

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