AND8469/D

The NCP1250, a Versatile Tiny Controller for Offline Converters

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APPLICATION NOTE

Despite its small size, the NCP1250 packs a lot of goodies not even found in higher−end controllers. In its simplest form of application (5 active pins) the device lends itself very well to the design of compact and inexpensive offline power supplies where protections are reduced to the minimum. Owing to a 6th multi−function pin, the controller can also play in an upper level range and drive ac−dc adapters for notebooks or netbooks. In this case, exclusive features such as a non−dissipative Over Power Protection make the part a candidate of choice when it is necessary to combine high performance and cost sensitivity.

General Description

The part is encapsulated in a TSOP−6 package, very close in dimensions to the SOT−23 6−lead type. Featuring a low−power BiCMOS process, the die accepts to work with V_{CC} levels up to 28 V, safely clamping the drive voltage below 12 V. With its 15 μA start−up current, a high−value resistive network can be used in offline applications to crank the converter, naturally minimizing the wasted power in high−line conditions. In nominal load operations, the switching frequency of this peak−current mode control circuit is either 65 kHz or 100 kHz. In light load operations, the part linearly reduces its switching frequency down to 26 kHz and enters skip cycle as the load goes further down in power. This mode of operation favors a high efficiency from high to moderate output levels and ensures the lowest acoustic noise in the transformer when the light−load mode is entered. To improve the EMI signature, a low−frequency modulation brings some dither to the switching pattern. Unlike other circuits, the dither is kept in foldback mode and still smoothes the noise signature. The feedback is simply made by pulling down the dedicated pin via an optocoupler, driven from the secondary side by a TL431 or a cheap Zener diode. Figure 1 shows the NCP1250 in its simplest implementation within a 12 V converter. Only 5 pins over the six are used.

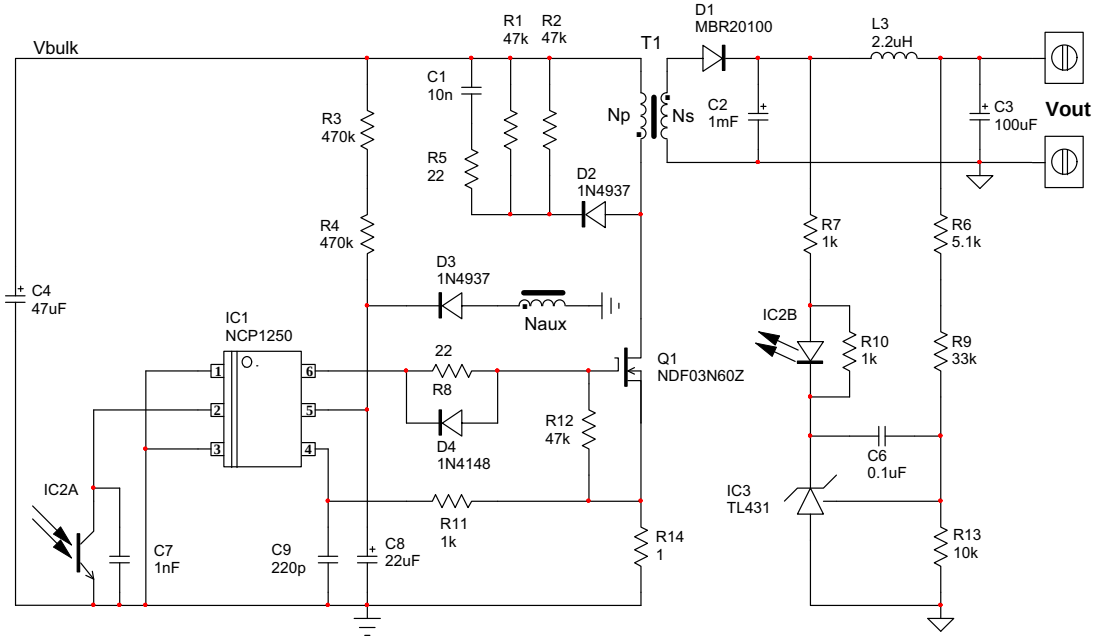

Figure 1. The Simplest Implementation of the NCP1250 in an Isolated Flyback Converter

Pin 5 − The V_{CC} Supply

The chip supply is brought in via pin 5. Upon start−up, for a voltage less than 18 V (typical), the internal consumption is limited to 15 μA maximum. It suddenly changes to around 2 mA as the controller starts to switch at 65 kHz on a 1 nF capacitive load when V_{CC} reaches 18 V. The auxiliary voltage can go down to around 9 V before the controller safely stops the switching pulses.

The classical configuration to start−up the controller appears in Figure 2. We can see a start−up resistor, R_1, connected to the bulk voltage. It generates a current I_1. Part of this current, 15 μA, is diverted inside the chip. This current is fairly constant up to V_{CC} equals 18 V. The current flowing inside the V_{CC} capacitor is thus:

$$I_2 = I_1 - I_{CC1} \quad \text{(eq. 1)}$$

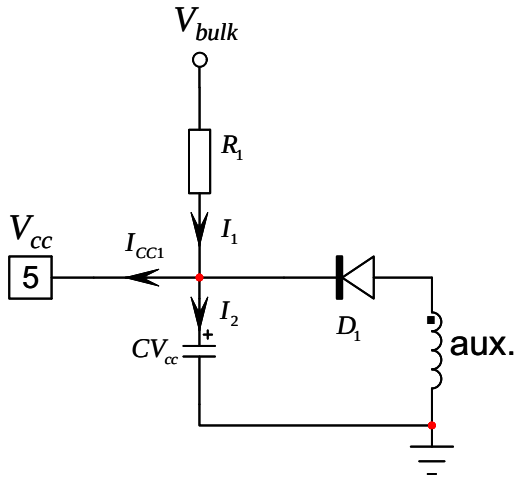

Figure 2. A Simple Resistive String Brings the Necessary Current to Charge CV_{CC}

When the controller starts to switch (i.e. V_{CC} is 18 V), the current consumption suddenly increases. The consumption depends on the MOSFET gate charge Q_G. As I_1 is kept small to minimize the wasted power in R_1 at high line, all the current is now delivered by the V_{CC} capacitor. This element remains alone to power the controller and the voltage across its terminals falls out. Before the voltage on Pin 5 reaches the VCC_{min} level, the auxiliary winding must be high enough to take over the controller supply via D_1. If the capacitor is too small, the voltage drops too quickly and the converter cannot start−up properly: the pulses are stopped and the current consumption switches back to 15 μA for a new re−start. An auto−recovery hiccup mode takes place as shown in Figure 3.

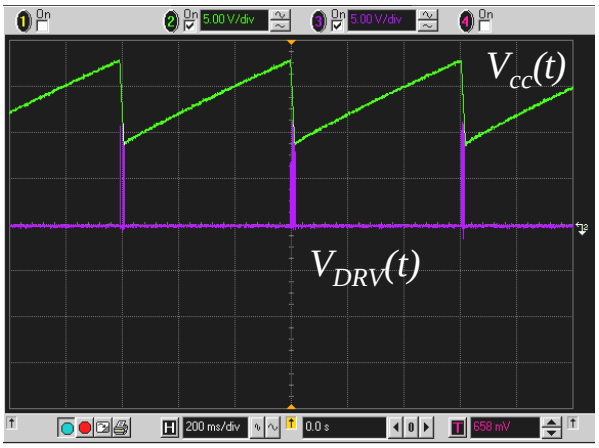

Figure 3. The Part Enters An Auto−recovery Hiccup Mode in Case the Auxiliary V_{CC} is Missing

Before calculating R_1, we have to know what capacitor value can maintain enough voltage on the V_{CC} pin until the auxiliary winding takes over. The most difficult task in this calculation is to estimate the worst−case time at which the auxiliary voltage takes over. This worst case happens when the output power P_{out} is maximal and the input voltage V_{in} is minimal. Based on our experience, a time−duration of 25 ms is a reasonable value to start with. Then, experiments on the prototype will either confirm the assumptions or will tell you to consider a different value. For the capacitor calculation, we have to check the minimum available voltage excursion across the capacitor from the specifications. Reading the NCP1250 datasheet, we find that this occurs when both the start−up voltage and the $UVLO_{low}$ thresholds are at minimum:

$$\Delta V_{CC} = VCC_{(on),min} - VCC_{(min),min} 16 - 8.3 = 7.7\ V \quad \text{(eq. 2)}$$

If we consider a 25 ms time duration for the auxiliary voltage takeover and a total consumption current around 3 mA (let's assume a 3 A power MOSFET, the V_{CC} capacitor must show a capacitance above the following value:

$$C_{VCC} \geq \frac{ICC_3 t_2}{\Delta V_{CC}} \geq \frac{3m \times 25m}{7.7} \geq 9.7\ \mu F \quad \text{(eq. 3)}$$

Given the manufacturing dispersions on this type of component, it is necessary to take tolerance precautions. Typically, for a 10 μF capacitor, we should select a 22 μF type as we can expect wide variations over time and manufacturing lots. Unfortunately, in some cases, as the startup current has to be minimized for obvious power

dissipation constraints, we can not increase the V_{CC} capacitor too much otherwise the start−up will suffer. Now, the 25 ms might be too conservative and a 10 μF capacitor might finally be the right choice. It is also possible to slightly increase the peak power capability of the converter and make it reach regulation sooner. Once the converter is assembled, a test is necessary to check this out. Worst case occurs at maximum loading conditions on a warmed−up transformer. The test result carried upon the adapter with a 10 μF capacitor appears in Figure 4 and confirms that enough margins exist with this value.

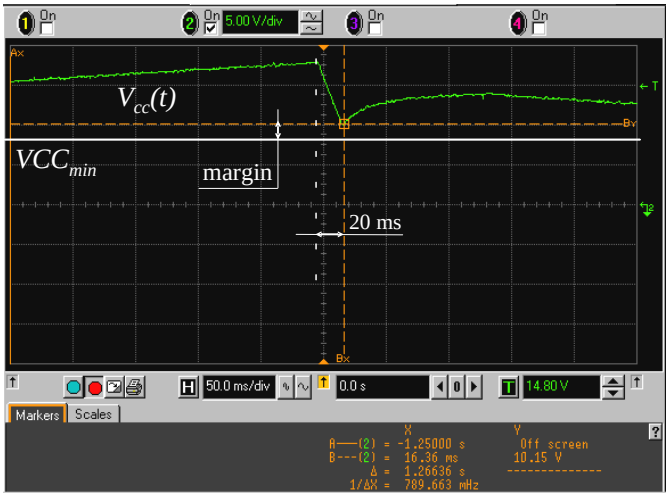

Figure 4. A Start−up Sequence at Maximum Output Power Shows Enough Margins on the V_{CC} Capacitor Voltage

The capacitor value being known, how much current do we need for I_1? If we adopt a 10 μF capacitor and need a start−up time less than 2.9 s at the lowest input voltage (85 Vrms or 120 V rectified), what current needs to be injected into C_{VCC} to raise from 0 to $V_{CC(on),max}$?

$$I_1 \geq \frac{V_{CC(on),max} C_{VCC}}{t_{startup}} \geq \frac{20 \times 10\mu}{2.9} \geq 69\ \mu A \quad \text{(eq. 4)}$$

These 69 μA, to which 15 μA must be added (I_{CC1}), have to be delivered from the lowest input line. This is 120 Vdc in a classical design intended to operate on a universal mains input. What resistor value must then be used to reach that number?

$$R_{startup} = \frac{V_{bulk,min} - V_{CC(on),max}}{I_1} = \frac{120 - 20}{84\mu} \approx 1.2\ M\Omega \quad \text{(eq. 5)}$$

Unfortunately, in high−line conditions (265 Vrms), this resistor is permanently biased and dissipates power. If we neglect the V_{CC} value, the dissipated power amounts to:

$$P_{Rstartup,hiline} = \frac{V_{bulk,max}^2}{R_{startup}} = \frac{375^2}{1.2M} = 117\ mW \quad \text{(eq. 6)}$$

This extra power dissipation is not a big problem if you plan to boast a no−load standby power less than 300 mW. On the contrary, if you wish to comply with a standard asking less than 100 mW at high line, Equation 6 tells you that it is impossible.

Looking for a Half Cycle

Rather than connecting the start−up network to the dc rail, V_{bulk}, why not connecting it directly to the mains? As one bridge diode will remain in series with the return path, we will benefit from a half−wave rectification, leading to a lower average value than on the bulk rail, hence lower power dissipation on the start−up resistor. This is what Figure 5 suggests.

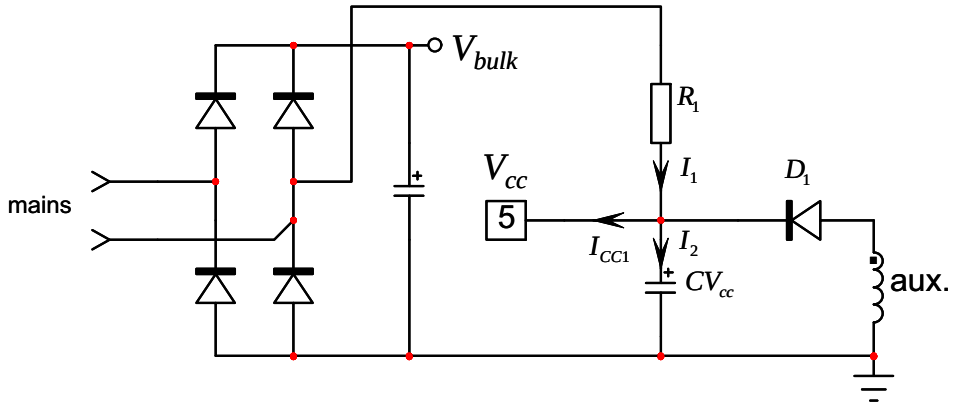

Figure 5. The Direct Connection to the Mains Significantly Reduces the Wasted Power on the Start−up Resistor

Now, it is interesting to calculate the value of resistor R_1 to keep the same start−up time as in the case we have the direct connection to the bulk capacitor. The calculation of R_1 leading to the same start−up time is approximate as a) the voltage on the capacitor grows cycle by cycle b) capacitive leaks are involved. However, considering perfect elements, the following formula gives a starting point:

$$R_1 = \frac{t_{start}}{C_{Vcc} \times \ln\left(\frac{V_{pLL}}{V_{pLL} - \pi \times V_{CC(on),max}}\right)} \quad \text{(eq. 7)}$$

From the above formula, we can extract R_1 value where $V_{in,peak}$ represents the lowest rectified input voltage (85 Vrms, 120 Vdc):

Using values given in (eq. 4), the start−up resistor in a half−wave configuration is evaluated to:

$$R_1 = \frac{2.9}{10\mu \times \ln\left(\frac{120}{120 - \pi \times 20}\right)} = 391\ k\Omega \quad \text{(eq. 8)}$$

It then possible to show as detailed in Ref. [1] that the average power dissipated by the above network is given by the following formula. In this case, the peak voltage becomes the highest value (375 Vdc, 265 Vrms):

$$P_{R1} = \frac{V_{in,peak}^{\ 2}}{4R_1} = \frac{375^2}{4 \times 391k} = 90\ mW \quad \text{(eq. 9)}$$

It corresponds to a significant decrease compared to the power dissipated by connecting the start−up network directly to the rectified bulk voltage.

There is one thing you must think about when designing the start−up network. If keeping the current at the lowest value is a must for a low standby power, it obviously slows down the start−up time. In some applications, where standby power is a less stringent parameter, it is desirable to crank the power supply in the shortest possible time. One way of doing it is to increase the start−up current. However, the auto−recovery circuitry works by discharging the V_{CC} capacitor via an internal consumption of around 1 mA. Therefore, if you force a current I_1 greater than 1 mA, then the controller will no longer be able to discharge the V_{CC} capacitor and auto−recovery will be lost.

Another parameter worth considering is how the parasitic capacitor offered by the active rectifying diode is affected by the addition of some extra capacitance. In our calculations, we considered a nice continuous half-wave signal feeding the start-up resistor R_1. The reality differs, especially if you connect the ground clip of the oscilloscope probe to the primary ground − i.e. the bulk capacitor minus pin − to observe the V_{CC} voltage. The input voltage shape can be changed, distorting the charging current and thus, modifying the start-up time. To measure this latter, it is certainly better to only look at the ac input current using a dedicated current probe while the output of the converter is charged with a resistive load (an electronic load could, again, affect the parasitic return via the Y-cap. and influence the measurement). Monitor the time at which the converter is plugged (this is $t = 0$ and you have a sharp in-rush spike) and look at the current shape until it is significantly affected. This is the time at which the converter operates and V_{CC} has reached the turn-on level. As the power supply only requires a few tens of milliseconds to reach its regulation level, considering the time from $t = 0$ to the change in current shape as the start-up time will not create a significant measurement error. On our adapter board, we have captured a typical start-up current signature obtained at an input voltage of 85 Vac. Figure 6 shows a start-up time of 2.4 s.

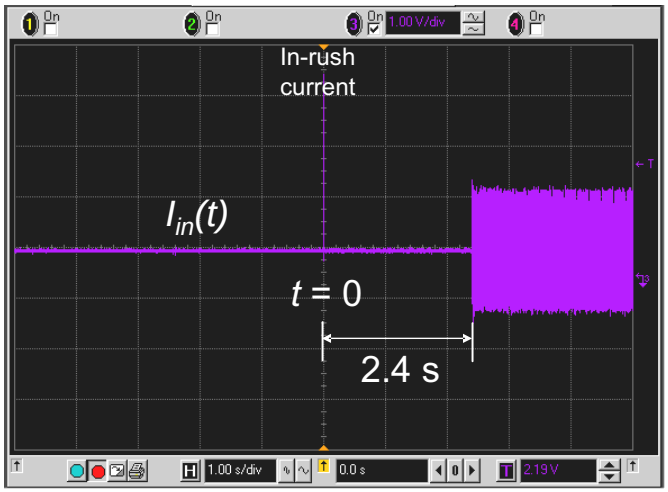

Figure 6. On This Plot, the Start−up Time is Measured at the Moment the Converter is Plugged to the Moment at Which the Current Significantly Changes. The Load is a Passive Resistor and No Oscilloscope Ground is Connected to the Board

Triggering the SCR

The latched-state of the NCP1250/1251 is maintained via an internal thyristor (SCR). When the voltage on pin 3 exceeds the latch voltage for four consecutive clock cycles, the SCR is fired and immediately stops the output pulses. Then V_{cc} is discharged to a fix level of 7 V typically: the circuit is latched and the converter no longer delivers power. To maintain the latched-state, a permanent current must be injected in the part. If too low, the part de-latches and the converter resumes operation. This current is characterized to 30 μA as a minimum but we recommend to include a design margin and select around 60 μA. The test is to latch the part and reduce the input voltage until it de-latches. If you de-latch at V_{in} = 70 V rms for a minimum voltage of 85 V rms, you are fine. If it precociously recovers, you will have to increase the start-up current, unfortunately to the detriment of standby power.

The most sensitive configuration is actually that of the half-wave connection proposed in Figure 5. As the current disappears 5 ms for a 10 ms period, the latch can potentially open at low line. If you really reduce the start-up current for a low standby power design, you must ensure enough current in the SCR in case of a faulty event. An alternate connection to the above is shown in Figure 7.

In this case, the current is no longer made of 5-ms “holes” and the part can be maintained at a low input voltage. Experiments show that these 2 MΩ resistor help to maintain the latch down to less than 50 V rms, giving an excellent design margin. Please note that these resistors also ensure the discharge of the X2 capacitor up to a 0.47 μF type.

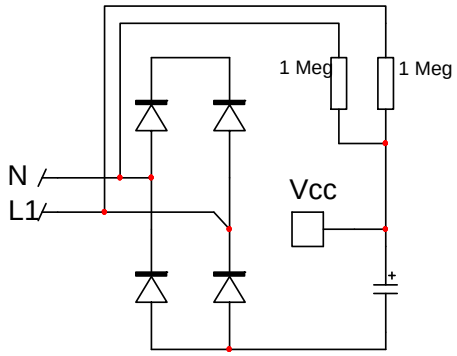

Figure 7. The full-wave connection ensures latch current continuity as well as a X2-discharge path.

Pin 6 – The Driver Output

The part features a CMOS−based output driving stage capable of sourcing 300 mA peak while sinking 600 mA. As the part accepts V_{CC} voltages up to 28 V, it is important to clamp the voltage actually applied to the gate−source terminals of the selected power MOSFET. The $R_{DS(on)}$ of a high−voltage MOSFET is usually defined at a 10 V V_{GS} bias. Going below this value will make the resistance increase, together with the conduction losses. On the contrary, biasing the MOSFET well beyond this 10 V reference, will only reduce the $R_{DS(on)}$ by a very small amount, unnecessarily increasing the power dissipation in the driver. Also, at a certain bias level, the MOSFET lifetime can also be affected. The internal 12 V clamp offers a safe operating choice.

Dissipation wise, it is now important to check that the selected MOSFET complies with the power dissipation capability of the package. If we look at the graph displayed in Figure 8, the thermal resistance junction−to−ambient for the smaller copper area (35 μm copper thickness) is 290°C/W for a 50 mm^2 pad. Additional measurements have shown that this number could be extrapolated to 360°C/W for half of this value, 25 mm^2. If we operate the part in an environment where the ambient temperature T_A is 70°C and we want to limit the maximum junction temperature to less than 110°C, then the maximum allowable power the package can dissipate is:

$$P_{max} = \frac{T_{J,max} - T_A}{R_{\theta JA}} = \frac{110 - 70}{360} = 111\ mW \qquad \text{(eq. 10)}$$

What are the sources justifying power dissipation in a PWM controller? The first is the inherent consumption of the blocks (clock, comparators, references etc.). On the data−sheet, this is the parameter I_{CC2} which also includes the various cross−conduction currents from the unloaded driver output. We have 1.8 mA. The other source is the average current necessary to drive the selected power MOSFET. This average current is nothing else than the total gate−charge Q_G multiplied by the switching frequency F_{SW}:

$$I_{DRV,avg} = Q_G F_{SW} \qquad \text{(eq. 11)}$$

If we supply the IC from a V_{CC} rail, then the power dissipation becomes:

$$P_D = \left(I_{CC2} + I_{DRV,avg}\right)V_{CC} \qquad \text{(eq. 12)}$$

Let's assume the V_{CC} is set to 14 V. From Equations 10 and 12, the maximum authorized current to drive the MOSFET becomes:

$$I_{DRV,avg} = \frac{P_D}{V_{CC}} - I_{CC2} = \frac{111m}{14} - 1.8m = 6.1\ mA \qquad \text{(eq. 13)}$$

Due to Equation 11, we can compute the maximum allowed Q_G for a junction temperature kept below 110°C in a 70°C atmosphere:

$$Q_{G,max} = \frac{I_{DRV,max}}{F_{SW}} = \frac{6.1m}{65k} = 94\ nC \qquad \text{(eq. 14)}$$

This number is fairly large and quite comfortable actually. Does it mean that the controller is capable to safely drive large gate−charge MOSFETs? Certainly not. The moderate driving capability of the NCP1250 would generate unacceptable switching losses and the total efficiency would suffer.

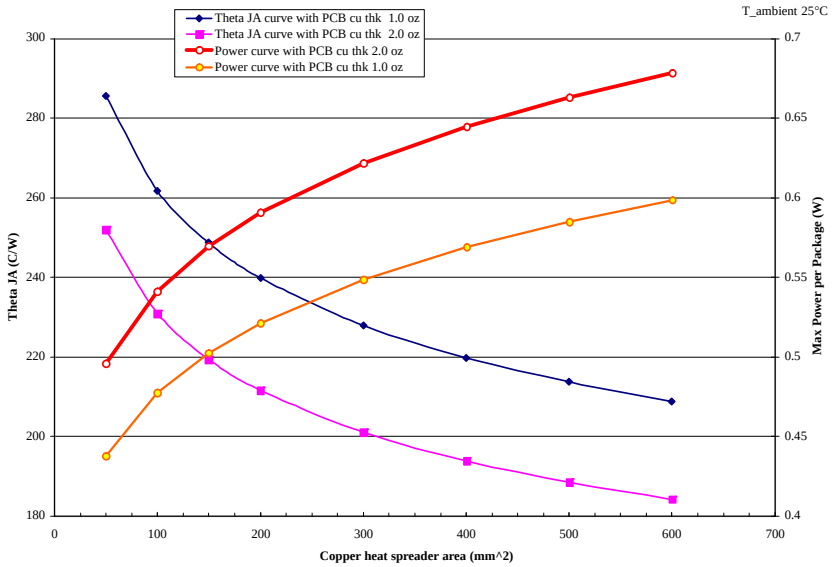

Figure 8. The Power Dissipation on the Package Depends on the Copper Area Around It

Given this power dissipation constraints, it is important to look at the selected MOSFET datasheet. For instance, a NDF04N60Z exhibits a total gate charge of 19 nC which is ok to be used with the NCP1250. Beyond these MOSFET sizes, for a 6 A or bigger, we recommend to add a small PNP transistor to help strengthening the turn−off discharge. This is what Figure 9 shows. In this picture, Q_2 is driven by R_{16}, adjusted to shape the turn−on time and soften the EMI signature of the converter. When pin 6 is down to ground, Q_1 is activated and blocks Q_2.

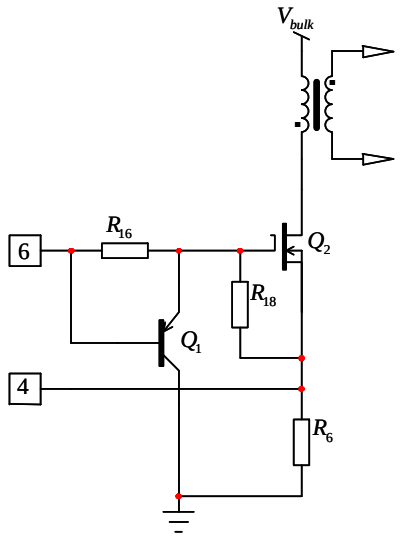

Figure 9. A Small PNP Transistor Vigorously Pulls the Gate Down at Turn Off

To avoid any production issues, e.g. leaving the gate open because the controller is not properly soldered, R_{18} keeps the gate connected to the source whatever the circuit state. Please note that the addition of the external transistor helps to divide the power dissipated on the package by a factor of 2.

Pin 4 – The Current Sense Input

The current sense pin routes the voltage developed across the sense resistor to a Leading Edge Blanking (LEB) circuit before reaching the PWM reset comparator. The LEB principle is to blind the current sense comparator for 300 ns and avoid false tripping because of spurious signals found on the sense voltage. The internal schematic appears in Figure 10 and discloses two switches.

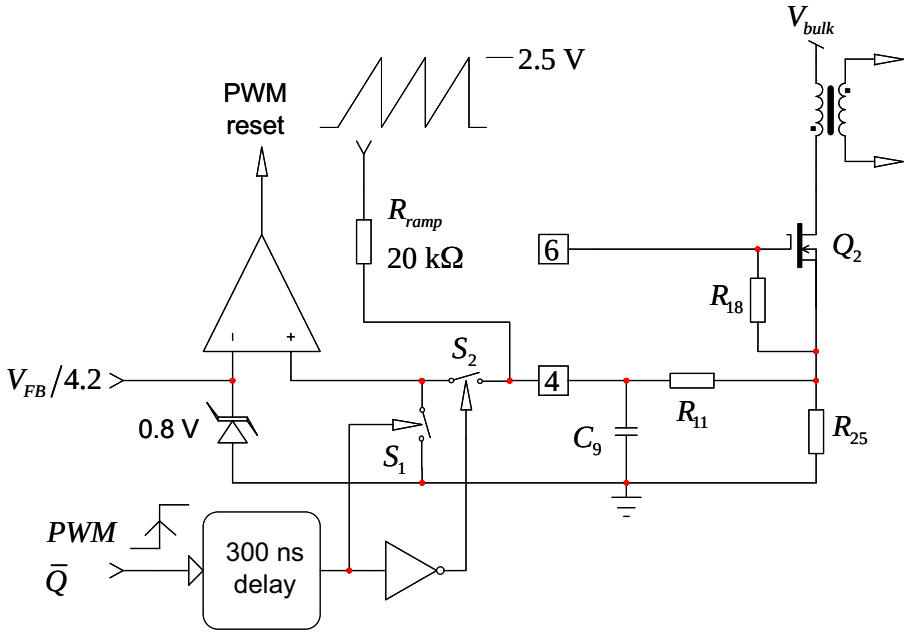

Figure 10. The Current Sense Pin Monitors the Voltage Coming from the Sense Resistor but Also Contributes to Inject Slope Compensation.

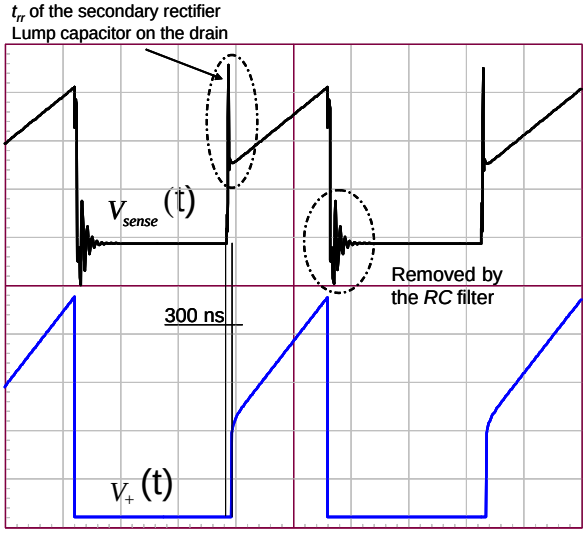

Figure 11. The LEB Circuitry Removes All Oscillations Found on the Current Sense Signal

When the driver output is high, the grounded switch S_1 is closed and the series switch S_2 is open. This network fully isolates the current−sense comparator from the CS pin. After 300 ns have elapsed, S_1 opens and S_2 closes, routing a clean signal to the (+) of the comparator (Figure 11).

The current−sense pin hosts another function which is the slope compensation. Slope compensation is necessary to tame the sub−harmonic oscillations that occur in a current−mode converter operating in a Continuous Conduction Mode (CCM) with a duty−ratio approaching or exceeding 50%. The cure to this problem is to subtract a ramp of the correct amplitude from the feedback signal or add the same ramp to the current sense pin. This latter is the technique adopted for the NCP1250 and described in Figure 10. A ramp signal is available from the clock circuitry. Once internally buffered, this signal drives the CS pin via a 20 kΩ resistor. Therefore, by adjusting the resistor placed in series with the current sense resistor signal – R_{10} in Figure 10 – it is possible to create a voltage divider and precisely adjust the level of slope compensation.

In the NCP1250 controller, the oscillator ramp features a 2.5 V swing. If the clock operates at a 65 kHz frequency, then the available oscillator slope corresponds to:

$$S_{ramp} = \frac{V_{ramp,peak} D_{max}}{T_{SW}} = \frac{2.5 \times 0.8}{15\mu} = \quad \text{(eq. 15)}$$

$$= 133\ \text{kV/s or } 133\ \text{mV/}\mu\text{s}$$

In a flyback design, let's assume that our primary inductance L_p is 600 μH, and the SMPS delivers 19 V with a N_p:N_s ratio of 1:0.25. The off−time primary current slope S_p is thus given by:

$$S_P = \frac{\left(V_{out} + V_f\right)\frac{N_S}{N_p}}{L_p} = \frac{(19 + 0.8) \times 4}{600\mu} = 132\ \text{kA/s} \quad \text{(eq. 16)}$$

If we have a sense resistor R_{sense} of 330 mΩ, the above primary current ramp turns into a voltage ramp of the following amplitude:

$$S_{sense} = S_p R_{sense} = 132\text{k} \times 0.33 \quad \text{(eq. 17)}$$

$$= 43.6\ \text{kV/s or } 43.6\ \text{mV/}\mu\text{s}$$

A common law to stabilize a current−mode converter is to select 50% of the inductor downslope as the required amount of ramp compensation. If we stick to this recommendation, then we shall inject a ramp whose slope is ≈22 mV/μs. As the internal compensation is of 133 mV/μs, the divider ratio (*divratio*) between R_{comp} and the internal 20 kΩ resistor has to be:

$$\text{divratio} = \frac{22\text{m}}{133\text{m}} = 0.165 \quad \text{(eq. 18)}$$

The formula must be updated with:

$$R_{comp} = R_{ramp}\text{divratio} = 20\text{k} \times 0.165 = 3.3\ \text{k}\Omega \quad \text{(eq. 19)}$$

A resistor of the above value will then be inserted from the sense resistor to the current sense pin as shown in Figure 10 (R_{10}). We recommend adding a small capacitor of 100 pF, from the current sense pin to the controller ground for an improved immunity to the noise. This is the capacitor C_{10} in Figure 10. Please make sure both components are located very close to the controller.

Maximum Peak Current Limit and Short−Circuit Protection

In case the feedback signal is lost, e.g. if the optocoupler is destroyed or the output undergoes a short−circuit, the peak current setpoint will be pushed to the maximum level. In this controller, without Over Power Protection (OPP) signal on pin 3, the maximum allowable level on the current sense pin is 0.8 V. As soon as the controller detects that the maximum peak current setpoint is reached, an internal countdown occurs. The minimum duration of this countdown is 100 ms. If within this period of time the feedback brings the peak current setpoint within operational limits (i.e. below 0.8 V), then the timer is reset. On the contrary, if during 100 ms (min) the controller senses an over current condition, then at the end of the count down, the circuitry stops all switching pulses. At this point, the V_{CC} capacitor remains alone to self−supply the controller and the voltage across its terminals falls down. Again, as the current consumed by the controller is around 1 mA, you have to make sure that the start−up current is not higher than this value otherwise the operation will be perturbed. When V_{CC} finally reaches the $VCC_{(min)}$ value, around 9 V, the circuit is reset and the consumption goes back to 15 μA (max): the V_{CC} level starts to rise towards VCC_{ON}, initiating a start−up sequence. If the fault is gone, the converter resumes operations; this is the auto recovery mode for the NCP1250B. The A extension latches off in presence of a fault. Otherwise, a hiccup mode takes place, as shown in Figure 12.

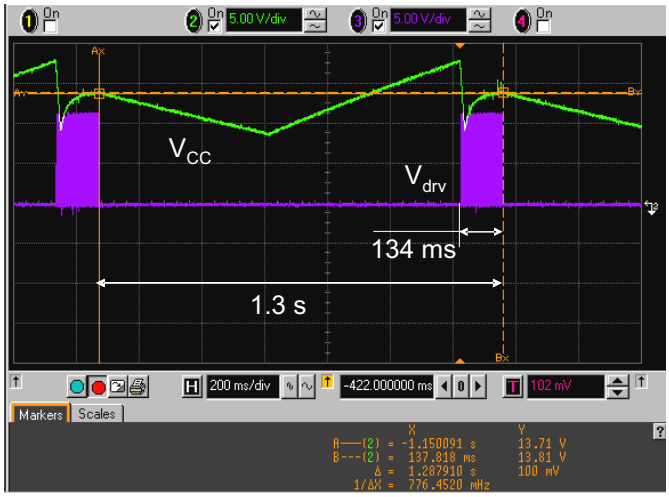

Figure 12. In Presence of a Short−Circuit or an Over Power Condition, a 100 ms Timer (typical) Shuts Down the Controller and Makes it Enter an Auto−recovery Protective Mode

Pin 1 – The Circuit Ground

Usually, there is not much to say about the circuit ground. However, even if we deal with moderate−power converters, we need to apply a few rules pertinent to the power electronics world. The most important one is to make sure all ground−referenced sensitive signals returns to a quiet 0 V point, the controller ground pin. For instance, the optocoupler collector is connected to the feedback pin of the NCP1250 (pin 2) whereas its emitter pin must connect to the ground. As the optocoupler is often placed remotely from the controller, it can be tempting to connect the emitter to the closest ground trace, perhaps the sense resistor return. Please do not otherwise spurious oscillations could take place and make the whole converter unstable. Rather, route a copper trace along the one that already routes the collector and connect it to the controller ground point. Make sure the compensating capacitor (C_7 in Figure 1) is not placed across the optocoupler, but right between the controller pins 2 and 1. The recommendations also apply for the current sense network (C_9 and R_{11} in Figure 1) that must be placed very close to the controller. A copper trace from R_{11} can then be placed to reach the sense resistor. Even if the trace is long, it is of less importance as the conveyed signal is low impedance. Figure 13 shows an example of Printed Circuit Board (PCB) routing when using the NCP1250.

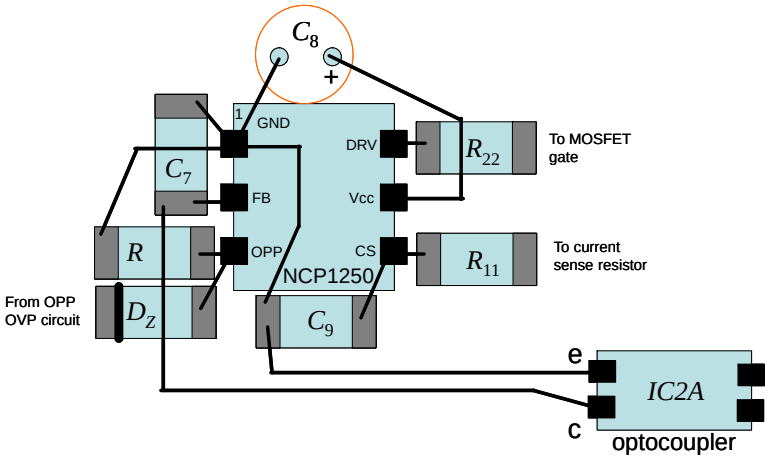

Figure 13. Decoupling Components Must Be Placed Very Close to the Controller

Pin 2 – The Feedback Pin

The feedback pin in a current−mode−controlled power supply is the control input that sets the inductor peak current on a cycle−by−cycle basis. The internal circuitry around pin 2 in the NCP1250 appears in Figure 14.

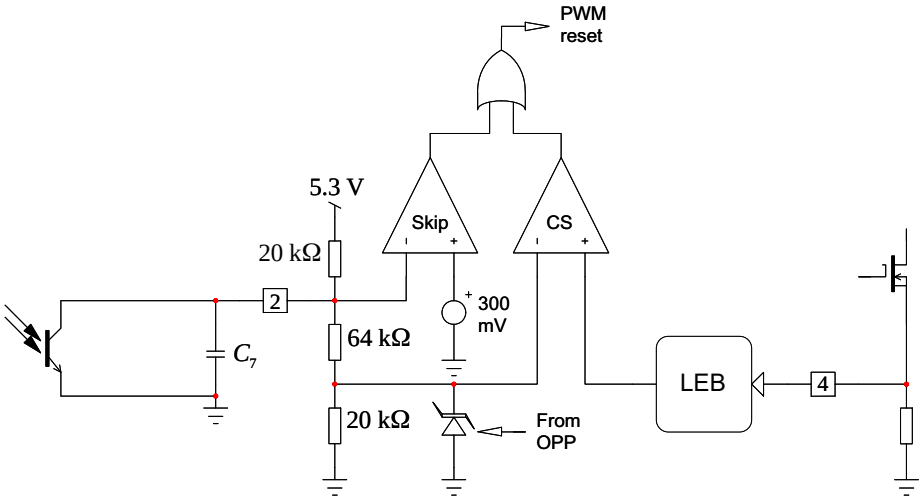

Figure 14. The Internal Simplified Schematic of the Feedback Circuitry

The regulation is obtained by pulling the feedback pin to ground via the optocoupler collector. The division ratio from the feedback pin to the current sense comparator is exactly 4.2. However, the maximum current voltage setpoint cannot exceed 0.8 V. For ac analysis, the equivalent pull−up resistor is made by the paralleling of the upper 20 kΩ resistor with the series combination of the 84 kΩ and the 20 kΩ resistors. It makes an equivalent value of 16 kΩ.

When the load is getting lighter, the operating frequency is decreased to limit the switching losses and thus improve the efficiency in this mode. An internal Voltage Controlled Oscillator (VCO) observes pin 2. When the voltage on this pin stays above 1.5 V, the frequency is fixed and corresponds to the nominal value, 65 or 100 kHz. As the load current still decreases, so does the feedback voltage. The VCO senses this change and the switching frequency also goes down. The lower limit is 26 kHz typically and will be reached for a feedback voltage of around 350 mV. Below this number, the part enters skip cycle. To obtain a better efficiency in skip mode, the peak current is frozen at a certain point. This point corresponds to 1.05 V on the feedback pin. As a divide−by−4.2 circuit is installed, it implies a maximum peak current setpoint of (1.05/4.2/0.8) x 100 = 31.2% of the nominal peak current. As an example, if you have a 1 Ω sense resistor, the maximum peak current in absence of OPP will be 0.8/1 = 800 mA. The skip operation will then occur at a ≈250 mA peak inductor current.

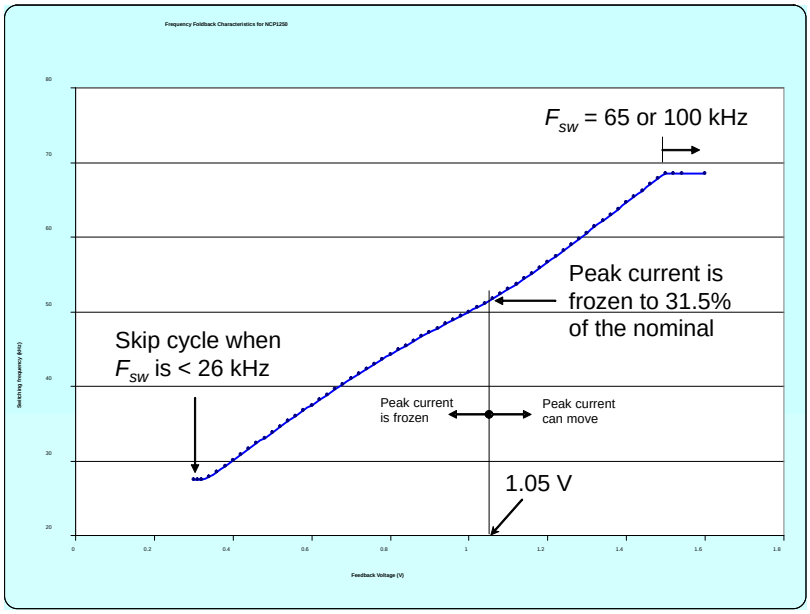

Figure 15. The Frequency is Reduced as the Feedback Pin Passes Below 1.5 V. When the Frequency Reaches 26 kHz and the Load Keeps Decreasing, the Part Enters Skip Cycle

This value combined with a 26 kHz frequency guaranties the lowest acoustic noise in the transformer or in the *RCD* clamp network.

Skip Cycle and Optocoupler

As indicated in the specifications, the skip−cycle level is placed at 300 mV. Popular optocouplers such as the PC817 or the PC123 from Sharp feature a $V_{CE,sat}$ of 200 mV as a maximum upper limit when loaded with a 1 mA collector current. They can be selected to work with the NCP1250. Experience in large−scale production shows that other devices with higher saturation levels can also be selected given the small feedback current of ≈250 μA (20 kΩ pull−up resistor with a 5 V open−loop voltage) and the available current dynamics via the LED series resistance (R_7 in Figure 8). If we take the specifications of the PS2913−1 from Renesas Electronics, it states a $V_{CE,sat}$ of 300 mV (max) when the LED is biased to 1 mA and a 200 μA current circulates in the collector. However, as indicated by Figure 16, an increase of the LED forward current from 500 μA to 2 mA makes the $V_{CE,sat}$ drop to 100 mV, giving enough margin for natural production spreads.

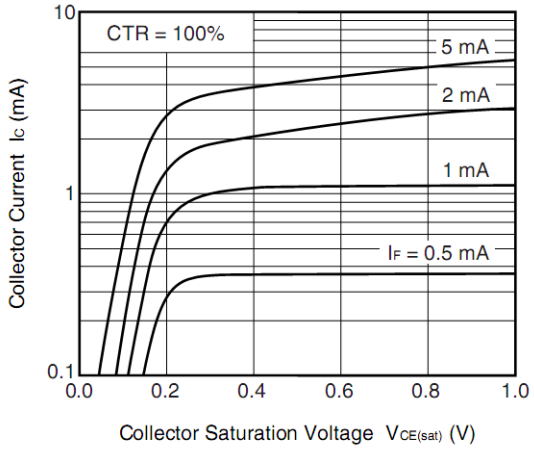

Figure 16. The Typical Saturation Voltage Curves of a PS2913−1 Optocoupler with Different LED Currents

In skip−cycle operation, the changes of the LED current are taken care of by the TL431 without impact on the no−load standby power. Experiments carried on the demonstration board using a SFH615A−2 gave a standby power at high line below 100 mW.

Shutting Down the Controller

Thanks to the presence of the skip−cycle comparator, it is easy to stop the controller. Just permanently pull the feedback pin below 300 mV and the switching pulses are stopped. Figure 17 shows that a simple transistor whose collector or drain is connected to the feedback pin is enough to stop the controller.

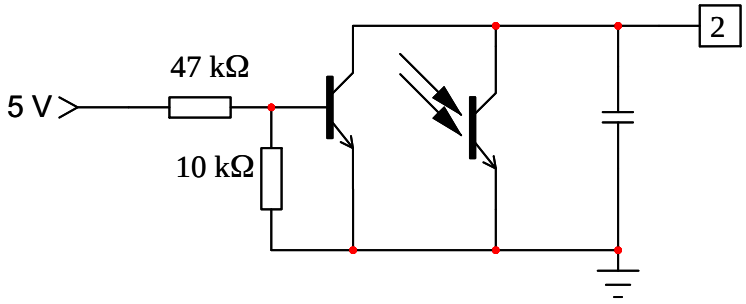

Figure 17. A Simple Transistor, Bipolar or a MOSFET, Can Be Used to Stop the Controller

Pin 3 – The Combined OVP−OPP Pin

When used, this pin offers a means to a) reduce the maximum power the converter can deliver at high line b) latch the circuit off in case of stringent problem such as an Over Voltage Protection (OVP) event or an Over Temperature Protection (OTP) events Let's first take a look at the first feature, the Over Power Protection (OPP) function.

Over Power Protection

The maximum power a flyback converter can deliver depends on several variables such as the switching frequency, the primary inductor and the maximum allowable primary peak current. Among these three variables, all of them are theoretically fixed and constant. Therefore, the power the converter can deliver at high input voltage should theoretically not differ from that delivered at the lowest input voltage. In reality, we know that both values differ and sometimes, in a large proportion. If we consider the primary inductor and the switching frequency independent from the input voltage, the final peak current seen by the inductor actually depends on the input voltage. Why? Because when the internal current−sense comparator detects an over−current condition, it takes time for this information to propagate inside the controller and eventually, bring the MOSFET gate down. The time needed is called the propagation delay. Most of the data−sheets, including the NCP1250, give you the propagation delay inherent to the controller, alone, when loaded by a 1 nF capacitor. In reality, depending on the drive current capability, the various resistors in series with the gate and the MOSFET gate−charge, it can be significantly longer. Figure 18 shows the resulting signals at low and high line levels. Depending on the propagation delay, the difference in current can be quite significant, impacting the maximum power at high line:

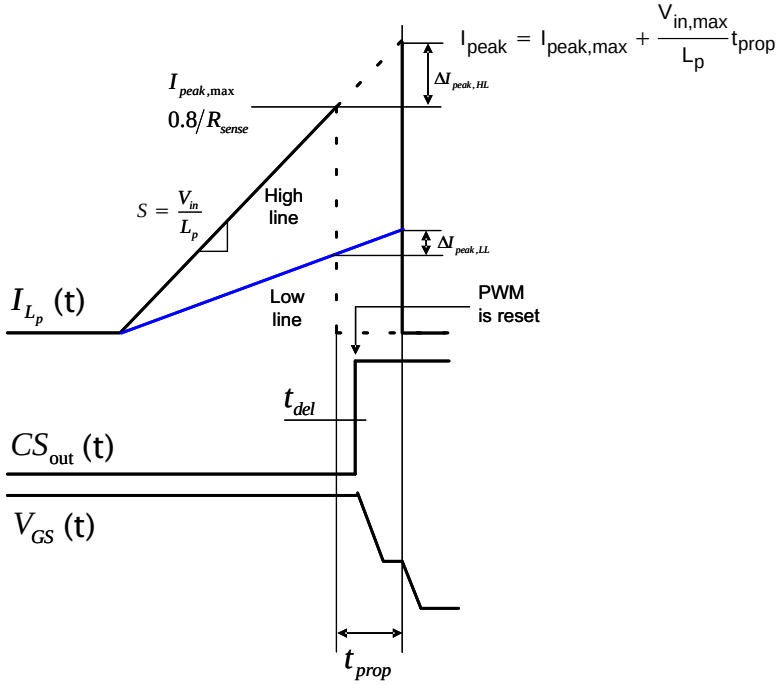

Figure 18. The Propagation Delay Affects the Final Peak Current Value at High Line

$$I_{peak,max} = \frac{V_{sense}}{R_{sense}} + \frac{V_{in}}{L_p} t_{prop} \quad \text{(eq. 20)}$$

The peak current runaway at high line is only partially responsible for the power increase in this operating condition. The second culprit is the transition from Continuous Conduction Mode (CCM) to Discontinuous Conduction Mode (DCM). This phenomenon happens because the on time naturally reduces at high line and offers more off−time to demagnetize the primary inductor (the inductor downslope is constant). This is what Figure 19 shows you. In this picture, we can see that the valley current tends to decrease as the input voltage goes up. The power transmitted by a flyback converter operating in CCM obeys the following formula:

$$P_{out} = \frac{1}{2} L_p \left(I_{peak}^{\ 2} - I_{valley}^{\ 2} \right) F_{SW} \eta \quad \text{(eq. 21)}$$

Where: L_p is the primary inductor, I_{peak} is the inductor peak current, I_{valley} is the inductor valley current, F_{sw} is the switching frequency and η is the converter efficiency. Since we deal with a peak current controller, in fault condition at high line, the maximum peak current will slightly increase compared to that obtained at low line. What actually matters in Equation 21 is the reduction of I_{valley} inherent to a longer off time. By manipulating a few equations, it is possible to calculate the valley current at high line and thus compute the power generated in this condition:

$$I_{valley,HL} = I_{peak,max,HL} - \frac{T_{SW} V_{in,HL} \left(V_f + V_{out} \right)}{L_p \left(V_f + V_{out} + N V_{in,HL} \right)} \quad \text{(eq. 22)}$$

Where:

T_{SW} is the switching period (15 μs or 65 kHz)
V_f is the secondary diode forward drop at the maximum output current (0.5 V)
V_{out} is the converter output voltage (19 V)
L_p is the primary inductor (600 μH)
N is the transformer turns ratio N_s/N_p (0.25)
t_{prop} is the total measured propagation delay (350 ns)
$V_{in,HL}$ = 370 V
$V_{in,LL}$ = 120 V
R_{sense} is the sense resistor (0.33 Ω)
$I_{peak,max,HL}$ is the maximum peak current obtained for V_{in} = $V_{in,HL}$ in Equation 20: 2.64 A
$I_{peak,max,LL}$ is the maximum peak current obtained for V_{in} = $V_{in,LL}$ in Equation 20: 2.49 A

With the above numbers, we obtain the following valley currents:

$$I_{valley,LL} = 1.28 \text{ A} \quad \text{(eq. 23)}$$

$$I_{valley,HL} = 0.99 \text{ A} \quad \text{(eq. 24)}$$

Based on these two numbers, we can now compute the maximum power delivered by the converter at low and high line levels:

$$P_{max,LL} = \frac{1}{2} L_p \left(I_{peak,maxLL}^{\ 2} - I_{valley,LL}^{\ 2} \right) F_{SW} \eta_{LL} \approx 76 \text{ W} \quad \text{(eq. 25)}$$

$$P_{max,HL} = \frac{1}{2} L_p \left(I_{peak,maxHL}^{\ 2} - I_{valley,HL}^{\ 2} \right) F_{SW} \eta_{HL} \approx 104 \text{ W} \quad \text{(eq. 26)}$$

In this equation, we considered the low−line efficiency η_{LL} at 85% whereas it increased to 89% in high−line conditions. The power growth at high line reaches 37% compared to that at low line. In terms of currents, for a 19 V output, the maximum low−line current is 4 A and can go up to 5.5 A at the maximum input voltage. In our example, as we target a 60 W adapter (I_{out} = 3.2 A), the current computed by Equation 26 is way too high and a means has to be found to reduce it.

There are several available techniques such as developing an offset on the current−sense pin in relationship to the input voltage. Unfortunately, this technique is dissipative and affects the standby power or the efficiency in light load conditions. The best is to directly play on the maximum peak current limit based on the bulk voltage level without sensing it directly to avoid power dissipation.

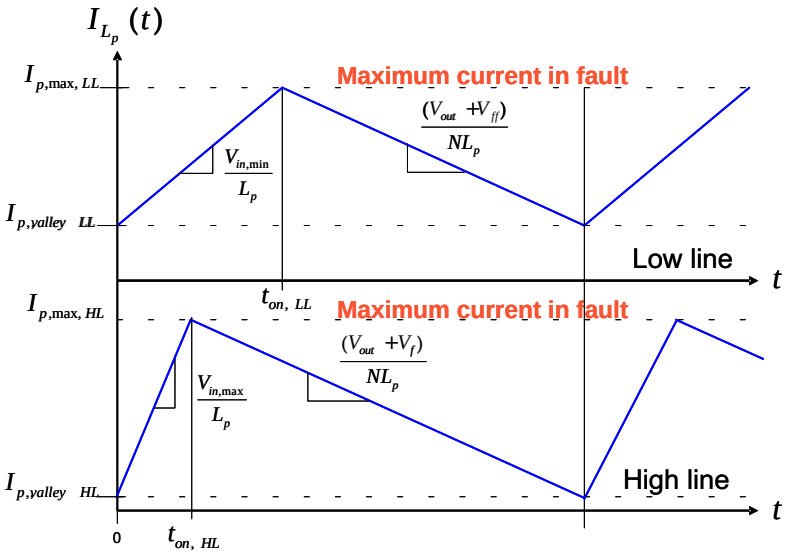

Figure 19. As the On Time Reduces at High Line, the Off Time Expands and Lets the Valley Current Go Down, Making the Operating Mode Closer to DCM: The Stored Energy Increases.

With the NCP1250, at low line and without any compensation, the maximum voltage across the current sense pin is limited to 0.8 V. To lower this signal at high line, a possible solution is to sum−up the 0.8 V reference voltage with a negative voltage proportional to the input voltage. This signal fortunately exists at no dissipation cost on the auxiliary winding, before the V_{CC} rectifying diode. It swings to $-N_{pa}V_{in}$ during the transistor on−time where N_{pa} is the turns ratio between the primary side of the transformer and the auxiliary winding. If we internally add a portion of this $-N_{pa}V_{in}$ level to the 0.8 V reference, we have a maximum peak current limit decreasing as the bulk voltage goes up. The implementation of this proprietary idea is described in Figure 20. As the auxiliary winding can be the seat of spurious oscillations at turn on, a small 300 ns blanking is performed on the signal to avoid false trigger of the downstream circuitry.

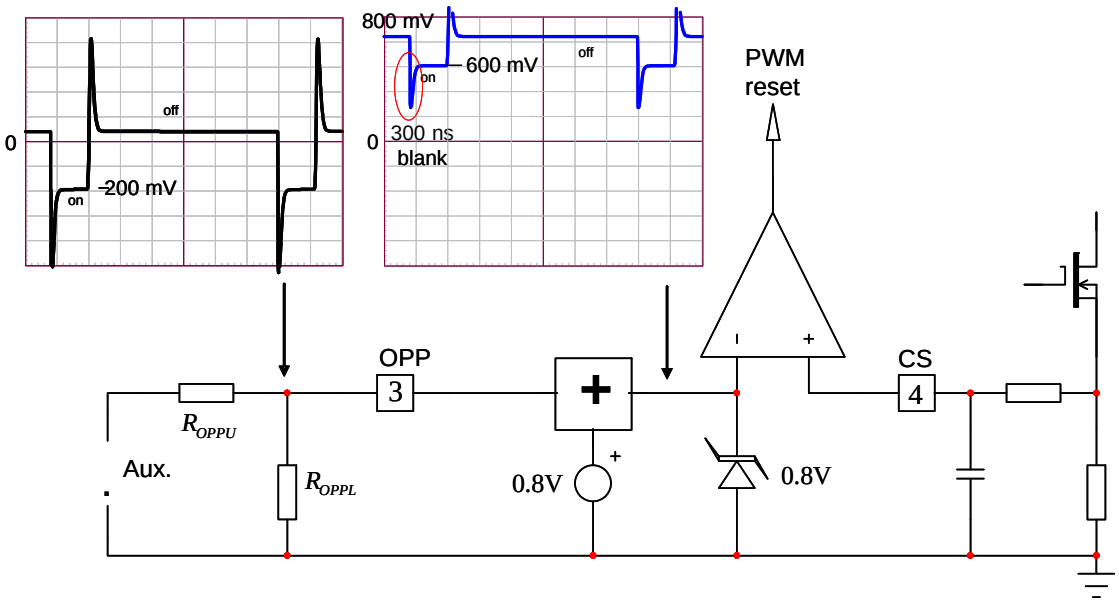

Figure 20. A Portion of the Auxiliary Voltage is Brought to the OPP Pin and Directly Subtracts from the 0.8 V Internal Reference Voltage. Here, the 0.8 V Reference Level is Decreased by 200 mV.

The calculation of the resistors tapping the auxiliary voltage is easy to compute. First, you need to know the exact amount of the required OPP level by extracting the peak current at high line producing the same output power as in low line operation. This is done by equating Equations 25 and 26 then subtracting the propagation delay contribution. You obtain:

$$I_{peak,max,HL} = \frac{F_{SW}L_p\eta_{HL}\Delta I_{Lp,HL}^{\ 2}}{2\eta_{HL}F_{SW}L_p\Delta I_{Lp,HL}} - \frac{V_{in,HL}}{L_p}t_{prop} \quad \text{(eq. 27)}$$

$$= 1.93\ A$$

In this equation, the term $\Delta IL_{p,HL}$ represents the inductor ripple at high line and is computed as:

$$\Delta I_{Lp,HL} = \frac{T_{SW}V_{in,HL}\left(V_f + V_{out}\right)}{L_p\left(V_f + V_{out} + NV_{in,HL}\right)} \quad \text{(eq. 28)}$$

Having in this example a sense resistor of 0.33 Ω, we produce a peak current of 0.8/0.33 = 2.42 A. To make this number go down to 1.9 A, we need to decrease the value of the reference voltage by:

$$V_{OPP} = I_{peak,max,HL} \times R_{sense} - V_{ref} \quad \text{(eq. 29)}$$
$$= 1.93 \times 0.33 - 0.8 \approx -160\ mV$$

We found that a negative voltage of ≈160 mV will do the job. On our prototype biased at 370 V, given a turns ratio between the primary and the auxiliary windings of 0.18, the auxiliary winding swings to:

$$-N_{pa}V_{in,max} = -0.18 \times 370 = -66.6\ V \quad \text{(eq. 30)}$$

To create the −160 mV level on pin 3, we can fix the pull−down resistor R_{OPPL} to 1 kΩ. Such low value guarantees a good noise immunity and low leakage from the pin. However, values up to 3 kΩ are acceptable. When biased at 160 mV, R_{OPPL} will see a current of:

$$I_{ROPPL} = \frac{160m}{1k} = 160\ \mu A \quad \text{(eq. 31)}$$

The upper resistor R_{OPPU} can then be computed as:

$$R_{OPPU} = \frac{66.6 - 160m}{160\mu} = 415\ k\Omega \quad \text{(eq. 32)}$$

This analytical method gives you a way to compute the resistive network for the OPP function. Nothing prevents you, however, from replacing R_{OPPU} by a 1 MΩ potentiometer and starting from its maximum value, slowly decreasing its value to force the protection to trip when the power supply exceeds the maximum current you accept at the highest line level.

Please note that the internal 0.8 V clamp prevents the maximum current sense level to be affected by an excessive positive bias accidentally applied on the OPP pin. For instance, should you apply 1 V on the OPP pin, the maximum peak current voltage excursion on the sense resistor will still safely be clamped at 0.8 V.

Over Voltage Protection

On top of the OPP function, pin 3 welcomes another circuitry dedicated to the latch of the device. If the OPP requires a negative signal during the on time, the OVP will sense a positive signal on pin 3 reaching 3 V. Therefore, when both OVP and OPP are combined on pin 3, the positive signal for the OVP must not bother the OPP operation. A simple network combining a Zener and a series diode is presented in Figure 20. When the auxiliary signal is negative, D_1 is blocked despite the forward bias of D_Z: the OPP network made of R_{OPPU} and R_{OPPL} can do its compensation job. When the power MOSFET turns off, the auxiliary winding jumps to the output voltage, reflected accordingly to the turns ratio between the power winding and the auxiliary winding. When this voltage exceeds the Zener voltage value, the voltage on pin 3 starts to rise cycle−by−cycle. However, thanks to the presence of D_1 and D_Z, the signal amplitude increases during the off time only and the OPP signal is kept intact. When the level on pin 3 reaches 3 V, the controller latches off. A total latch is often necessary in stringent situations, for instance when the optocoupler is broken or when the temperature in the adapter exceeds a safe level.

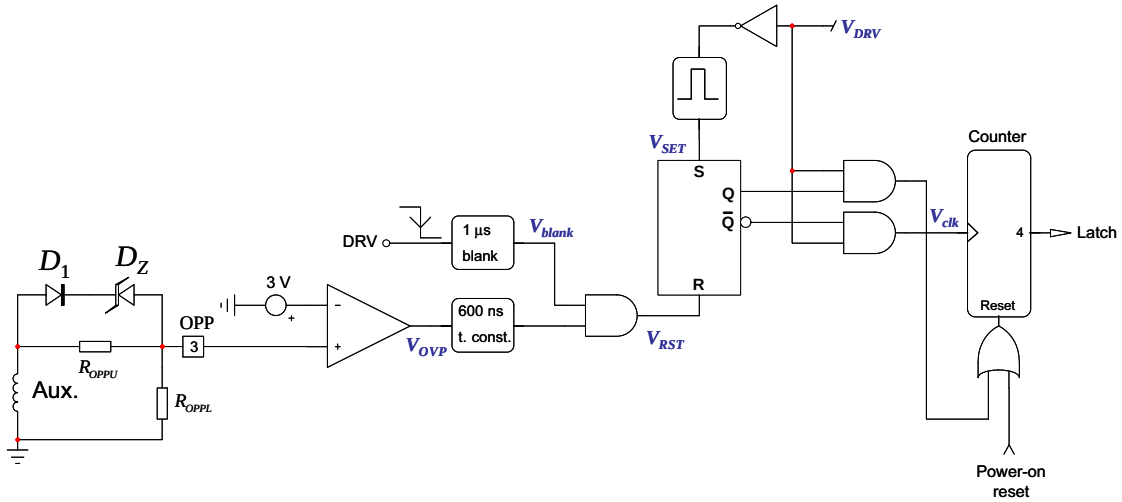

Figure 21. The Internal Circuitry Hosts a Divide−by−4 Counter That Helps Avoiding False Tripping

A latch circuitry can sometimes create troubles if made too sensitive to external perturbations for instance. For this reasons, the NCP1250 hosts an architecture combining blanking signals with a counter by 4. The simplified internal circuitry appears in Figure 21. The principle is to count 4 successive OVP events to latch off the controller. If the counter was advanced by 2 only (i.e. because of noise) and the 2 remaining OVP are ignored, the next clock cycle will reset the counter. Let's have a look on how it works. When the drive output goes down, at the end of the on time, a pulse sets the latch on the right−side of the picture: *Q* is "1" and $\overline{Q}$ is "0". If Q is high and stays high in the absence of an OVP event, it naturally resets the counter on the next clock pulse. If prior to this reset the OVP comparator senses a voltage on the OPP pin greater than 3 V, it toggles in the high state. Its level propagates through the 600 ns time constant and passes the AND gate provided it lasts longer than the 1 μs blanking time, started after the DRV pin is down. It resets the latch, making its output *Q* down while $\overline{Q}$ toggles to "1": the pulse is passed to the counter clock that increments by 1. When 4 events are sensed, the counter output n°4 goes high and latches the controller. When this occurs, all driving pulses are stopped and the V_{CC} pin is vigorously pulled down to around 7 V by an internal SCR. Reset occurs when the user cycles the V_{CC} down, e.g. by unplugging the converter from the wall outlet.

Filtering the Leakage Inductance Spikes

The auxiliary voltage is made of sharp transitions when swinging from $-N_{pa}V_{in}$ to N_{sa} (V_{out} + V_f) where N_{sa} represents the turns ratio between the secondary side and the auxiliary winding. These sharp discontinuities could couple to the OPP pin when a Zener diode is installed. This is because the diode features a parasitic junction capacitance that can propagate spurious spikes to the OPP pin. Despite a comfortable safety margin associated with a blanking circuitry, we recommend the addition of a simple *RC* network connected as what Figure 23 suggests. The values indicated on the sketch have been tested successfully. If necessary, a small capacitor of 10 − 22 pF can also be installed directly between pin 3 and pin 1 (GND), wired very close to the controller.

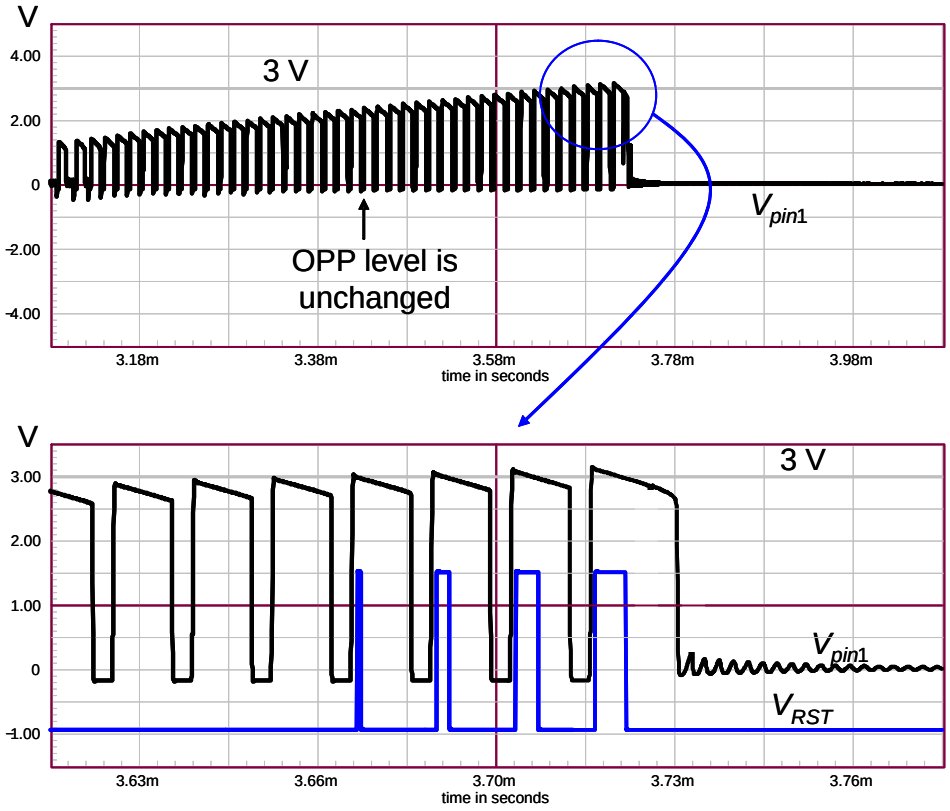

Figure 22. Simulation Results of an OVP Event Sensed by the NCP1250. Please Note That the OPP Level is Unchanged Despite the Positive Growth of the Auxiliary Signal.

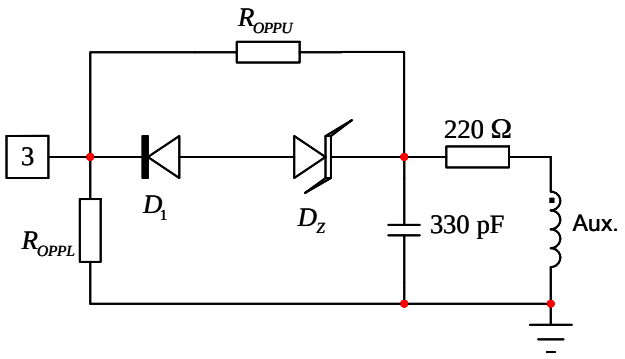

Figure 23. A Simple RC Filter Helps to Soften the Transitions Before Reaching the Zener Diode.

Latching the Controller from the Secondary Side

There are some cases where the observation of the auxiliary V_{CC} does not deliver the required precision. In this case, it is possible to monitor the secondary side output voltage and bring the information on the primary side via an optocoupler. However, the signal must be carried on pin 3 accounting for the presence of the OPP circuit which needs negative voltage. A resistor R_{opto} installed in series with the optocoupler collector limits the injected current in pin 3 when the OVP event occurs. The resistor must be sized to roughly limit the peak current in the internal ESD Zener (10 V breakdown) below 10 mA.

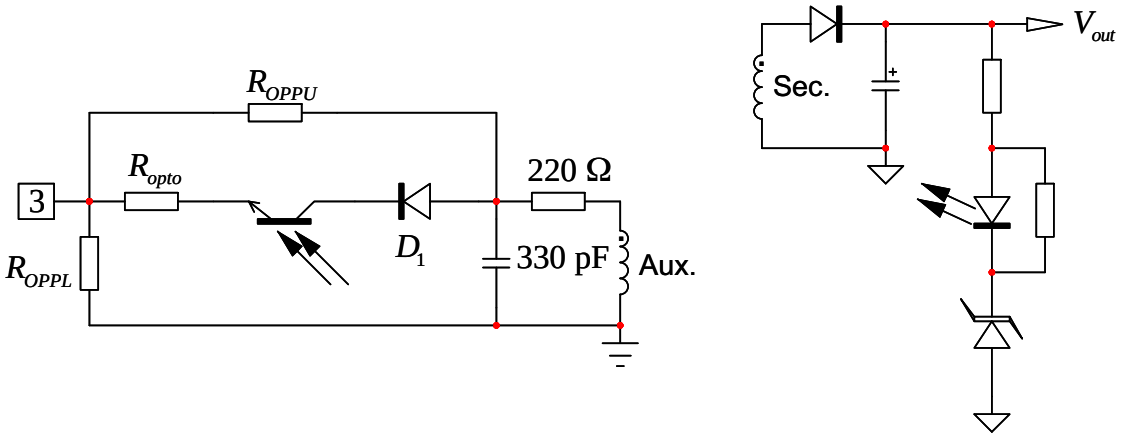

Figure 24. When the Optocoupler Conducts, it Positively Biases Pin 3 Over 3 V During the Off−Time Period

Over Temperature Protection

Over Temperature Protection (OTP) is a means to stop the adapter in case the ambient temperature exceeds a certain level. By adding a Negative Temperature Coefficient (NTC) resistor over the Zener diode, you have the possibility to trigger the latch when the temperature is too high. The proposed configuration appears in Figure 25.

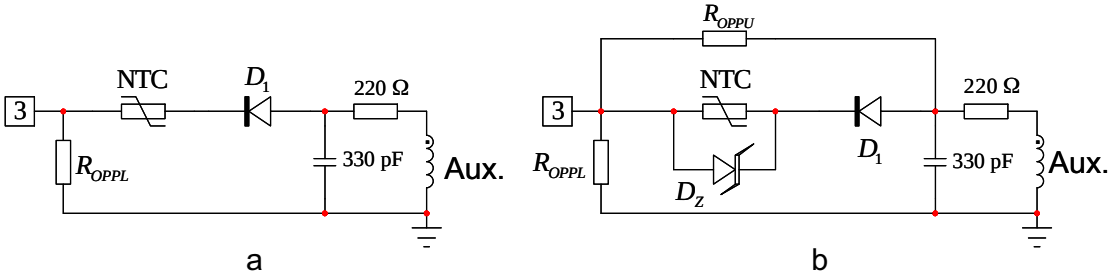

Figure 25. A NTC Resistor is Placed Across the Zener Diode and Offers a Way to Shutdown the Adapter When the Ambient Temperature Runs Way

In the left side of the picture, labeled “a”, the OTP is considered alone whereas it is coupled with the OVP on the right side (label “b”). The calculation is rather simple depending on the selected NTC device. What matters is the resistance at the temperature trip point. Let’s assume the selected NTC offers a resistance R_{110} of 8.8 kΩ at T_A =

110°C and the OTP solution alone is considered (Figure 25, a). If we consider a 3 V trip point on the OPP pin derived from a 14 V auxiliary level plateau, then the pull−down resistor R_{OPPL} must be calculated as follows:

$$R_{OPPL} = \frac{V_{latch}R_{110}}{\left(V_{aux} - V_f\right) - V_{latch}} = \frac{3 \times 8.8k}{(14 - 0.6) - 3} \approx 2.5\ k\Omega \quad \text{(eq. 33)}$$

Where V_f represents the voltage drop from the series diode D_1. This diode ensures a positive bias only during the off time to avoid bothering the OPP circuitry. When the temperature will increase, the voltage will also slowly grow on pin 3 (during the off time only) until 3 V are reached. At this point, the controller stops all operations and goes into a latched mode. Reset occurs when the user cycles the power off and on.

When combined with the OPP, the calculation must include the requirement of negatively biasing pin 3 during the on time. Let's use the same NTC resistance as in the above example. The pull−down resistor value does not change and is still 2.5 kΩ as given in Equation 33. Now that the pull−down OPP resistor is known, we can calculate the upper resistor value R_{OPPU} to adjust the power limit at the chosen output power level. Suppose the OPP requirement dictates a 200 mV decrease from the 0.8 V set point. In our application, as the on−time swing on the auxiliary anode is −67.5 V, we need to drop over R_{OPPU} a voltage of:

$$V_{ROPPU} = N_{pa}V_{in} - V_{OPP} = 67.5 - 0.2 = 67.3\ V \quad \text{(eq. 34)}$$

The current circulating in the pull down resistor R_{OPPL} in a 200 mV bias will be:

$$I_{ROPPL} = \frac{200m}{2.5k} = 80\ \mu A \quad \text{(eq. 35)}$$

The R_{OPPU} value is therefore easily derived:

$$R_{OPPU} = \frac{V_{ROPPU}}{I_{ROPPL}} = \frac{67.3}{80\mu} = 841\ k\Omega \quad \text{(eq. 36)}$$

Experiments carried on an adapter combining both OPP, OVP and OTP have shown very precise trip points in both situations, over voltage and over temperature.

Conclusion

This application note describes how a controller housed in a TSOP6 package can offer the flexibility and ease of use usually found in much larger packages. With its extended jittering capability and a unique non−dissipative OPP circuitry, the NCP1250 represents a serious candidate in designs where ease of implementation and cost sensitivity are two important variables.

References

1. C. Basso, "Switch Mode Power Supplies: SPICE Simulations and Practical Designs", McGraw−Hill, 2008

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