AND9115/D

NCP1255, a Controller with Peak Output Power Capability

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APPLICATION NOTE

The NCP1255 capitalizes on the NCP1250 circuitry to which several enhancements have been brought. Specifically tailored for applications requiring peak power capability, the part can increase its switching frequency on the fly while making sure the maximum peak current setpoint is not exceeded. The total available power is authorized for a period of time defined by a programmable timer. This timer is either of full duration in an overload situation or divided by 4 in presence of a short-circuit event. The typical application of such a control scheme is a converter that is thermally tailored for medium power level while capable of delivering an extra amount of power for a short period of time only.

Using the same protection set as NCP1250 to which a brown-out protection has been added, the NCP1255 is the perfect candidate when high performance, safety and cost sensitivity are design factors.

General Description

The part is encapsulated in a SOIC−8 package but a reduced-feature set version (no brown-out and the timer is internally set), the NCP1254, also exists in a tiny TSOP−6 package. Featuring a low-power BiCMOS process, the die accepts to work with V_{CC} levels up to 35 V, safely clamping the drive voltage below 12 V. With its 15 μA start-up current, a high-value resistive network can be used in offline applications to crank the converter, naturally minimizing the wasted power in high-line conditions. In nominal load operations, the switching frequency of this peak-current mode control circuit is 65 kHz.

When the power demand goes up, the controller increases the peak current setpoint until it reaches the upper limit (0.8 V over R_{sense}). At this point, the output power increase can only be answered by further shifting the switching frequency up until it reaches another limit, 130 kHz. The maximum power is thus obtained at this moment. On the contrary, in light-load operations, the part linearly reduces its switching frequency down to 26 kHz and enters skip cycle as power goes further down. This mode of operation favors higher efficiency from high to moderate output levels and ensures the lowest acoustic noise in the transformer. To improve the EMI signature, a low-frequency modulation brings some dither to the switching pattern. Unlike other circuits, the dither is kept in foldback and peak excursion modes, continuously smoothing the noise signature.

The part hosts several new protections such as an auto-recovery brown-out circuit adjustable via a resistive divider. A double hiccup on the V_{CC} brings down the average input power while in auto-recovery fault mode. Regulation is ensured by pulling down the dedicated pin via an optocoupler, driven from the secondary side by a TL431 or a cheap Zener diode. Figure 1 shows the NCP1255 in its typical implementation within a 12 V converter.

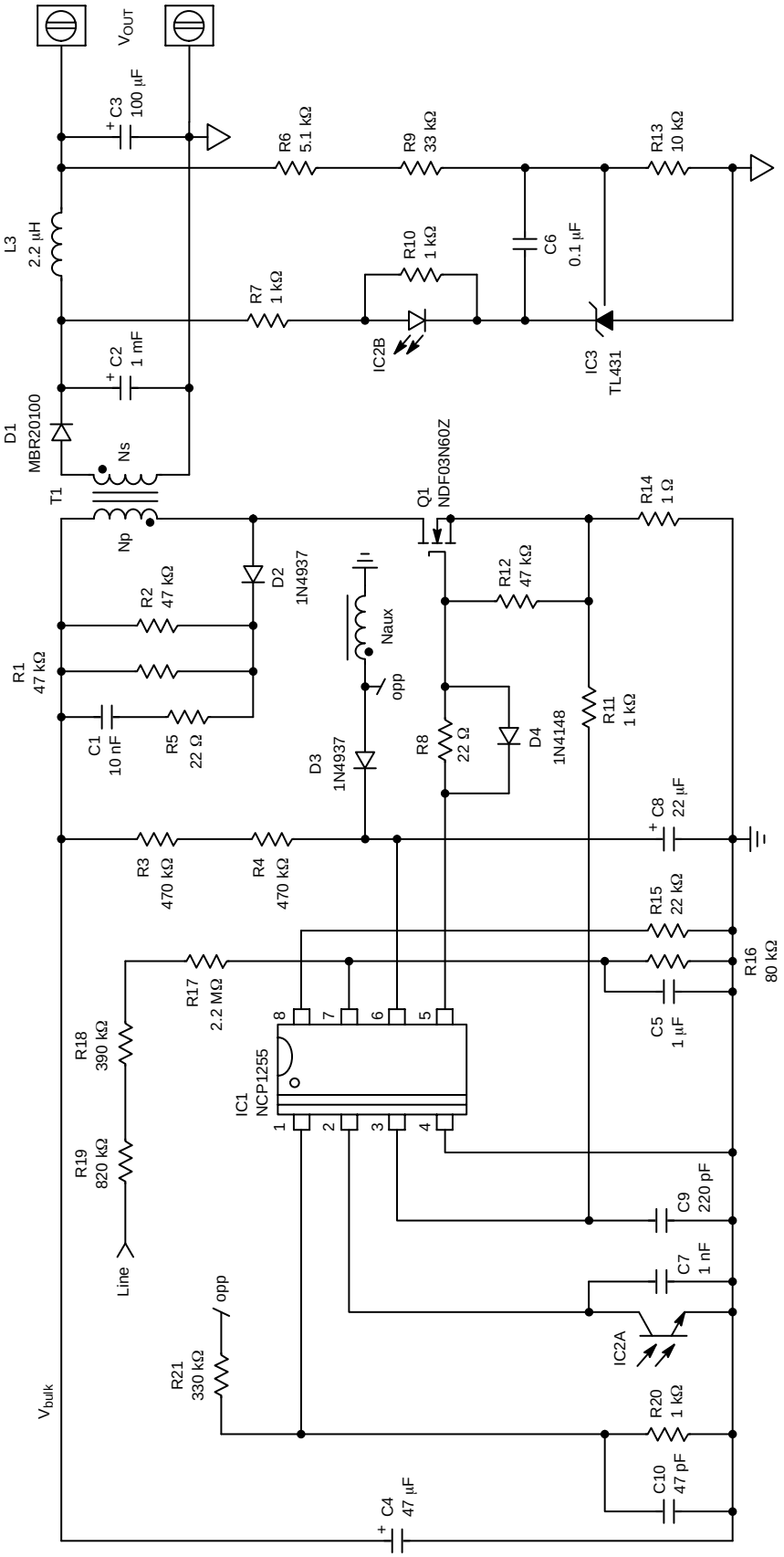


Figure 1. The Typical Implementation of the NCP1255 in an Isolated Flyback Converter

Pin 6 − The V_{CC} Supply

The chip supply is brought in via pin 6. Upon start-up, for a voltage less than 18 V (typical), the internal consumption is limited to 15 μA maximum. It suddenly changes to around 2 mA as the controller starts to switch at 65 kHz on a 1 nF capacitive load when V_{CC} reaches 18 V. The auxiliary voltage can go down to around 9 V before the controller safely stops the switching pulses.

The classical configuration to start-up the controller appears in Figure 2. We can see a start-up resistor, R_1, connected to the bulk voltage. It generates a current I_1. Part of this current, 15 μA, is diverted inside the chip. This current is fairly constant up to V_{CC} equals 18 V. The current flowing inside the V_{CC} capacitor is thus:

$$I_2 = I_1 - I_{CC1} \qquad \text{(eq. 1)}$$

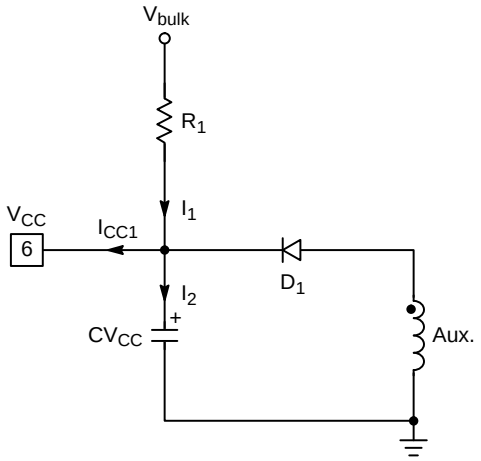


Figure 2. A Simple Resistive String Brings the Necessary Current to Charge CV_{CC}

When the controller starts to switch (i.e. V_{CC} is 18 V), the current consumption increases suddenly. The consumption depends on the MOSFET gate charge Q_G but also on the circuit internals. As I_1 is purposely kept small to minimize the wasted power in R_1 at high line, all the current is now delivered by the V_{CC} capacitor. This element is alone to power the controller and the voltage across its terminals falls out. Before the voltage on pin 6 reaches the V_{CCmin} level, the auxiliary voltage must build quickly enough to take over the controller supply via D_1. If the V_{CC} capacitor is small, the voltage drops too quickly and the converter cannot start-up properly: the pulses are stopped and the current consumption switches back to 15 μA for a new re-start. An auto-recovery hiccup mode takes place as shown in Figure 3. Please note that the hiccup is now doubled compared to that of the NCP1250, naturally ensuring the lowest average input power consumption in a fault condition.

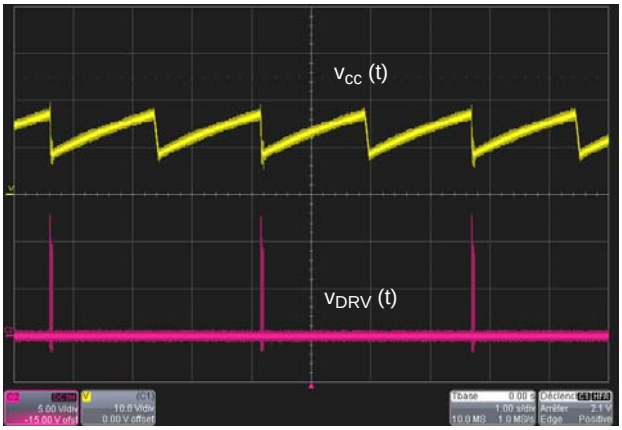


Figure 3. The Part Enters an Auto-recovery Hiccup Mode in Case the Auxiliary V_{CC} is Missing
(The Double Hiccup Reduces the Average Input Power when the Part is in Fault Mode)

Before calculating R_1, we have to know what capacitor value can maintain enough voltage on the V_{CC} pin until the auxiliary winding takes over. The most difficult task in this calculation is to estimate the worst-case time at which the auxiliary voltage takes over. This worst case happens when the output power P_{out} is maximal and the input voltage V_{in} is minimal. Based on our experience, a time-duration of 25 ms is a reasonable value to start with. Then, experiments on the prototype will either confirm the assumptions or will tell you to consider a different value. For the capacitor calculation, we have to check the minimum available voltage excursion across the capacitor from the specifications. Reading the NCP1255 data-sheet, we find that this occurs when both the start-up voltage and the $UVLO_{low}$ thresholds are at minimum:

$$\Delta V_{CC} = VCC_{(on),\,min} - VCC_{(min),\,min} = \\ = 16 - 8.3 = 7.7\ V \qquad \text{(eq. 2)}$$

If we consider a 25 ms time duration for the auxiliary voltage takeover and a total consumption current around 4.5 mA:

- Part Consumption alone is ≈ 1.7 mA
- Our 4 A MOSFET shows a total gate-charge Q_G of 20 nC. At a 130 kHz frequency, it induces an average current of:

$$20\,n \times 130\,k = 2.6\,mA \qquad \text{(eq. 3)}$$

- Total consumption is therefore around 4.3 mA, increased to 4.5 mA to include some margin

To hold the charge a time that is long enough, the V_{CC} capacitor must show a capacitance above the following value:

$$C_{V_{CC}} \geq \frac{ICC_3 t_2}{\Delta V_{CC}} \geq \frac{4.5\,m \times 25\,m}{7.7} \geq 14.6\,\mu F \qquad \text{(eq. 4)}$$

Given the manufacturing dispersions on this type of component, it is necessary to take tolerance precautions. Typically, we should select a 22 μF type as we can expect wide variations over time and manufacturing lots. Unfortunately, in some cases, as the startup current has to be minimized for obvious power dissipation constraints, we cannot increase the V_{CC} capacitor too much otherwise the start-up time will suffer (less than 3 s for notebook ac-dc adapters). Now, the 25 ms might be too conservative and a 10 μF capacitor may finally be the right choice. It is also possible to slightly increase the peak power capability of the converter and make it reach regulation sooner. Once the converter is assembled, a test is necessary to check this out. Worst case occurs at maximum loading conditions on a warmed-up transformer at low ambient temp where the capacitor Equivalent Series Resistance (ESR) is the highest. The test result carried upon the adapter with a 10 μF capacitor appears in Figure 4 and confirms that enough margins exist with this value.

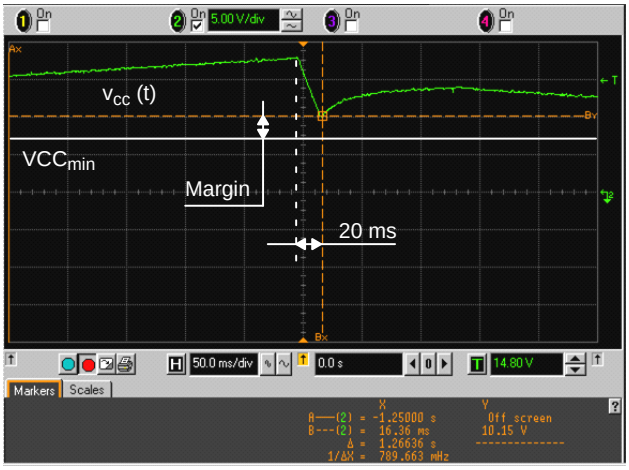


Figure 4. A Start-up Sequence at Maximum Output Power Shows Enough Margins on the V_{CC} Capacitor Voltage

The capacitor value being known, how much current do we need for I_1? If we adopt a 10 μF capacitor and need a start-up time less than 2.9 s at the lowest input voltage (85 V rms or 120 V rectified), what current needs to be injected into C_{Vcc} to raise from 0 to $V_{CC(on),max}$?

$$I_1 \geq \frac{V_{CC(on),\,max}\, C_{V_{CC}}}{t_{startup}} \geq \frac{20 \times 10\,\mu}{2.9} \geq 69\,\mu A \qquad \text{(eq. 5)}$$

These 69 μA, to which 15 μA must be added (I_{CC1}), have to be delivered from the lowest input line. This is 120 V dc in a classical design intended to operate on a universal mains input. What resistor value must then be used to reach that number?

$$R_{startup} = \frac{V_{bulk,\,min} - V_{CC(on),\,max}}{I_1} = \qquad \text{(eq. 6)}$$

$$= \frac{120 - 20}{84\,\mu} \approx 1.2\,M\Omega$$

Unfortunately, in high-line conditions (265 V rms), this resistor is permanently biased and dissipates power. If we neglect the V_{CC} value, the dissipated power amounts to:

$$P_{R_{startup,\,hiline}} = \frac{V_{bulk,\,max}^{\,2}}{R_{startup}} = \frac{375^2}{1.2\,M} = 117\,mW \qquad \text{(eq. 7)}$$

This extra power dissipation is not a big problem if you plan to boast a no-load standby power less than 300 mW. On the contrary, if you wish to comply with a standard asking less than 100 mW at high line, (eq. 7) tells you that it is impossible.

Looking for a Half Cycle

Rather than connecting the start-up network to the dc rail, V_{bulk}, why not connecting it directly to the mains? As one bridge diode will remain in series with the return path, we will benefit from a half-wave rectification, leading to a lower average value than on the bulk rail, hence lower power dissipation on the start-up resistor. This is what Figure 5 suggests where two resistors, R_1 and R_2, actually route both positive and negative waves to the V_{CC} capacitor.

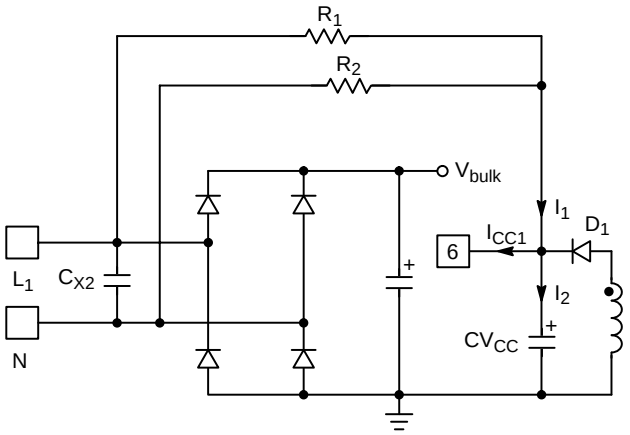


Figure 5. The Direct Connection to the Mains Significantly Reduces the Wasted Power on the Start-up Resistor

Now, it is interesting to calculate the value of resistances R_1, R_2 to keep the same start-up current as in the case where we have the direct connection to the bulk capacitor. What total current value charges CV_{CC}? The average current provided by the two start-up resistors is expressed by the following formula, neglecting the V_{CC} value as CV_{CC} charges up:

$$I_{1,\,avg} \approx \frac{V_{in,\,peak}}{\pi R_1} + \frac{V_{in,\,peak}}{\pi R_2} \qquad \text{(eq. 8)}$$

If R_1 is equal to R_2, then:

$$I_{1,avg} = \frac{2V_{in,\,peak}}{\pi R} \qquad \text{(eq. 9)}$$

with $R = R_1 = R_2$.

If we consider a 85 V rms input voltage, then a 84 μA charging current will require the following resistor values:

$$R = \frac{2V_{in,\,peak}}{\pi\, I_{1,\,avg}} = \frac{2 \times 120}{3.14159 \times 84\,\mu} = 910\,k\Omega \quad \text{(eq. 10)}$$

The average power dissipated per resistance at the highest input level (265 V rms) will be:

$$P_R = \frac{V_{in,\,peak}^{\,2}}{4R} = \frac{375^2}{4 \times 910\,k} \approx 39\,mW \quad \text{(eq. 11)}$$

or a total of 78 mW for both elements. Another benefit of this configuration is that these resistors play the role of the X2 capacitor discharge path. As you know, the IEC−950 safety standard imposes a 1 s time constant to discharge a capacitor directly installed across the input line and which value is above 0.1 μF. By using the configuration suggested in Figure 5, the resistors play a charging role for the start-up sequence but also provide a discharge path for the X2 capacitor. No need to install more dissipating components.

There is another thing you must think about when designing the start-up network. If keeping the current at the lowest value is a must for a low standby power, it obviously slows down the start-up time. In some applications, where standby power is a less stringent parameter, it is desirable to crank the power supply in the shortest possible time. One way of doing it is to increase the start-up current. However, the auto-recovery circuitry works by discharging the V_{CC} capacitor via an internal consumption of around 1 mA. Therefore, if you force a current I_1 greater than 1 mA, then the controller will no longer be able to discharge the V_{CC} capacitor and auto-recovery will be lost.

Another parameter that is worth considering, is the parasitic capacitor offered by a rectifying diode when blocked. In our calculations, we considered a nice continuous half-wave signal feeding the start-up resistors. The reality is different as the rectifying diodes only conduct during the refueling of the bulk capacitor, probably a few milliseconds. For the rest of the time, they are blocked. Therefore, the current in R_1 (or R_2) is mainly provided by these parasitic capacitors during the considered half-wave portion of the sinusoid. Connecting an oscilloscope over the V_{CC} pin could affect the parasitic path through the earth and might change the charging current, disturbing the measurement. To measure the start-up time, it is certainly better to only look at the ac input current using a dedicated current probe while the output of the converter is charged with a resistive load (an electronic load could, again, affect the parasitic return and influence the measurement). Monitor the time at which the converter is plugged (this is t = 0 and you have a sharp in-rush spike) and look at the current shape until it is significantly affected. This is the time at which the converter operates and V_{CC} has reached the turn-on level. As the power supply only requires a few tens of milliseconds to reach its regulation level, considering the time from t = 0 to the change in current shape as the start-up time will not create a significant measurement error. On our adapter board, we have captured a typical start-up current signature obtained at an input voltage of 85 V ac. It shows a start-up time of 2.4 s.

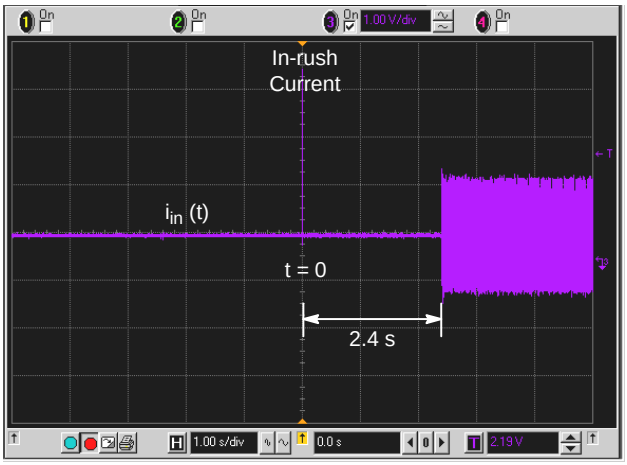


Figure 6. On this Plot, the Start-up Time is Measured at the Moment the Converter is Plugged to the Moment where the Current Significantly Changes

(The Load is a Passive Resistor and No Oscilloscope Ground is Connected to the Board)

Pin 5 − The Driver Output

The part features a CMOS-based output driving stage capable of sourcing 300 mA peak while sinking 600 mA. As the part accepts V_{CC} voltages up to 35 V, it is important to clamp the voltage actually applied to the gate-source terminals of the selected power MOSFET. The $R_{DS(on)}$ of a high-voltage MOSFET is usually defined at a 10 V V_{GS} bias. Going below this value will make the resistance increase, together with the conduction losses. On the contrary, biasing the MOSFET well beyond this 10 V reference, will only reduce the $R_{DS(on)}$ by a small amount, unnecessarily increasing the power dissipation in the driver. Also, at a certain bias level, the MOSFET lifetime can also be affected. The internal 12 V clamp offers a safe operating choice.

Dissipation wise, it is now important to check that the selected MOSFET complies with the thermal capability of the package. A SOIC−8 package features a junction-to-ambient thermal resistance of 178°C/W. When you add some copper around the device, let's say a square centimeter of 35 μm copper, the thermal resistance drops around 110°C/W. If we operate the part in an environment where the ambient temperature T_A is 70°C and we want to limit the maximum junction temperature to less than 110°C, then the maximum allowable power the package can dissipate is:

$$P_{max} = \frac{T_{j,\,max} - T_A}{R_{\Theta J-A}} = \frac{110 - 70}{110} \approx 364\,mW \quad \text{(eq. 12)}$$

What are the sources justifying power dissipation in a PWM controller? The first is the inherent consumption of the blocks (clock, comparators, references etc.). On the

data-sheet, this is the parameter I_{CC2} which also includes the various cross-conduction currents from the unloaded driver output. We have 1.8 mA. The other source is the average current necessary to drive the selected power MOSFET. This average current is nothing else than the total gate-charge Q_G multiplied by the switching frequency F_{SW}:

$$I_{DRV,\,avg} = Q_G F_{SW} \qquad \text{(eq. 13)}$$

If we supply the IC from a V_{CC} rail, then the power dissipation becomes:

$$P_D = \left(I_{CC2} + I_{DRV,\,avg}\right) V_{CC} \qquad \text{(eq. 14)}$$

Let's assume the V_{CC} is set to 14 V. From (eq. 12) and (eq. 14), the maximum authorized current to drive the MOSFET becomes:

$$I_{DRV,\,avg} = \frac{P_D}{V_{CC}} - I_{CC2} = \frac{364\,m}{14} - 2\,m = 24\,mA \qquad \text{(eq. 15)}$$

According to (eq. 15), we can compute the maximum allowed Q_G for a junction temperature kept below 110°C in a 70°C atmosphere:

$$Q_{G,\,max} = \frac{I_{DRV,\,avg}}{F_{SW}} = \frac{24\,m}{65\,k} > 200\,nC \qquad \text{(eq. 16)}$$

This number is fairly large and quite comfortable actually. Does it mean that the controller is capable to safely drive large gate-charge MOSFETs? Certainly not. The moderate driving capability of the NCP1255 would generate unacceptable switching losses and the total efficiency would suffer.

Given these power dissipation constraints, it is important to look at the selected MOSFET data-sheet. For instance, a NDF04N60Z exhibits a total gate charge of 19 nC which is ok to be used with the NCP1255. Beyond these MOSFET sizes, for a 6 A or bigger, we recommend to add a small PNP transistor to help strengthening the turn-off discharge. This is what Figure 7 shows. In this picture, Q_2 is driven by R_{16}, adjusted to shape the turn-on time and soften the EMI signature of the converter. When pin 5 is down to ground, Q_1 is activated and blocks Q_2.

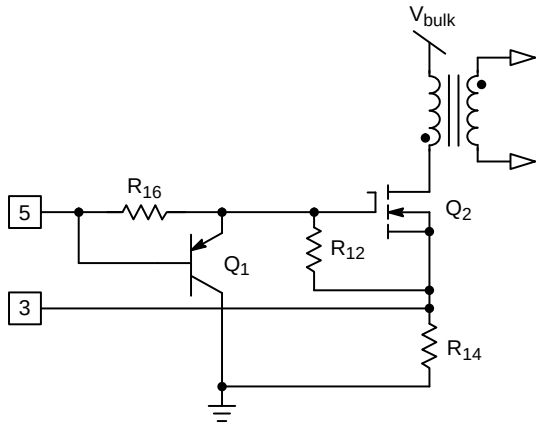


Figure 7. A Small PNP Transistor Vigorously Pulls the Gate Down at Turn Off

To avoid any production issues, e.g. the gate is open because the controller is not properly soldered for instance, R_{12} keeps the MOSFET blocked and prevents any destruction.

Pin 3 − The Current Sense Input

The current sense pin routes the voltage developed across the sense resistor to a Leading Edge Blanking (LEB) circuit before reaching the PWM reset comparator. The LEB principle is to blind the current sense comparator for 300 ns and avoid false tripping because of spurious signals found on the sense voltage. The internal schematic appears in Figure 8 and discloses two switches.

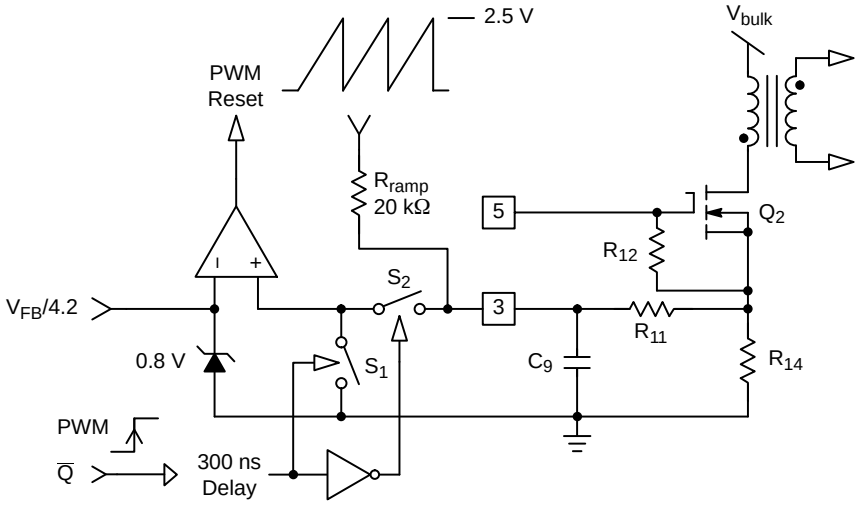


Figure 8. The Current Sense Pin Monitors the Voltage Coming from the Sense Resistor but also Contributes to Inject Slope Compensation

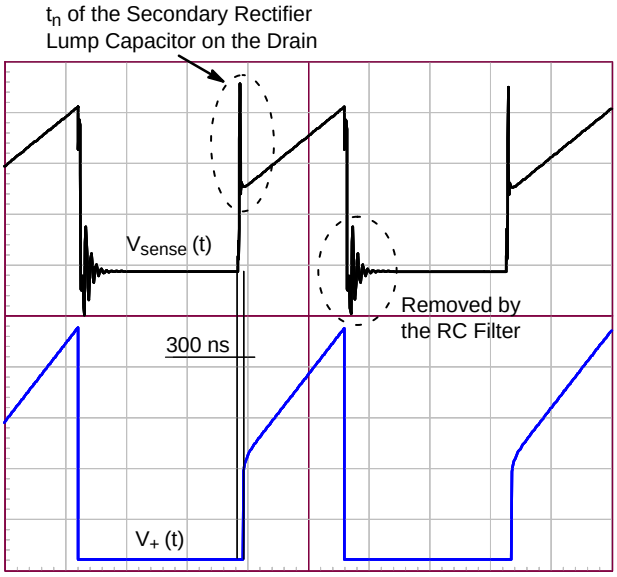


Figure 9. The LEB Circuitry Removes All Oscillations Found on the Current Sense Signal

When the driver output is high, the grounded switch S_1 is closed and the series switch S_2 is open. This network fully isolates the current-sense comparator from the CS pin. After 300 ns have elapsed, S_1 opens and S_2 closes, routing a clean signal to the (+) of the comparator (Figure 9).

The current-sense pin hosts another function which is the slope compensation. Slope compensation is necessary to tame the sub-harmonic oscillations that occur in a current-mode converter operating in a Continuous Conduction Mode (CCM) with a duty ratio approaching or exceeding 50%. The cure to this problem is to subtract a ramp of the correct amplitude from the feedback signal or add the same ramp to the current sense pin. This latter is the technique adopted for the NCP1255 and described in Figure 8. A ramp signal is available from the clock circuitry. Once internally buffered, this signal drives the CS pin via a 20 kΩ resistor. Therefore, by adjusting the resistor placed in series with the current sense resistor signal – R_{11} in Figure 8 – it is possible to create a voltage divider and precisely adjust the level of slope compensation.

In the NCP1255 controller, the oscillator ramp features a 2.5 V swing. If the clock operates at a 65 kHz frequency, then the available oscillator slope corresponds to:

$$S_{ramp} = \frac{V_{ramp,peak}}{D_{max} T_{sw}} = \frac{2.5}{0.8 \times 15\,\mu} = 208\ kV/s \text{ or } 208\ mV/\mu s \quad \text{(eq. 17)}$$

In a flyback design, let's assume that our primary inductance L_p is 600 µH, and the SMPS delivers 19 V with a N_p:N_s ratio of 1:0.25. The off-time primary current slope S_p is thus given by:

$$S_p = \frac{(V_{out} + V_f)\frac{N_p}{N_s}}{L_p} = \frac{(19 + 0.8) \times 4}{600\,\mu} = 132\ kA/s \quad \text{(eq. 18)}$$

If we have a sense resistor R_{sense} of 330 mΩ, the above primary current ramp turns into a voltage ramp of the following amplitude:

$$S_{sense} = S_p R_{sense} = 208\ k \times 0.33 \approx \approx 69\ kV/s \text{ or } 69\ mV/\mu s \quad \text{(eq. 19)}$$

A common law to stabilize a current-mode converter is to select 50% of the inductor downslope as the required amount of ramp compensation. If we stick to this recommendation, then we shall inject a ramp whose slope is ≈34 mV/µs. As the internal compensation is of 208 mV/µs, the divider ratio (divratio) between R_{comp} and the internal 20 kΩ resistor has to be:

$$divratio = \frac{34\ m}{208\ m} = 0.163 \quad \text{(eq. 20)}$$

The series compensation resistor value is thus:

$$R_{comp} = R_{ramp}\, divratio = 20\ k \times 0.163 = 3.3\ k\Omega \quad \text{(eq. 21)}$$

A resistor of the above value will then be inserted from the sense resistor to the current sense pin as shown in Figure 8 (R_{11}). We recommend adding a small capacitor of 100 pF, from the current sense pin to the controller ground for an improved immunity to the noise. This is the capacitor C9 in Figure 8. Please make sure both components are located very close to the controller.

Maximum Peak Current Limit and Short-circuit Protection

In case the feedback signal is lost, e.g. if the optocoupler is destroyed or the output undergoes a short-circuit, the peak current setpoint will be pushed to the maximum level. In this controller, without Over Power Protection (OPP) signal on pin 1, the maximum allowable level on the current sense pin is 0.8 V. As this is considered a fault condition, the controller must protect the converter against temperature runaway or an over current in the power cable.

This controller differs from the NCP1250 in the sense that two timers with different durations are implemented when a fault mode is entered. The circuit distinguishes a transient overload (OVL) from a permanent output short circuit (SC). For a transient overload, the controller starts a timer which duration is adjustable through a pull-down resistor connected to pin 8. The countdown is initiated as the maximum peak current setpoint is hit. This limit can be 0.8 V or less if some OPP signal is injected into pin 1. The overload timer can be adjusted up to 1 s if necessary. Once the transient event is gone, e.g. the current limit returns within normal conditions, the timer is simply reset. If for any reason the overload becomes a short circuit, the feedback voltage jumps to its open-loop voltage, around 4.5 V. The controller senses a short circuit when it detects that the feedback voltage exceeds 4 V. Please note that it also happens upon start-up, until the loop takes over. At this moment, the frequency is maximum (130 kHz typically) and the timer duration is divided by 4. For instance, should

you have programmed an OVL timer of 250 ms (R_{pin8} = 7 kΩ), when the controller senses a short circuit, this timer becomes 63 ms. The circuit implements a digital circuitry whose low-frequency clock is set by the resistor hooked to pin 8. By sensing a short-circuit condition, the controller simply multiplies by 4 the timer clock, forcing a faster countdown. It means that wherever the OVL timer is within its countdown, when a SC condition is met, the countdown goes faster. When the timer is elapsed, all pulses are stopped and the part enters a double-hiccup auto-recovery mode.

At this moment, the V_{CC} capacitor remains alone to self-supply the controller and the voltage across its terminals falls down. Again, as the current consumed by the controller is around the mA, you have to make sure the start-up current is not higher than this value otherwise the operation will be perturbed. When V_{CC} finally reaches the $VCC_{(min)}$ value, around 9 V, the circuit is reset and the consumption goes back to 15 μA (max): the V_{CC} level starts to rise towards VCC_{ON}, initiating a start-up sequence. Because of the double-hiccup configuration, this start-up is ignored and V_{CC} quietly falls down again. When it finally reaches VCC_{ON} for the second time, then a fresh start-up sequence takes place with soft-start and brown-out sensing. The double hiccup is nice as it naturally increases the off-time duration between two start-up sequences where maximum power is delivered. It has the effect of reducing the average input power in fault and the rms current in the output cable. Figure 10 shows a typical double-hiccup operation.

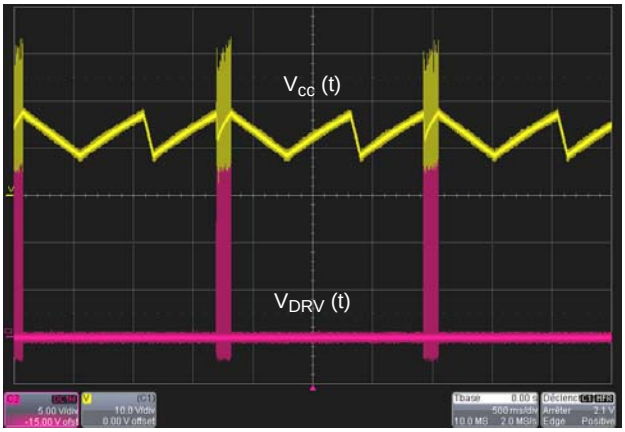


Figure 10. In Presence of a Short-circuit Or an over Power Condition
(a Timer Shuts Down the Controller and Makes it Enter an Auto-recovery Protective Mode)

Pin 4 – The Circuit Ground

Usually, there is not much to say about the circuit ground. However, even if we deal with moderate-power converters, we need to apply a few rules pertinent to the power electronics world. The most important one is to make sure all ground-referenced sensitive signals returns to a quiet 0 V point, the controller ground pin. For instance, the optocoupler collector is connected to the feedback pin of the NCP1255 (pin 2) whereas its emitter pin must connect to the ground. As the optocoupler is often placed remotely from the controller, it can be tempting to connect the emitter to the closest ground trace, perhaps the sense resistor return. Please do not otherwise spurious oscillations could take place and make the whole converter unstable, especially in fault mode where large currents must be interrupted. Rather, route a copper trace along the one that already routes the collector and connect it to the controller ground point. Make sure the compensating capacitor (C_7 in Figure 1) is not placed across the optocoupler, but right between the controller pins 2 and 4. The recommendations also apply for the current sense network (C_9 and R_{11} in Figure 1) that must be placed very close to the controller. A copper trace from R11 can then be placed to reach the sense resistor. Even if this trace is long, it is of less importance as the conveyed signal is low impedance. Figure 11 shows an example of Printed Circuit Board (PCB) routing when using the NCP1255.

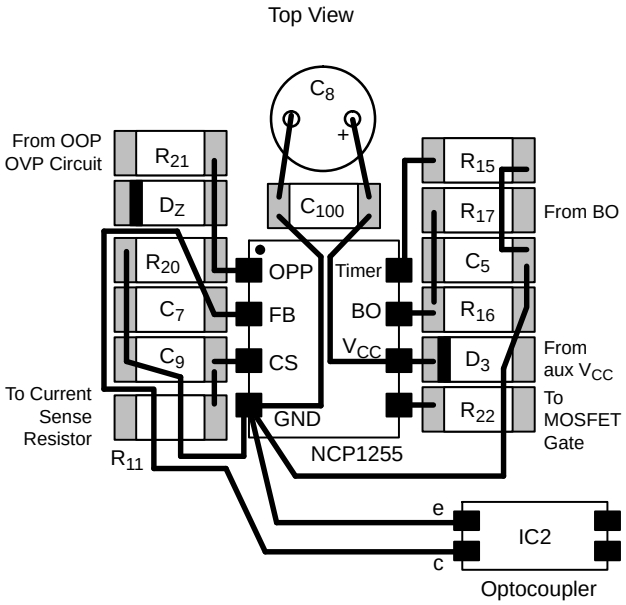


Figure 11. Decoupling Components Must be Installed Very Close to the Controller
(Above is a Possible Routing Way)

Pin 2 – The Feedback Pin

The feedback pin in a current-mode-controlled power supply is the control input that sets the inductor peak current on a cycle-by-cycle basis. The internal circuitry around pin 2 in the NCP1255 appears in Figure 12.

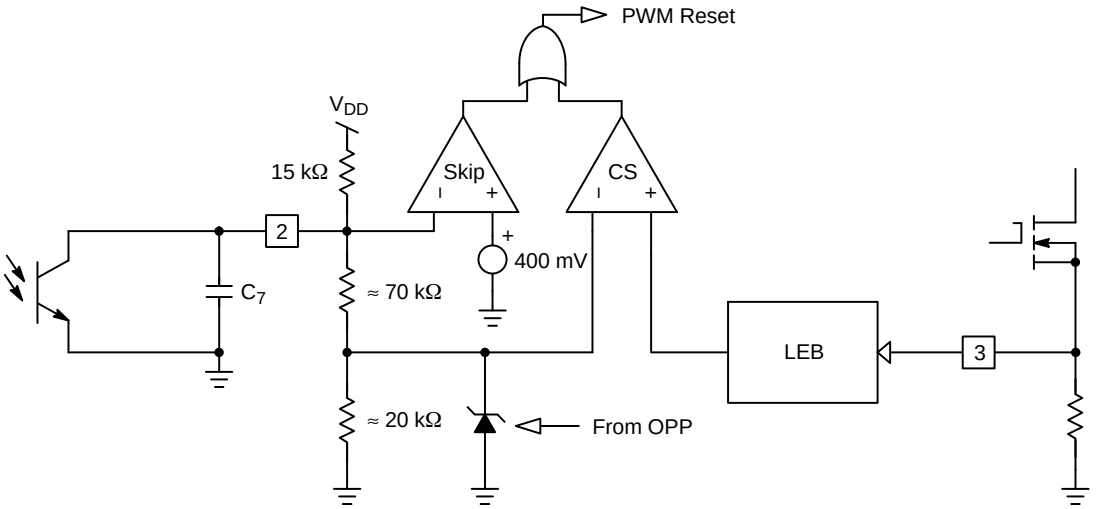


Figure 12. The Internal Simplified Schematic of the Feedback Circuitry

The regulation is obtained by pulling the feedback pin to ground via the optocoupler collector. The division ratio from the feedback pin to the current sense comparator is 4. However, the maximum current voltage setpoint cannot exceed 0.8 V.

Unlike the NCP1250, the NCP1255 authorizes a switching frequency excursion in both directions. The frequency can decrease as the load goes lighter but it can also increase in case of a transient overload. Let us describe these modes:

1. In nominal load, the controller switches at its operating frequency, 65 kHz. The peak current setpoint varies depending on the feedback voltage but always remains safely clamped to 0.8 V over the sense resistance (or less if OPP is active). Assume the feedback voltage is above 1.9 V. If it decreases below this threshold, the internal clock turns into a variable frequency oscillator which value depends on the feedback voltage. As the frequency starts to decrease (the load is getting lighter), the peak current is still free to move. When the feedback voltage hits 1.5 V, the frequency is fixed to 26 kHz and will no longer vary if V_{FB} goes further down. The only variable to move now is the peak current setpoint. It can be adjusted by the feedback voltage down to 1 V. At this point, the current setpoint is frozen to 250 mV which corresponds to 31% of the maximum peak. Now both variables, frequency and peak current are frozen and the load current still goes down. The feedback voltage lowers until it touches the 400 mV threshold. At this moment, the part skips cycles and the feedback voltage ripples around 400 mV.
2. In high power, the feedback voltage is coming closer to the limit, e.g. 3.2 V for a 800 mV maximum setpoint (assume OPP is zero). In this zone, the frequency is still 65 kHz. When the power suddenly surges, the feedback voltage increases further. As it crosses the 3.2 V level, the peak current setpoint can no longer change. The frequency however is free and increases in an attempt to maintain V_{out}. The overload timer is started and counts down. If the feedback voltage returns to the normal area, e.g. a V_{FB} below 3.2 V, then timer is reset. If not, it continues to count and when the time is out, all pulses are stopped and an auto-recovery double hiccup mode takes place. If within the overload timer zone the feedback voltage continues its rise, the frequency increases until the feedback voltage reaches 4 V. At this point, the frequency has hit its upper limit of 130 kHz.
3. Should the load current still increase, all controller parameters being frozen, the output voltage collapses, bringing V_{FB} further up: the controller now considers a short circuit situation. At this moment, the low-frequency clock driving the fault timer is multiplied by 4, accelerating the counting and accordingly reducing the fault duration. When the timer elapses, the controller stops all pulses and enters double-hiccup mode.

Figure 13 shows the frequency evolution in relationship to the operating range.

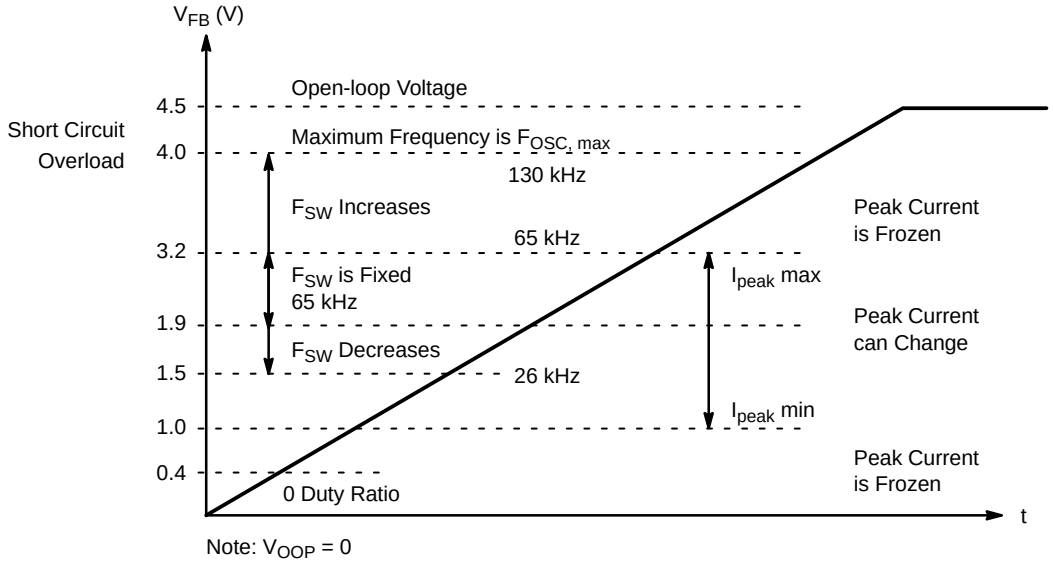


Figure 13. The Frequency is Reduced as the Feedback Pin Passes below 1.9 V
(When the Frequency Reaches 26 kHz and the Load Keeps Decreasing, the Part Enters Skip Cycle)

This value combined with a 26 kHz frequency guaranties the lowest acoustic noise in the transformer or in the RCD clamp network.

Shutting Down the Controller

Thanks to the presence of the skip-cycle comparator, it is easy to stop the controller. Just permanently pull the feedback pin below 400 mV and the switching pulses are stopped. Figure 14 shows that a simple transistor whose collector or drain is connected to the feedback pin is enough to stop the controller.

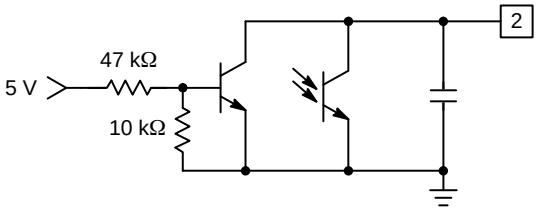


Figure 14. A Simple Transistor, Bipolar or a MOSFET, Can be Used to Stop the Controller

Pin 1 – The Combined OVP-OPP Pin

When used, this pin offers a means to a) reduce the maximum power the converter can deliver at high line b) latch the circuit off in case of stringent problem such as an Over Voltage Protection (OVP) event or an Over Temperature Protection (OTP) condition. Let's take a look at the first feature, the Over Power Protection (OPP) function.

Over Power Protection

The maximum power a flyback converter can deliver depends on several variables such as the switching frequency, the primary inductor and the maximum allowable primary peak current. Among these three variables, all of them are theoretically fixed and constant. Therefore, the power the converter can deliver at high input voltage should theoretically not differ from that delivered at the lowest input voltage. In reality, we know that both values differ and sometimes, in a large proportion. If we consider the primary inductor and the switching frequency independent from the input voltage, the final peak current seen by the inductor actually depends on the input voltage. Why? Because when the internal current-sense comparator detects an over-current condition, it takes time for this information to propagate inside the controller and eventually, bring the MOSFET gate down. The time needed is called the propagation delay. Most of the data-sheets, including the NCP1255, give you the propagation delay inherent to the controller, alone, when loaded by a 1 nF capacitor. In reality, depending on the drive current capability, the various resistors in series with the gate and the MOSFET gate-charge, it can be significantly longer. Figure 15 shows the resulting signals at low and high line levels. Depending on the propagation delay, the difference in current can be quite significant, impacting the maximum power at high line:

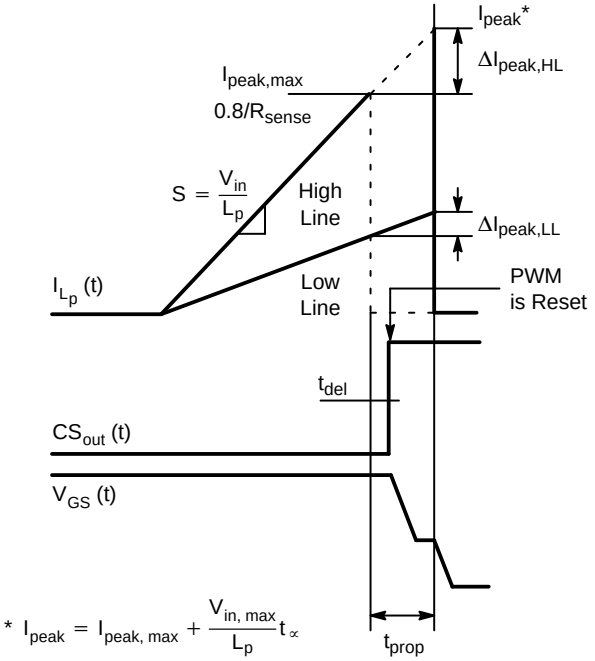


Figure 15. The Propagation Delay Affects the Final Peak Current Value at High Line

$$I_{peak,\,max} = \frac{V_{sense}}{R_{sense}} + \frac{V_{in}}{L_p}\,t_{\propto} \qquad \text{(eq. 22)}$$

The peak current runaway at high line is only partially responsible for the power increase in this operating condition. The second culprit is the transition from Continuous Conduction Mode (CCM) to Discontinuous Conduction Mode (DCM). This phenomenon happens because the on time naturally reduces at high line and offers more off-time to demagnetize the primary inductor (the inductor downslope is constant). This is what Figure 16 shows you. In this picture, we can see that the valley current tends to decrease as the input voltage goes up. The power transmitted by a flyback converter operating in CCM obeys the following formula:

$$P_{out} = \frac{1}{2} L_p \left(I_{peak}^{\,2} - I_{valley}^{\,2}\right) F_{SW}\,\eta \qquad \text{(eq. 23)}$$

where:

L_p is the primary inductor

I_{peak} is the inductor peak current

I_{valley} is the inductor valley current

F_{sw} is the switching frequency

η is the converter efficiency

Since we deal with a peak current controller, in fault condition at high line, the maximum peak current will slightly increase compared to that obtained at low line. What actually matters in (eq. 23) is the reduction of I_{valley} inherent to a longer off time. By manipulating a few equations, it is possible to calculate the valley current at high line and thus compute the power generated in this condition:

$$I_{valley,\,HL} = I_{peak,\,max,\,HL} - \frac{T_{SW}\,V_{in,\,HL}\left(V_f + V_{out}\right)}{L_p\left(V_f + V_{out} + N V_{in,\,HL}\right)} \qquad \text{(eq. 24)}$$

where:

T_{SW} is the switching period (15 μs or 65 kHz)

V_f is the secondary diode forward drop at the maximum output current (0.5 V)

V_{out} is the converter output voltage (19 V)

L_p is the primary inductor (600 μH)

N is the transformer turns ratio N_s/N_p (0.25)

t_{prop} is the total measured propagation delay (350 ns)

$V_{in,\,HL}$ = 370 V

$V_{in,\,LL}$ = 120 V

R_{sense} is the sense resistor (0.33 Ω)

$I_{peak,\,max,\,HL}$ is the maximum peak current obtained for $V_{in} = V_{in,\,HL}$ in (eq. 22): 2.64 A

$I_{peak,\,max,\,LL}$ is the maximum peak current obtained for $V_{in} = V_{in,\,LL}$ in (eq. 22): 2.49 A

$$I_{valley,\,LL} = 1.28\ A \qquad \text{(eq. 25)}$$

$$I_{valley,\,HL} = 0.99\ A \qquad \text{(eq. 26)}$$

Based on these two numbers, we can now compute the maximum power delivered by the converter at low and high line levels:

$$P_{max,\,LL} = \frac{1}{2} L_p \left(I_{peak,\,max,\,LL}^{\,2} - I_{valley,\,LL}^{\,2}\right) F_{SW}\,\eta_{LL} \approx \qquad \text{(eq. 27)}$$
$$\approx 76\ W$$

$$P_{max,\,HL} = \frac{1}{2} L_p \left(I_{peak,\,max,\,HL}^{\,2} - I_{valley,\,HL}^{\,2}\right) F_{SW}\,\eta_{HL} \approx \qquad \text{(eq. 28)}$$
$$\approx 104\ W$$

In this equation, we considered the low-line efficiency η_{LL} at 85% whereas it increased to 89% in high-line conditions. The power growth at high line reaches 37% compared to that at low line. In terms of currents, for a 19 V output, the maximum low-line current is 4 A and can go up to 5.5 A at the maximum input voltage. In our example, as we target a 60 W adapter (I_{out} = 3.2 A), the current computed by (eq. 28) is way too high and a means has to be found to reduce it.

There are several available techniques such as developing an offset on the current-sense pin in relationship to the input voltage. Unfortunately, this technique is dissipative and affects the standby power or the efficiency in light load conditions. The best is to directly play on the maximum peak current limit based on the bulk voltage level without sensing it directly to avoid power dissipation.

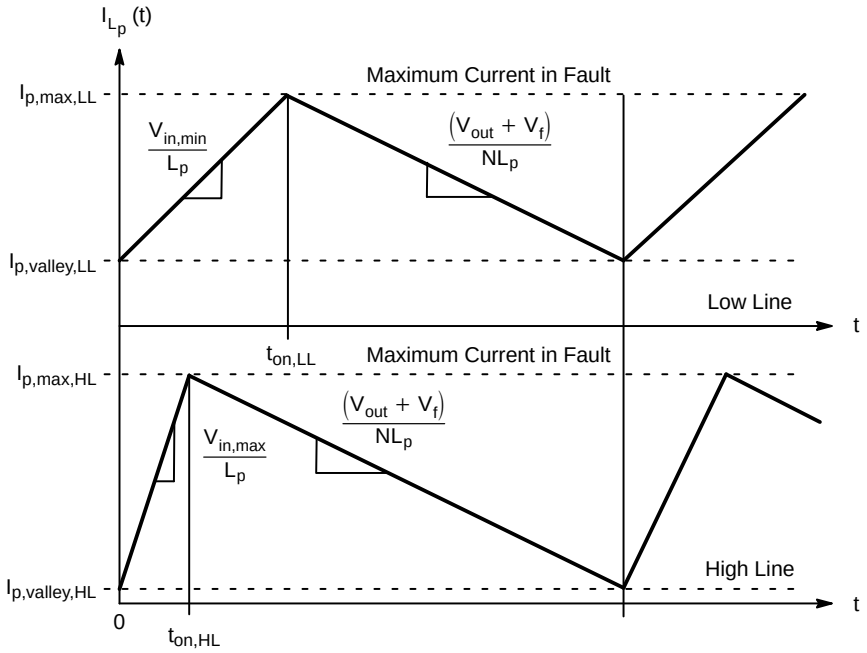


Figure 16. As the On-time Reduces at High Line, the Off-time Expands and Lets the Valley Current Go Down, Making the Operating Mode Closer to DCM: the Released Energy Cycle-by-cycle Increases

With the NCP1255, at low line and without any compensation, the maximum voltage across the current sense pin is limited to 0.8 V. To lower this signal at high line, a possible solution is to sum-up the 0.8 V reference voltage with a negative voltage proportional to the input voltage. This signal fortunately exists at no dissipation cost on the auxiliary winding, before the V_{CC} rectifying diode. It swings to $-N_{pa}V_{in}$ during the transistor on-time where N_{pa} is the turns ratio between the primary side of the transformer and the auxiliary winding. If we internally add a portion of this $-N_{pa}V_{in}$ level to the 0.8 V reference, we have a maximum peak current limit decreasing as the bulk voltage goes up. The implementation of this proprietary idea is described in Figure 17. As the auxiliary winding can be the seat of spurious oscillations at turn on, a small 300 ns blanking is performed on the signal to avoid false trigger of the downstream circuitry.

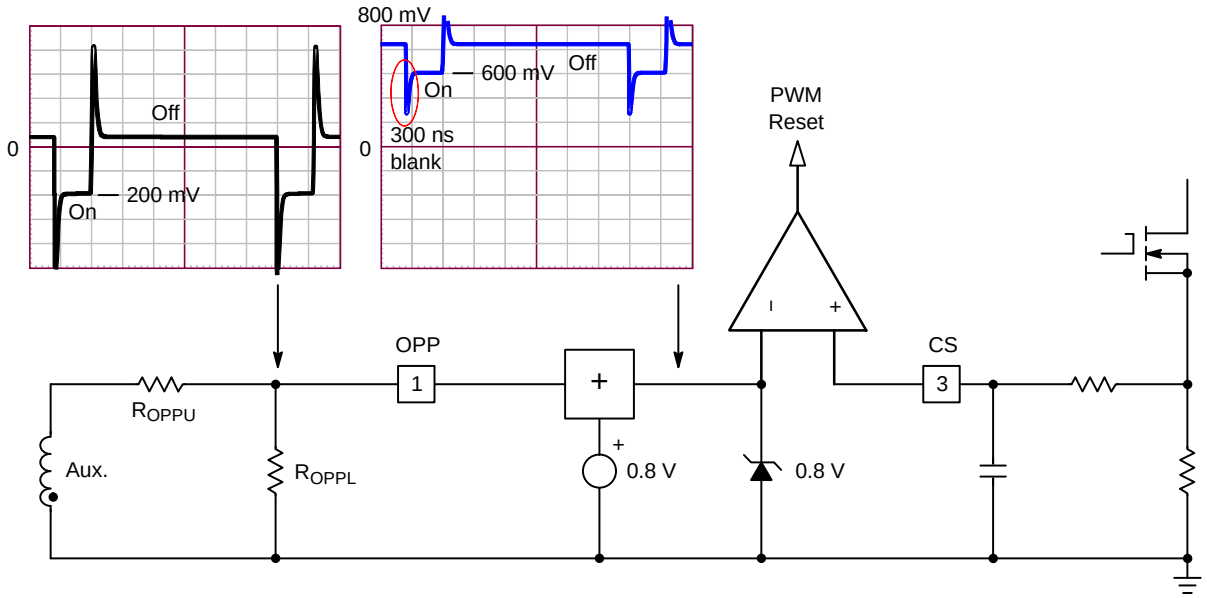


Figure 17. A Portion of the Auxiliary Voltage is Brought to the OPP Pin and Directly Subtracts from the 0.8 V Internal Reference Voltage
(Here, the 0.8 V Reference Level is Decreased by 200 mV)

The calculation of the resistances tapping the auxiliary voltage is easy. First, you need to know the exact amount of the required OPP level by extracting the peak current at high line producing the same output power as in low line operation. This is done by equating (eq. 27) and (eq. 28) then subtracting the propagation delay contribution. You obtain:

$$I_{peak,max,HL} = \frac{F_{SW} L_p \eta_{HL} \Delta I_{L_p,HL}^{\ 2} + 2P_{max,LL}}{2\eta_{HL} F_{SW} L_p \Delta I_{L_p,HL}} - \frac{V_{in,HL}}{L_p} t_{\propto} = \\ = 1.93\ A \quad \text{(eq. 29)}$$

In this equation, the term $\Delta I_{lp,HL}$ represents the inductor ripple at high line and is computed as:

$$\Delta I_{p,HL} = \frac{T_{SW} V_{in,HL}\left(V_f + V_{out}\right)}{L_p\left(V_f + V_{out} + NV_{in,HL}\right)} \quad \text{(eq. 30)}$$

Having in this example a sense resistor of 0.33 Ω, we produce a peak current of 0.8/0.33 = 2.42 A. To make this number go down to 1.9 A, we need to decrease the value of the reference voltage by:

$$V_{OPP} = I_{peak,max,HL} \times R_{sense} - V_{ref} = \\ = 1.93 \times 0.33 - 0.8 \approx -160\ mV \quad \text{(eq. 31)}$$

We found that a negative voltage of ≈160 mV will do the job. On our prototype biased at 370 V, given a turns ratio between the primary and the auxiliary windings of 0.18, the auxiliary winding swings to:

$$-N_{pa} V_{in,max} = -18 \times 370 = -66.6\ V \quad \text{(eq. 32)}$$

To create the −160 mV level on pin 1, we can fix the pull-down resistor R_{OPPL} to 1 kΩ. Such low value guarantees a good noise immunity and low leakage from the pin. However, values up to 3 kΩ are acceptable if a clean and adequate PCB routing is adopted. When biased at 160 mV, R_{OPPL} will see a current of:

$$I_{R_{OPPL}} = \frac{160\ m}{1\ k} = 160\ \mu A \quad \text{(eq. 33)}$$

The upper resistor R_{OPPU} can then be computed as:

$$R_{OPPU} = \frac{66.6 - 160\ m}{160\ \mu} = 415\ k\Omega \quad \text{(eq. 34)}$$

This analytical method gives you a way to compute the resistive network for the OPP function. Nothing prevents you, however, from replacing R_{OPPU} by a 1 MΩ potentiometer and starting from its maximum value, slowly decreasing its value to force the protection to trip when the power supply exceeds the maximum current you accept at the highest line level.

Please note that the internal 0.8 V clamp prevents the maximum current sense level to be affected by an excessive positive bias accidentally applied on the OPP pin. For instance, should you apply 1 V on the OPP pin, the maximum peak current voltage excursion on the sense resistor will still safely be clamped at 0.8 V.

Over Voltage Protection

On top of the OPP function, pin 1 welcomes another circuitry dedicated to the latch of the device. If the OPP requires a negative signal during the on time, the OVP will sense a positive signal on pin 1 reaching 3 V. Therefore, when both OVP and OPP are combined on pin 1, the positive signal for the OVP must not bother the OPP operation. A simple network combining a Zener diode in series with another diode is presented in Figure 18. When the auxiliary signal is negative, D1 is blocked despite the forward bias of D_Z: the OPP network made of R_{OPPU} and R_{OPPL} can do its compensation job.

When the power MOSFET turns off, the auxiliary winding jumps to the output voltage, reflected accordingly to the turns ratio between the power winding and the auxiliary winding. When this voltage exceeds the Zener voltage value, the voltage on pin 1 starts to rise cycle-by-cycle. However, thanks to the presence of D_1 and D_Z, the signal amplitude increases during the off-time only and the OPP signal is kept intact. When the level on pin 1 reaches 3 V, the controller latches off. A full latch is often necessary in critical situations, for instance when the optocoupler is broken or when the temperature in the adapter exceeds a safe level.

A latch circuitry can sometimes create troubles if made too sensitive to external perturbations for instance. For this reasons, the NCP1255 hosts an architecture combining blanking signals with a counter by 4. The simplified internal circuitry appears in Figure 18. The principle is to count 4 successive OVP events to latch off the controller. If the counter was advanced by 2 only (i.e. because of noise) and the 2 remaining OVP are ignored, the next clock cycle will reset the counter. Let's have a look on how it works. When the drive output goes down, at the end of the on-time, a pulse sets the latch on the right-side of the picture: Q is "1" and $\overline{Q}$ is "0". If Q is high and stays high in the absence of an OVP event, it naturally resets the counter on the next clock pulse. If prior to this reset the OVP comparator senses a voltage on the OPP pin greater than 3 V, it toggles in the high state. Its level propagates through the 600 ns time constant and passes the AND gate provided it lasts longer than the 1 µs blanking time, started after the DRV pin is down. It resets the latch, making its output Q down while $\overline{Q}$ toggles to "1": the pulse is passed to the clock counter that increments by 1. When 4 events are validated, the counter output n°4 goes high and latches the controller. When this occurs, all driving pulses are stopped and the V_{CC} pin is vigorously pulled down to around 7 V by an internal SCR. Reset occurs when the user cycles the V_{CC} down, e.g. by unplugging the converter from the wall outlet.

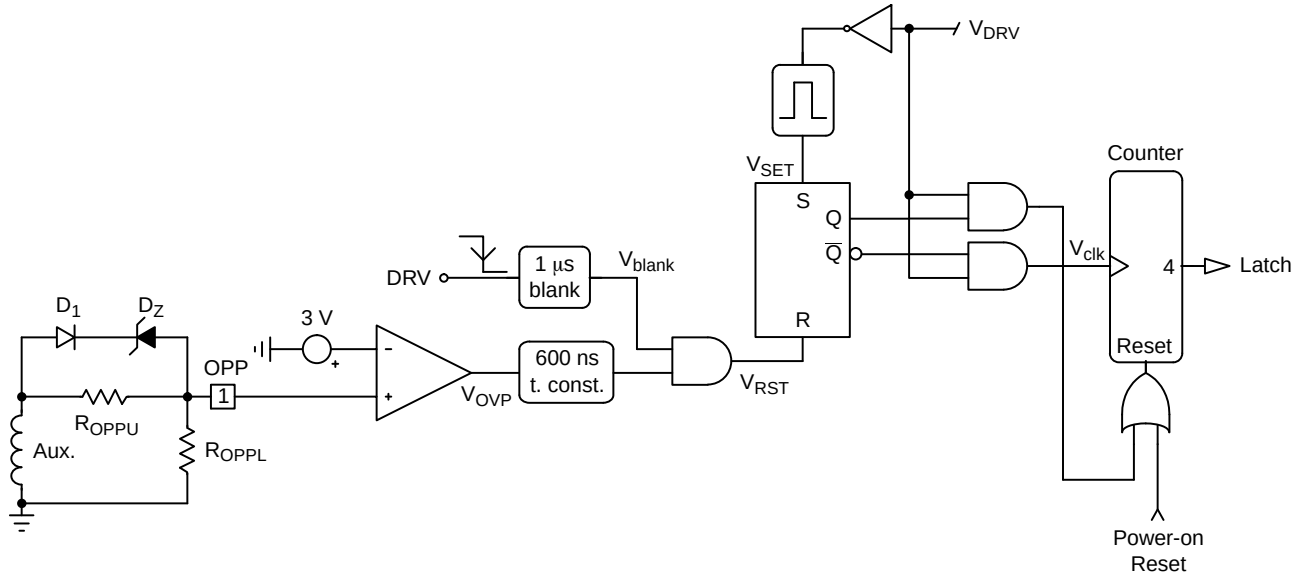


Figure 18. The Internal Circuitry Hosts a Divide-by-4 Counter that Helps Avoiding False Tripping

Filtering the Leakage Inductance Spikes

The auxiliary voltage is made of sharp transitions when swinging from $-N_{pa}V_{in}$ to $N_{sa}\,(V_{out} + V_f)$ where N_{sa} represents the turns ratio between the secondary side and the auxiliary winding. These sharp discontinuities could couple to the OPP pin when a Zener diode is installed. This is because the diode features a parasitic junction capacitance that can propagate spurious spikes to the OPP pin. Despite a comfortable safety margin associated with a blanking circuitry, we recommend the addition of a simple RC network connected as what Figure 20 suggests. The values indicated on the sketch have been tested successfully. If necessary, a small capacitor of 10−22 pF can also be installed directly between pin 1 and pin 4 (GND), wired very close to the controller.

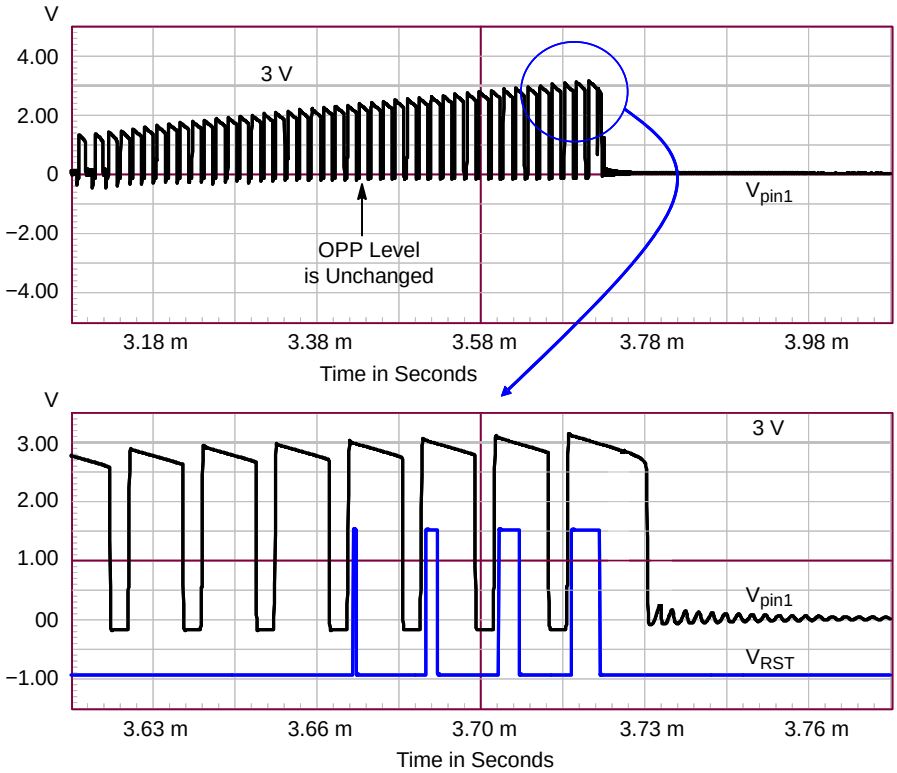


Figure 19. Simulation Results of an OVP Event Sensed by the NCP1255
(Please Note that the OPP Level is Unchanged Despite the Positive Growth of the Auxiliary Signal)

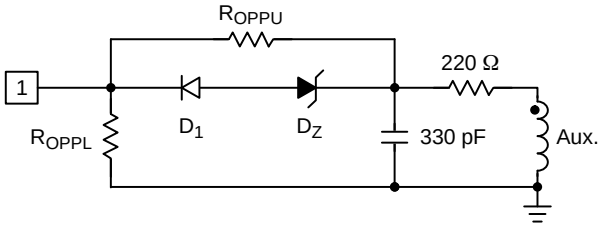


Figure 20. A Simple RC Filter Helps to Soften the Transitions before Reaching the Zener Diode

As a final comment on this OPP pin, we recommend to maintain a low impedance from pin 1 to ground, i.e. adopt a low value for the pull-down resistor R_{OPPL}. Values around or below 3 kΩ are recommended, 1 kΩ being a good choice.

Latching the Controller from the Secondary Side

There are some cases where the observation of the auxiliary V_{CC} does not deliver the required precision. In this case, it is possible to monitor the secondary side output voltage and bring the information on the primary side via an optocoupler. However, the signal must be carried on pin 1 accounting for the presence of the OPP circuit which needs negative voltage. A resistor R_{opto} installed in series with the optocoupler collector limits the injected current in pin 1 when the OVP event occurs. The resistor must be sized to roughly limit the peak current in the internal ESD Zener (10 V breakdown) below 10 mA.

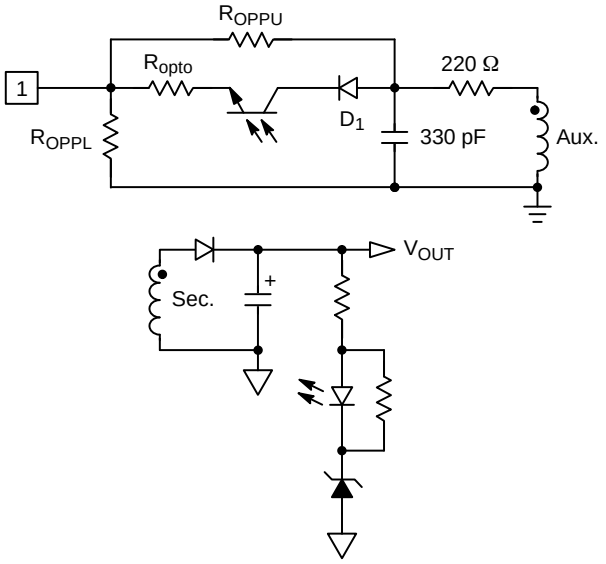


Figure 21. When the Optocoupler Conducts, it Positively Biases Pin 3 over 3 V during the Off-time Period

Over Temperature Protection

Over Temperature Protection (OTP) is a means to stop the adapter in case the ambient temperature exceeds a certain level. By adding a Negative Temperature Coefficient (NTC) resistor over the Zener diode, you have the possibility to trigger the latch when the temperature is too high. The proposed configuration appears in Figure 22.

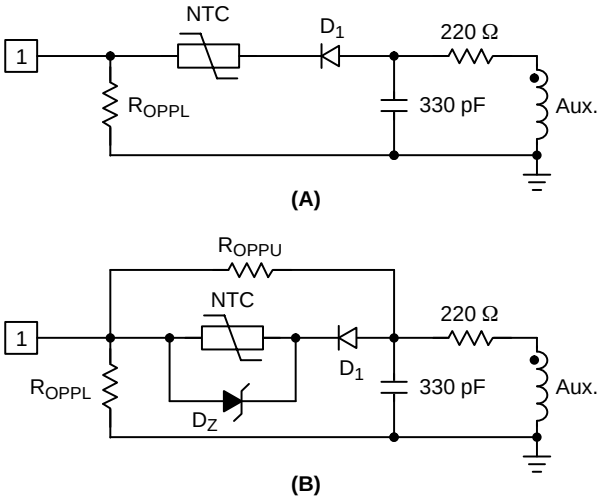


Figure 22. A NTC Resistor is Placed across the Zener Diode and Offers a Way to Shut Down the Adapter when the Ambient Temperature Runs Away

In the left side of the picture, labeled “A”, the OTP is considered alone whereas it is coupled with the OVP on the right side (label “B”). The calculation is rather simple depending on the selected NTC device. What matters is the resistance at the temperature trip point. Let’s assume the selected NTC offers a resistance R_{110} of 8.8 kΩ at T_A = 110°C and the OTP solution alone is considered (Figure 22, A). If we consider a 3 V trip point on the OPP pin derived from a 14 V auxiliary level plateau, then the pull-down resistor R_{OPPL} must be calculated as follows:

$$R_{OPPL} = \frac{V_{latch}\, R_{110}}{(V_{aux} - V_f) - V_{latch}} = \frac{3 \times 8.8\,k}{(14 - 0.6) - 3} \approx 2.5\,k\Omega \quad \text{(eq. 35)}$$

Where V_f represents the voltage drop from the series diode D_1. This diode ensures a positive bias only during the off-time to avoid bothering the OPP circuitry. When the temperature will increase, the voltage will also slowly grow on pin 1 (during the off-time only) until 3 V are reached. At this point, the controller stops all operations and goes into a latched mode. Reset occurs when the user cycles the power off and on.

When combined with the OPP, the calculation must include the requirement of negatively biasing pin 1 during the on-time. Let’s use the same NTC resistance as in the above example. The pull-down resistor value does not change and is still 2.5 kΩ as given in (eq. 35) Now that the pull-down OPP resistor is known, we can calculate the upper resistor value R_{OPPU} to adjust the power limit at the chosen output power level. Suppose the OPP requirement dictates a 200 mV decrease from the 0.8 V set point. In our application, as the on-time swing on the auxiliary anode at high line is −67.5 V, we need to drop over R_{OPPU} a voltage of:

$$V_{R_{OPPU}} = N_{pa}\, V_{in} - V_{OPP} = 67.5 - 0.2 = 67.3\,V \quad \text{(eq. 36)}$$

The current circulating in the pull down resistor R_{OPPL} in a 200 mV bias will be:

$$I_{R_{OPPL}} = \frac{200\,m}{2.5\,k} = 80\,\mu A \qquad \text{(eq. 37)}$$

The R_{OPPU} value is therefore easily derived:

$$R_{OPPU} = \frac{V_{R_{OPPU}}}{I_{R_{OPPL}}} = \frac{67.3}{80\,\mu} = 841\,k\Omega \qquad \text{(eq. 38)}$$

Experiments carried on an adapter combining both OPP, OVP and OTP have shown very precise trip points in both situations, over voltage and over temperature.

Pin 8 – The Timer Pin

The fault timer lets the user set the maximum duration of a fault event such as an overload or a short circuit. Both durations are linked by a ratio of 4: if the overload timer is set to 100 ms then the short circuit duration cannot exceed 25 ms. Please note that during the start-up sequence, where the feedback loop is open, the controller naturally senses a short circuit. The corresponding timer must thus be long enough to let the converter properly start up.

Figure 23 depicts the simplified internals of the timer circuitry. The timer duration is affected, on the fly, by the feedback voltage. When the feedback voltage is below 4 V, the internal capacitor is charged with a current I. If a short circuit suddenly occurs, this current becomes 4I, accelerating the capacitor charge and reducing the low-frequency clock period: the timer counts at a faster pace. The duration is adjusted by pulling pin 8 to ground via a resistor. This resistor sets a reference current inside the chip and lets you adjust the duration you need. Figure 24 links the resistor value to the timer length.

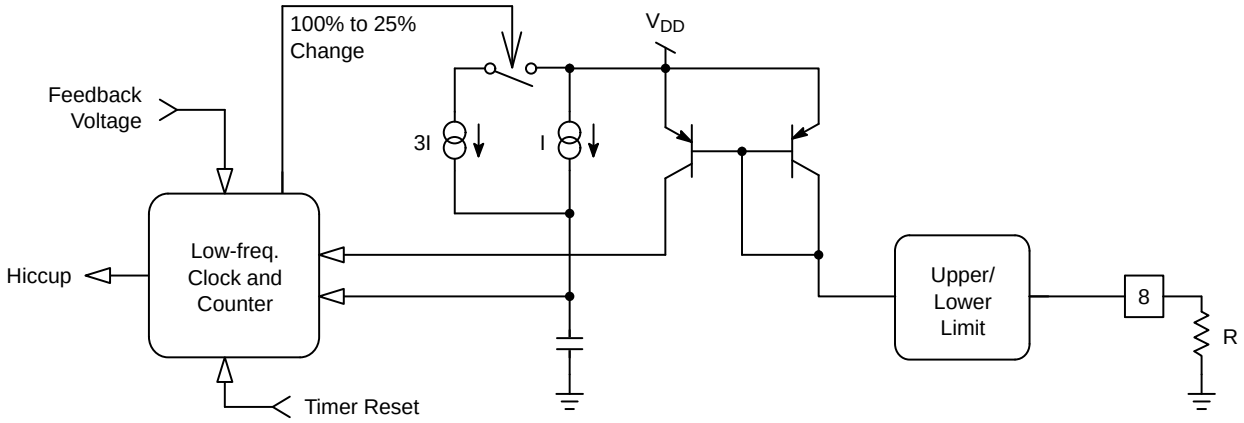


Figure 23. This Simplified Circuitry Shows the Protection against Short/Open Test Implemented in the NCP1255

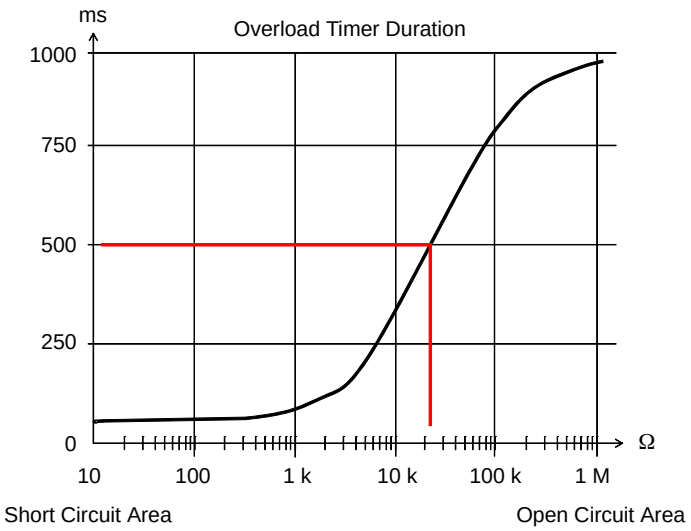


Figure 24. A 22 kΩ Resistor Connected to Pin 8 Sets the Timer Duration to a Typical Value of 500 ms in Overload
(125 ms in Short Circuit)

We have captured a start-up event while the converter output was in an over power situation (almost a short circuit but V_{out} is not 0 V). The auxiliary voltage builds up with difficulty and maintains a sufficient V_{CC} level. During this time, the controller senses a short circuit and as the timer is set to 500 ms in overload mode, it reduces this value around 120 ms. When the timer has elapsed, all pulses are stopped and the part enters auto recovery.

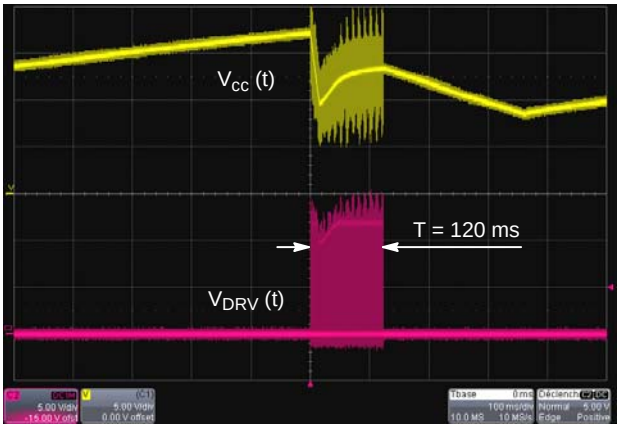
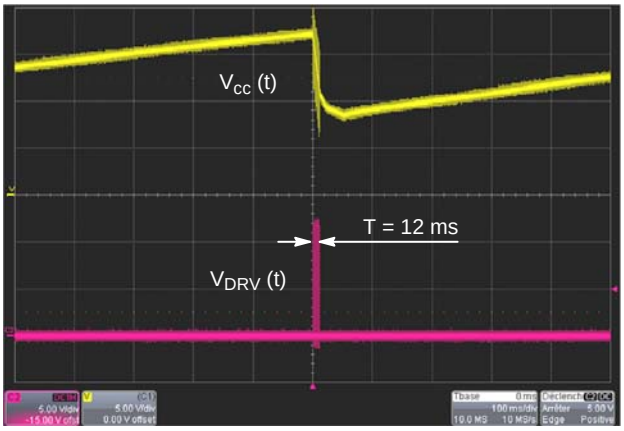


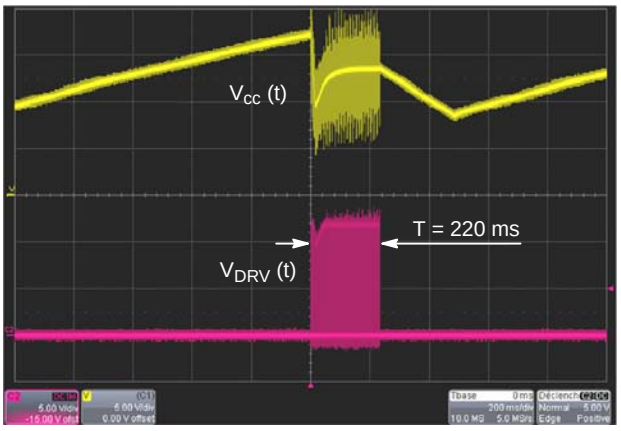
Figure 25. In an Over Power Situation, the Auxiliary Voltage Does Not Collapse and Gives Enough Time to Let the Timer Elapse

(Here, with a 22 kΩ Resistor on Pin 8, the Duration is 120 ms)

In case of the timer pin shorted to ground or if the pin is left floating, the timer enters a pre-determined mode. In case of short circuit, the overload duration is fixed to 50 ms while it is set to 1 s in case of open-pin condition. Figure 26 illustrates this behavior in a given converter.



(A)



(B)

Figure 26. The Timer is Always in a Known State even if its Pin Gets Shorted to Ground (A) or Left Floating (B) During Safety Tests

Pin 7 – Brown Out Protection

A brown out input protects the converter in presence of a low input voltage, for instance during a transient network fall out. Without this protection, the converter would be pushed to its maximum power with destruction risks. It could enter a protective hiccup mode delivering at this moment an output voltage swinging up and down. Some loads, such as printers, do not accept hiccup conditions: a clean cutoff is necessary in case the converter cannot maintain V_{out} within acceptable limits. When the mains returns to a normal level, the converter must resume operations automatically.

Figure 27 shows a simplified implementation in the controller.

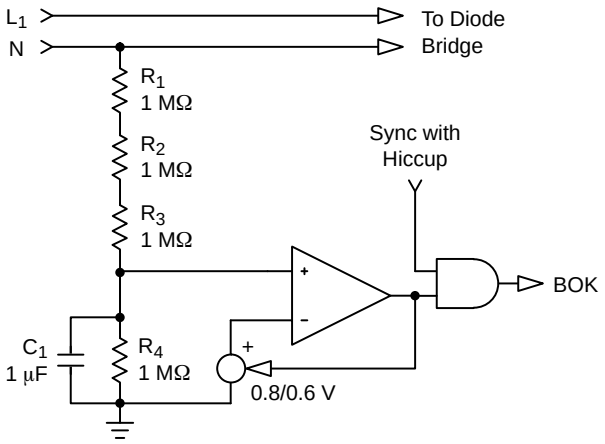


Figure 27. A Simple Comparator Monitors the Input Voltage via a Single Pin

(When this Voltage is too Low, the Pulses are Stopped and the V_{CC} Hiccups)

To ensure a clean re-start, the BO information is only validated when V_{CC} reaches VCC_{ON}. This ensures a fully-charged V_{CC} capacitor when the controller pulses again. An asynchronous BO-related re-start could induce aborted start-up sequences if the V_{CC} capacitor would too close to the UVLO threshold. This behavior is confirmed by the waveforms appearing in Figure 28.

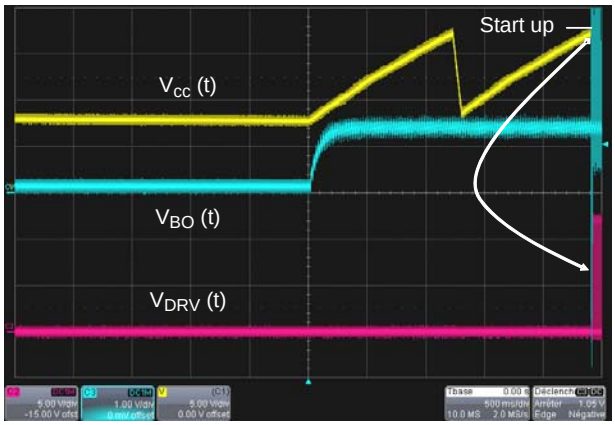


Figure 28. The Restart, when Leaving a Brown-out Situation, is always Synchronized to the Start-up Level, Ensuring a Clean Sequence

From the given schematic, the calculation of the resistor is straightforward. We have connected the resistor to the input line and thus observe a single-wave signal peaking to $V_{in,peak}$. The average voltage seen on top of R_1 is thus:

$$V_{in,\,avg} = \frac{V_{in,\,peak}}{\pi} \qquad \text{(eq. 39)}$$

Then, pick a bridge current compatible with the power consumption you can accept. If we chose 10 μA, the pull-down resistor R_4 calculation is straightforward:

$$R_4 = \frac{V_{BOon}}{I_{bridge}} = \frac{0.8}{10\,\mu} = 80\,k\Omega \qquad \text{(eq. 40)}$$

Now suppose we want a typical turn-on voltage $V_{turn\text{-}on}$ of 78 V rms. From the two above equations, we can calculate the value of the upper resistive string:

$$R_{upper} = \frac{\left(\frac{V_{turn-on}\sqrt{2}}{\pi}\right) - V_{BOon}}{I_{bridge}} = \qquad \text{(eq. 41)}$$

$$= \frac{\frac{78\times 1.414}{3.14} - 0.8}{10\,\mu} = 3.4\,M\Omega$$

The hysteresis on the internal reference source is 200 mV typically. The ratio of the two voltages is 1.33. With the upper resistive network, the turn-off voltage can then easily be derived:

$$V_{turn-off} = \frac{V_{turn-on}}{1.33} = \frac{78}{1.33} \approx 59\ V\ rms \qquad \text{(eq. 42)}$$

A 1 μF capacitor is necessary to filter out the input ripple. Reducing its value, hence allowing more ripple, can help to fine tune the hysteresis, if necessary.

When the controller senses a BO event, all pulses are immediately cut. An internal pull-down source (typically 1 mA) is activated and brings V_{CC} down towards UVLO. When this level is reached, the controller goes back into low-consumption mode and lifts V_{CC} up again. At VCC_{ON}, a check on the BO comparator is made: if the input level is correct, the part re-starts, if still too low, the 1 mA source brings V_{CC} down again. As a result, V_{CC} operates in hiccup mode during a BO event.

Conclusion

This application note shows the peak power capability offered by the NCP1255. Its frequency excursion offers a nice means of transiently increasing the power capability without affecting the transformer as the peak current remains constant. Packed with a wealth of features, this SOIC package will let you build safe and rugged power converters with a limited count of surrounding components.

References

[1] C. Basso, “Switch Mode Power Supplies: SPICE Simulations and Practical Designs”, McGraw-Hill, 2008

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