# AND9207/D

# The NCP1256, a Tiny Controller for Offline Converters

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APPLICATION NOTE

Despite its small size, the NCP1256 packs a lot of goodies not even found in higher-end controllers. Capitalizing on the NCP1250 popularity, the 1256 now includes a brown-out circuit which shields the power supply against erratic behaviors when the input line dangerously drops. The overpower protection is implemented in a non-dissipative way and helps harnessing the maximum output power along the input voltage range. Various protections are included in the part such as the possibility to implement over temperature protection (OTP) or over voltage protection (OVP) in really simple ways. Capitalizing on all these points, the part is a candidate of choice when designing ac-dc adapters for notebook, tablets and other applications in which combining high performance and cost efficiency is an absolute necessity.

### General Description

The part is encapsulated in a TSOP−6 package, very close in dimensions to the SOT−23 6-lead type. Featuring a low-power BiCMOS process, the die accepts $V_{cc}$ levels up to 28 V, safely clamping the drive voltage below 12 V. With its 10-μA maximum start-up current (guaranteed from −40°C to 125°C), a high-value resistive network can be used in offline applications to crank the converter, naturally minimizing the wasted power in high-line conditions. In nominal load operations, the switching frequency of this peak-current mode control circuit is either 65 kHz or 100 kHz depending on the selected version. In light-load operations, the part quickly reduces its switching frequency down to 26 kHz and enters skip cycle as the load consumption goes further down in power. This mode of operation favors a high efficiency from high to moderate output power levels and ensures the lowest acoustic noise in the transformer when light-load mode is entered. To improve the EMI signature, a low-frequency modulation brings some dither to the switching pattern. Unlike other circuits, the dither is kept in foldback mode and still smoothes the noise signature. The feedback is simply made by pulling down the dedicated pin via an optocoupler, driven from the secondary side by a TL431 or a simple Zener diode. A brown-out circuitry prevents power supply operations from too low an input voltage. The controller permanently monitors the scaled-down input voltage image and uses that image to build over power protection (OPP) by sourcing current out of the CS pin. Figure 1 shows the NCP1256 in a typical implementation for a 12-V converter.



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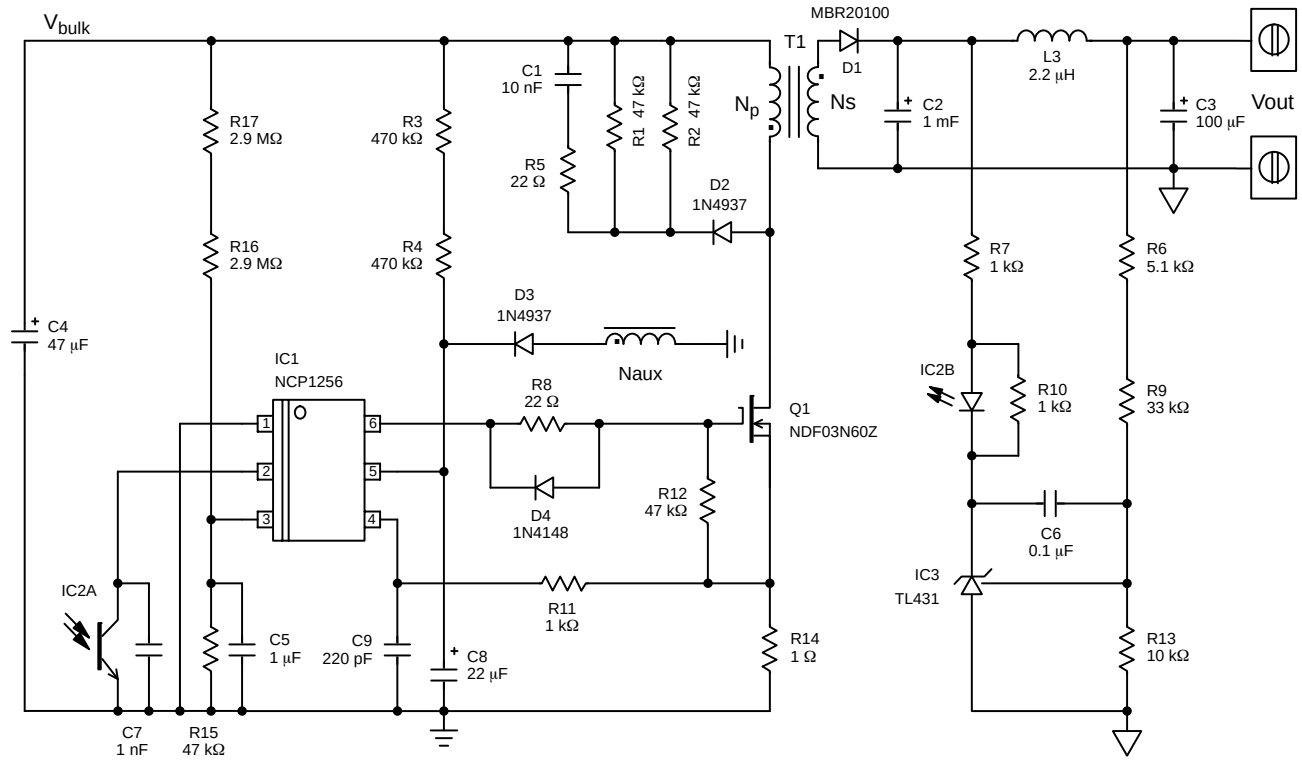



**Figure 1. The Simplest Implementation of the NCP1256 in an Isolated Flyback Converter**

### Pin 5 − The $V_{CC}$ Supply

The chip supply is brought in via pin 5. Upon start-up, for a voltage less than 18 V (typical), the internal consumption is limited to 10 µA maximum across the temperature range. It suddenly changes to around 1.5 mA as the controller starts switching at 65 kHz on a 1-nF capacitive load. The auxiliary $V_{cc}$ voltage can go down to around 9 V before the controller safely stops the switching pulses.

The classical configuration to start-up the controller appears in Figure 2. We can see a start-up resistor, $R_1$, connected to the bulk voltage. It generates a current $I_1$. Part of this current, 10 µA, is diverted inside the chip. This current is fairly constant until $V_{cc}$ equals 18 V. The current flowing inside the $V_{cc}$ capacitor is thus:

$$I_2 = I_1 - I_{CC1} \qquad \text{(eq. 1)}$$

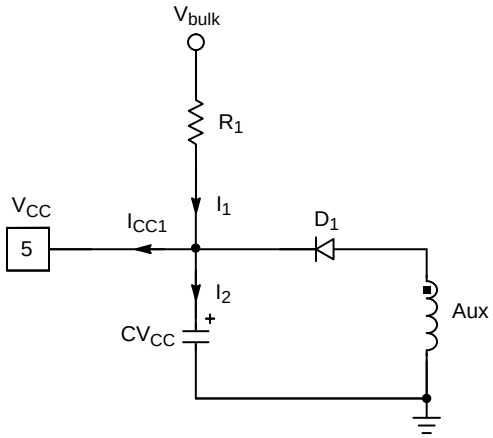



**Figure 2. A Simple Resistive String Brings the Necessary Current to Charge $CV_{CC}$**

When the controller starts switching (i.e. $V_{cc}$ is 18 V), the current consumption suddenly increases. The consumption budget is linked to the controller own absorption but also to the MOSFET gate charge $Q_G$. As $I_1$ is kept small to minimize the power wasted in $R_1$ at high line, all the current is now delivered by the $V_{cc}$ capacitor. This element remains alone to power the controller and the voltage across its terminals falls out. Before the voltage on pin 5 reaches the $VCC_{min}$ level, the auxiliary winding must be high enough to take over the controller supply via $D_1$. If the capacitor is too small, the voltage drops too quickly and the converter cannot start-up properly: pulses are stopped and the current consumption switches back to less than 10 μA for a new re-start. An auto-recovery hiccup mode takes place as shown in Figure 3. Please note the presence of a double hiccup which ensures the lowest average input current when the converter is in a fault mode. Here, a typical operation at low line with a total capacitance of 4.7 μF + 47 μF ensures a duty cycle in burst mode of less than 3% at both input line extremes.

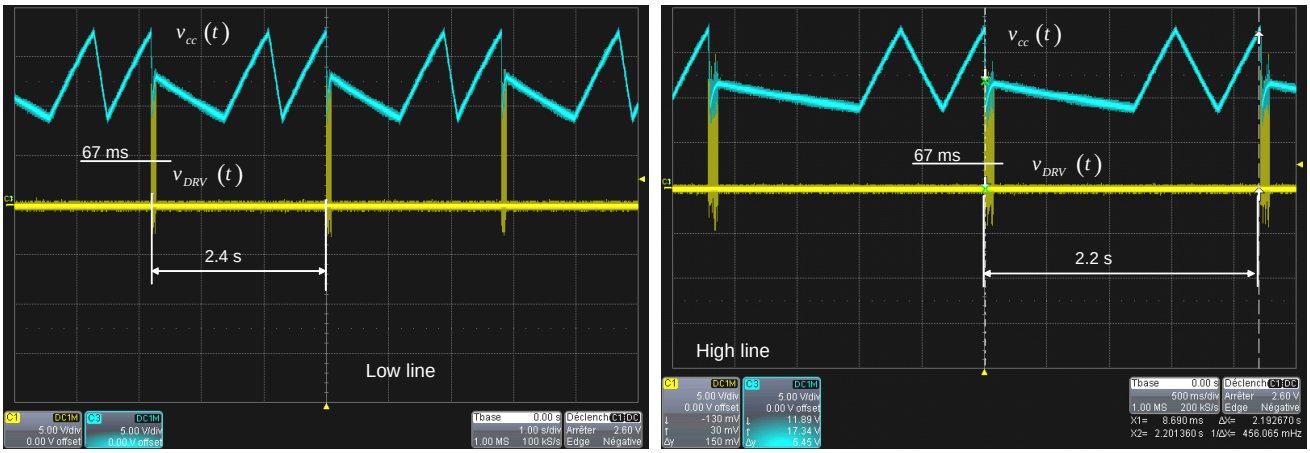



**Figure 3. The Part Enters an Auto-Recovery Double Hiccup Mode in Case the Auxiliary $V_{CC}$ is Missing**

Before calculating $R_1$, we have to know what capacitor value can maintain enough voltage on the $V_{cc}$ pin until the auxiliary winding takes over. The most difficult task in this calculation is to estimate the worst-case time at which the auxiliary voltage takes over. This worst case happens when the output power $P_{out}$ is maximal, the input voltage $V_{in}$ is minimal but comprehensive start-up tests also include high and low temperature. This parameter depends on several elements such as the maximum peak current, the soft-start duration, the output capacitance and so on. Based on our experience, a time-duration of 15 ms is a reasonable value to start with. Then, experiments on the prototype will either confirm the assumptions or will tell you to consider a different value. For the capacitor calculation, we have to check the minimum available voltage excursion across this energy-storing element from the specifications. Reading the NCP1256 data-sheet, we find that this occurs when both the start-up voltage and the $UVLO_{low}$ thresholds are at minimum:

$$\Delta V_{CC} = VCC_{(on),min} - VCC_{(min),min} = \\ = 16 - 8.3 = 7.7\ V \qquad \text{(eq. 2)}$$

If we consider a 15-ms time duration for the auxiliary voltage takeover and a total consumption current around 1.5 mA (let's assume a 3-A power MOSFET, the $V_{cc}$ capacitor must show a capacitance above the following value:

$$C_{V_{cc}} \geq \frac{ICC_3 t_2}{\Delta V_{CC}} \geq \frac{1.5\ m \cdot 15\ m}{7.7} \geq 3\ \mu F \qquad \text{(eq. 3)}$$

Given the manufacturing dispersions on this type of component, it is necessary to take design margins. Typically, a 4.7-μF capacitor will do well.

The above calculation solely focuses on the start-up sequence but does not consider standby power mode where the $V_{cc}$ level has to be maintained above the $VCC_{(min)}$ level. In this mode, and particularly with a NCP1256 featuring an extremely low consumption, the distance between switching pulses can be quite large as shown in Figure 4. A large ripple can affect the $V_{cc}$ line and its valley could trip the UVLO circuitry. To make sure $V_{cc}$ is maintained in light-load conditions, do not insert any resistor in series with $D_1$ in Figure 3 example. The smallest drop in refueling current ($Q = i \cdot t$) would degrade the $V_{cc}$ level in no-load situations. The best solution is adopting a split $V_{cc}$ configuration as shown in Figure 5. $C_1$ rectifies the auxiliary winding signal and can be of large value. As it is isolated from the $C_2$ by diode $D_2$, it has no impact on start-up time. However, keep in mind that this capacitor value affects the take over time $t_2$ in Equation 3.

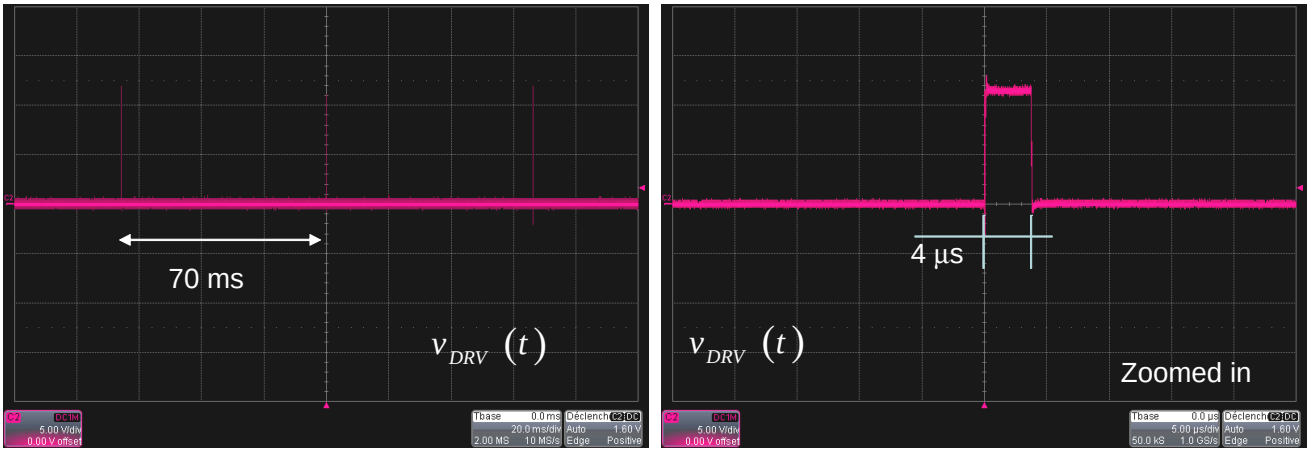



**Figure 4. In Skip Mode, the Distance between Two Pulses can be Quite Large and the $V_{CC}$ Capacitor Remains Alone to Supply the Controller between Two Switching Events**

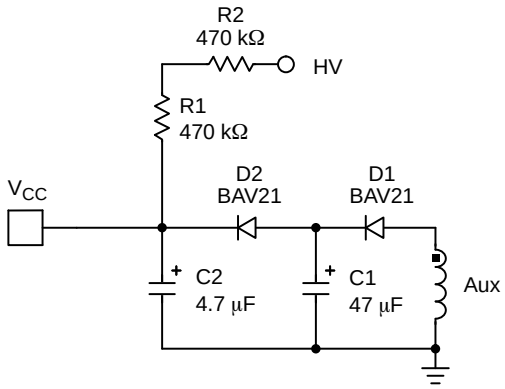



**Figure 5. A split $V_{CC}$ Configuration Does Not Hamper the Start-Up Time and Lets You Grow Capacitor $C_1$ to Keep $V_{CC}$ Alive in No-Load Operation**

When the configuration has been selected, whether it is a simple or split-$V_{cc}$ configuration, you have to test it on the bench in a worst-case configuration, meaning full load/low line and at operating temperature extremes. It is important to test across the operating temperature range because capacitance and Equivalent Series Resistances do vary at large and safe start up must be ensured in all conditions. Figure 6 shows a typical plot from the NCP1256 demonstration board shot at low line and full power.

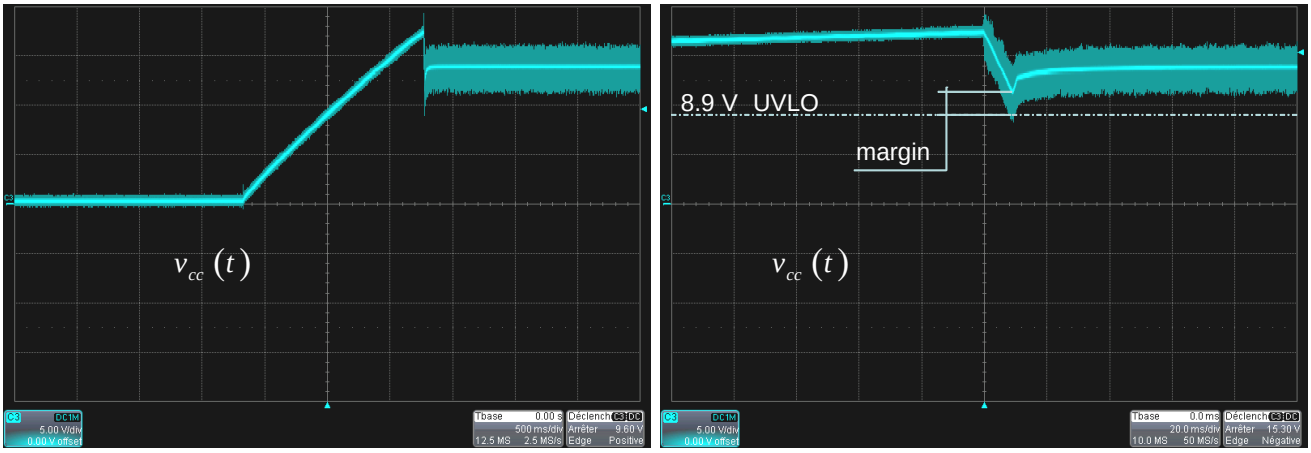



**Figure 6. A Start-Up Sequence at Maximum Output Power Shows Enough Margins on the $V_{CC}$ Capacitor Voltage**

The capacitor value being known, how much current do we need for $I_1$? If we adopt a 4.7-μF capacitor and need a start-up time less than 2.9 s at the lowest input voltage (85 V rms or 120 V rectified), what current needs to be injected into $C_{Vcc}$ to raise from 0 to $V_{CC(on),max}$?

$$I_1 \geq \frac{V_{CC(on),max} C_{V_{cc}}}{t_{startup}} \geq \frac{20 \cdot 4.7\,\mu}{2.9} \geq 32.4\ \mu A \quad \text{(eq. 4)}$$

These 32.4-μA, to which 10 μA must be added ($I_{CC1}$), i.e. 43 μA roughly, have to be delivered from the lowest input line. This is 120 V dc in a classical design intended to operate on a universal mains input (85−265 V rms). What resistor value must then be used to reach that value?

$$R_{startup} = \frac{V_{bulk,min} - V_{CC(on),max}}{I_1} = \frac{120 - 20}{43\,\mu} \approx 2.3\ M\Omega \quad \text{(eq. 5)}$$

Unfortunately, in high-line conditions (265 V rms), this resistor is permanently biased and dissipates power. If we neglect the $V_{cc}$ value, the dissipated power amounts to:

$$P_{R_{startup,hiline}} \approx \frac{V_{bulk,max}^2}{R_{startup}} = \frac{375^2}{2.3\ Meg} = 61\ mW \quad \text{(eq. 6)}$$

This extra power dissipation is not a big problem if you plan to boast a no-load standby power less than 300 mW. On the contrary, if you wish to comply with a standard asking less than 100 mW at high line, Equation 6 tells you that you will have to keep the dc-dc natural consumption below 30 mW to keep some margin. Depending on the adopted architecture, it may be difficult.

### Looking for a Half Cycle

Rather than connecting the start-up network to the dc rail, $V_{bulk}$, why not connecting it directly to the mains? As one bridge diode will remain in series with the return path, we benefit from a half-wave rectification, leading to a lower average value than on the bulk rail, hence lower power dissipation on the start-up resistor. This is what Figure 7 suggests.

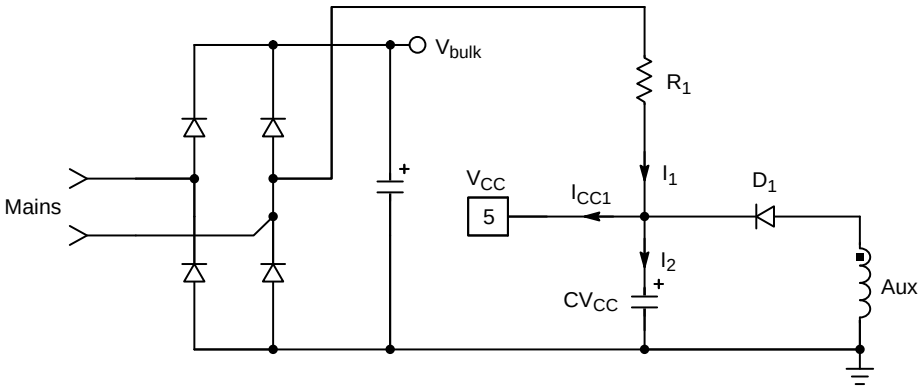



**Figure 7. The Direct Connection to the Mains Significantly Reduces the Wasted Power on the Start-Up Resistor**

Now, it is interesting to calculate the value of the resistor $R_1$ to keep exactly the same start-up current as in the case where we have the direct connection to the bulk capacitor. The calculation of $R_1$ leading to the same start-up time is approximate since a) the voltage on the capacitor grows cycle by cycle b) capacitive leaks are involved c) the simplified expression does not account for the 10-μA start-up current. However, considering perfect elements, the following formula gives a starting point:

$$R_1 = \frac{t_{start}}{C_{V_{cc}} \cdot \ln\left(\frac{V_{pLL}}{V_{pLL} - \pi V_{CC(on),max}}\right)} \quad \text{(eq. 7)}$$

Where $V_{pLL}$ is the lowest input line voltage at which you want the converter to start. Using values given in Equation 4, the start-up resistor in a half-wave configuration is evaluated to

$$R_1 = \frac{2.9}{4.7\,\mu \cdot \ln\left(\frac{120}{120 - \pi \cdot 20}\right)} = 832\ k\Omega \quad \text{(eq. 8)}$$

A quick simulation setup helps calibrate this resistor to 750 kΩ for a 2.9-s startup time at low line.

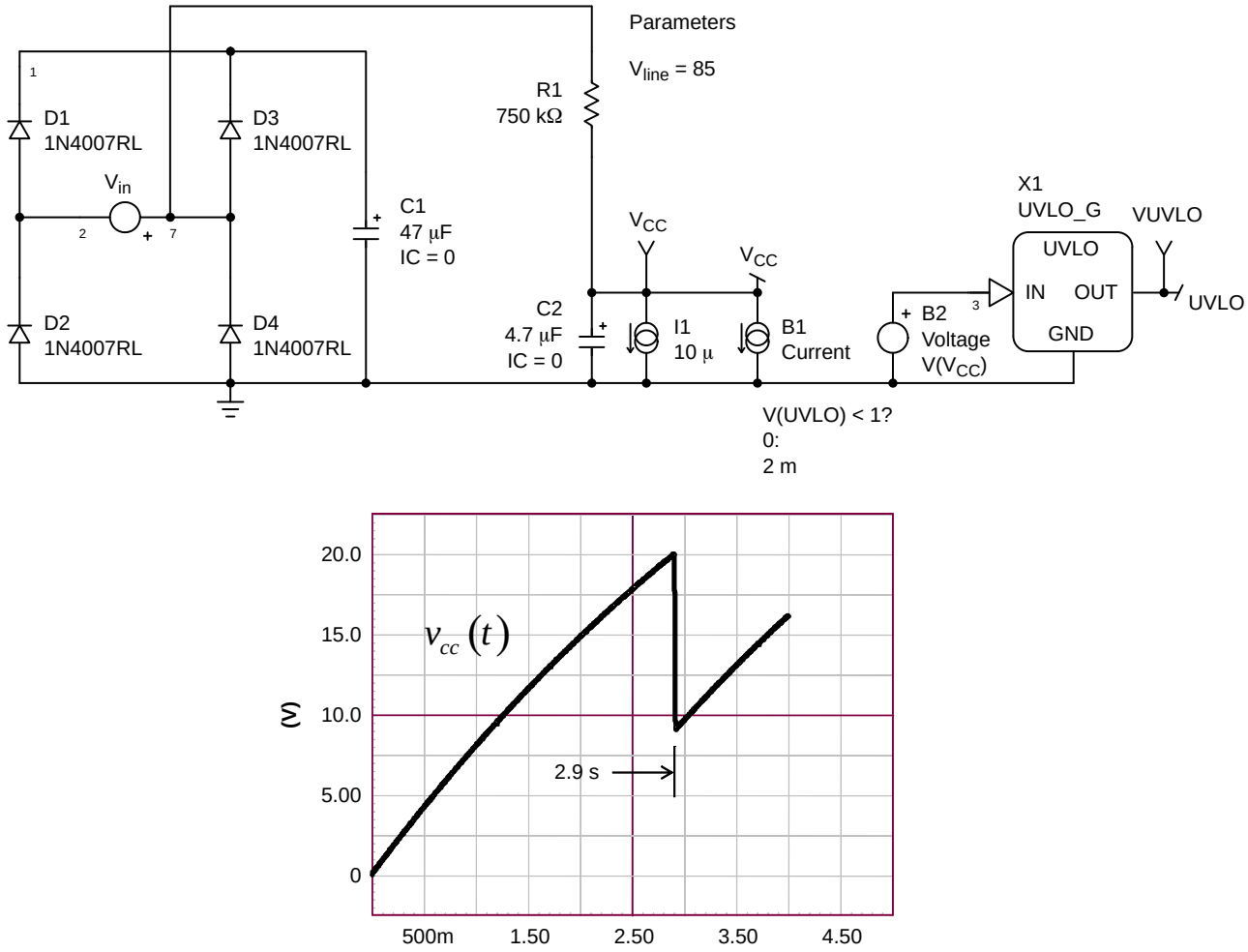



**Figure 8. Simulation is Helpful to Calibrate the Start-Up Resistor to the Correct Value**

It is then possible to show that the average power dissipated by the above network is given by the following formula. In this case, the peak voltage becomes the highest value (375 V dc, 265 V rms):

$$P_{R_1} = \frac{V_{pHL}^2}{4R_1} = \frac{375^2}{4 \cdot 750\ k} \approx 47\ mW \qquad \text{(eq. 9)}$$

It corresponds to a decrease compared to the power dissipated by connecting the start-up network directly to the rectified bulk voltage. To further gain in power dissipation, it can be possible to reduce the $V_{cc}$ capacitor a little more and thus increase the start-up resistor. Always make sure, though, that enough margin exists in worst case start-up conditions where natural component dispersions are being accounted for.

There is one thing you must keep in mind when designing the start-up network. If keeping the current at the lowest value is a must for a low standby power, it obviously slows down the start-up time. In some applications, where standby power is a less stringent parameter, it is desirable to crank the power supply in the shortest possible time. One way of doing it is to increase the start-up current. However, the auto-recovery circuitry works by discharging the $V_{cc}$ capacitor via an internal consumption of around 400 µA. Therefore, if you force a current $I_1$ greater than 400 µA, then the controller will no longer be able to discharge the $V_{cc}$ capacitor and auto-recovery is lost.

Another parameter that is worth considering, is the parasitic capacitor offered by a rectifying diode when blocked. In our calculations, we considered a nice continuous half-wave signal feeding the start-up resistor $R_1$. The reality is different as the rectifying diodes only conduct during the refueling of the bulk capacitor, probably a few milliseconds and even less during start up as the bulk capacitor is unloaded. For the rest of the time, they are blocked. Therefore, the current in $R_1$ is mainly provided by these parasitic capacitors during the considered half-wave portion of the sinusoid. Connecting an oscilloscope over the $V_{cc}$ pin could affect the parasitic path through the earth and might change the charging current, disturbing the measurement. To measure the start-up time, it is certainly better to only look at the ac input current using a dedicated current probe while the output of the converter is charged with a resistive load (an electronic load could, again, affect

the parasitic return and influence the measurement). Monitor the time at which the converter is plugged (this is $t = 0$ and you have a sharp in-rush spike) and look at the current shape until it is significantly affected. This is the time at which the converter operates and $V_{cc}$ has reached the turn-on level. As the power supply only requires a few tens of milliseconds to reach its regulation level, considering the time from $t = 0$ to the change in current shape as start-up time will not create a significant measurement error. On our adapter board, we have captured a typical start-up current signature obtained at an input voltage of 85 V rms. It shows a start-up time of 2.4 s.

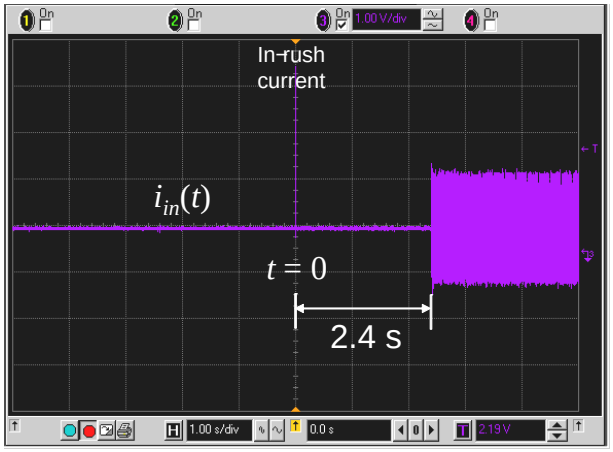



**Figure 9. On This Plot, the Start-Up Time is Measured at the Moment the Converter is Plugged to the Moment at which the Current Significantly Changes. The Load is a Passive Resistor and No Oscilloscope Ground is Connected to the Board**

### A Fully Capacitive Start-Up Network

In case no-load standby power needs to be extremely low, another solution consists of using a capacitive start-up network as shown in Figure 10. The charge pump operates from the two input branches and charges the $V_{cc}$ capacitor via two additional diodes. The traditional start-up network has disappeared and this solution offers the best performance in terms of standby power.

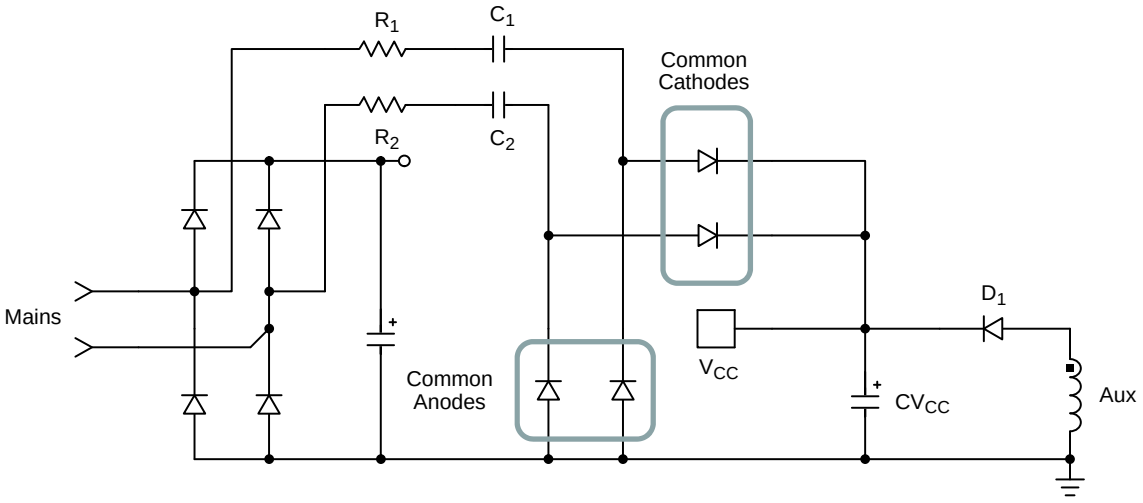



**Figure 10. A Capacitive Network Significantly Reduces All Losses Related to the Start-Up Resistors**

As shown in Figure 11, the network offers a fast turn-on time without the drawback of an extra power dissipation burden when the output load is removed.

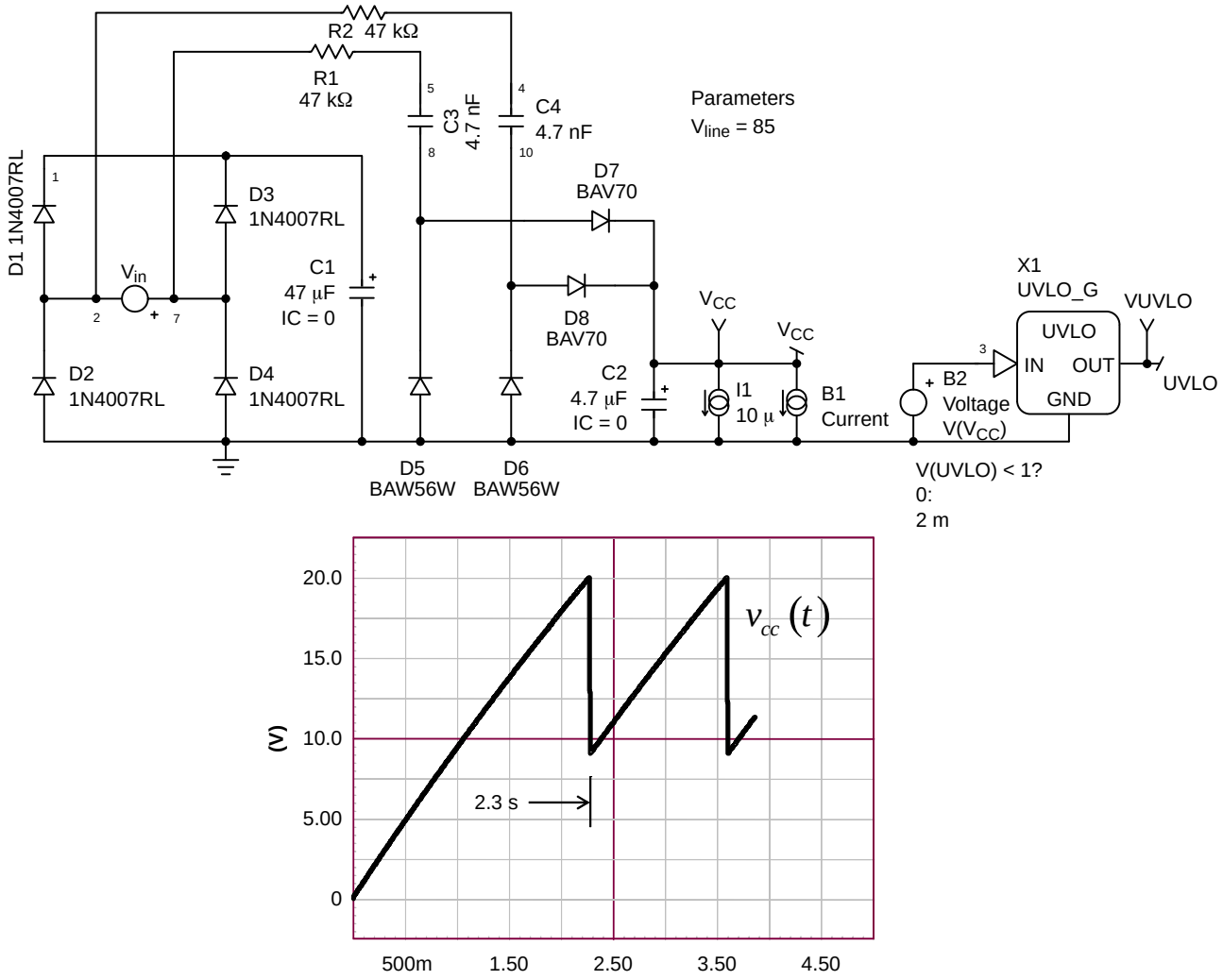



**Figure 11. A Simulation Setup Confirms the Performance of the Capacitive Network**

Figure 12 shows the start-up sequence recorded on the demonstration board. Component values are that of Figure 11 simulation example.

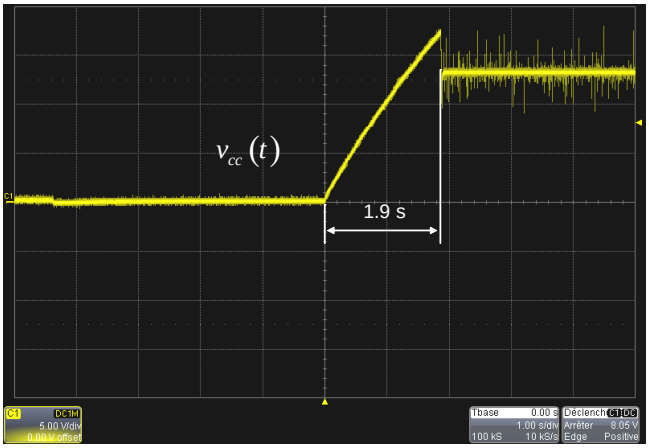



**Figure 12. The Start-Up Sequence Recorded on the Demonstration Board Featuring Capacitive Network. The Input Line is 85 V rms in This Example**

### Pin 6 – The Driver Output

The part features a CMOS-based output driving stage capable of sourcing and sinking 500 mA peak. As the part accepts $V_{cc}$ voltages up to 28 V, it is important to clamp the voltage actually applied to the gate-source terminals of the selected power MOSFET. NCP1256 clamps it to 12 V. The $r_{DS(on)}$ of a high-voltage MOSFET is usually defined at a 10-V $V_{GS}$ bias. Going below this value will make the resistance increase, together with the conduction losses. On the contrary, biasing the MOSFET well beyond this 10-V reference, will only reduce the $r_{DS(on)}$ by a very small amount, unnecessarily increasing the power dissipation in the driver. Also, at a certain bias level, the MOSFET lifetime can also be affected. The internal 12-V clamp offers a safe operating choice as shown in Figure 13.

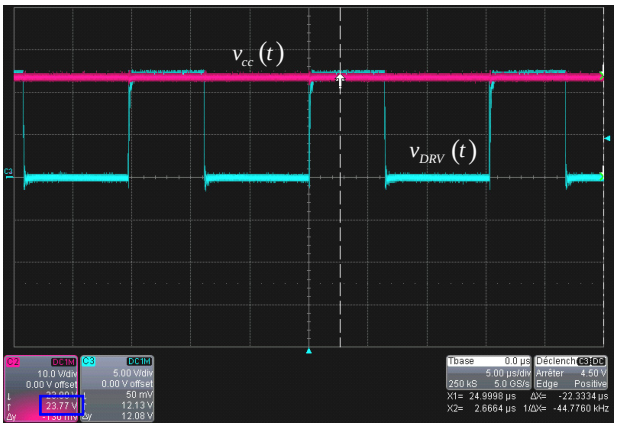



**Figure 13. The MOSFET Gate-Source Waveform is Safely Kept below 12 V**

Dissipation wise, it is now important to check that the selected MOSFET complies with the power dissipation capability of the package. If we look at the graph displayed in Figure 14, the junction-to-ambient thermal resistance for the smaller copper area (35-µm copper thickness) is 290°C/W for a 50-mm$^2$ pad. Additional measurements have shown that this number could be extrapolated to 360°C/W for half of this value, 25 mm$^2$. If we operate the part in an environment where the ambient temperature $T_A$ is 70°C and we want to limit the maximum junction temperature to less than 110°C, then the maximum allowable power the package can dissipate is:

$$P_{max} = \frac{T_{j,max} - T_A}{R_{\theta J-A}} = \frac{110 - 70}{360} = 111\ mW \qquad \text{(eq. 10)}$$

What are the sources justifying power dissipation in a PWM controller? The first one is the inherent consumption of the blocks (clock, comparators, references etc.). On the data-sheet, this is the parameter $I_{CC2}$ which also includes the various cross-conduction currents from the unloaded driver output. We have 0.8 mA. The other source is the average current necessary to drive the selected power MOSFET. This average current is nothing else than the total gate-charge $Q_G$ multiplied by the switching frequency $F_{SW}$:

$$I_{DRV,avg} = Q_G \cdot F_{SW} \qquad \text{(eq. 11)}$$

If we supply the controller from a $V_{cc}$ rail, then the power dissipation becomes:

$$P_D = \left(I_{CC2} + I_{DRV,avg}\right) \cdot V_{CC} \qquad \text{(eq. 12)}$$

Let's assume the $V_{cc}$ is set to 14 V. From Equation 10 and Equation 12, the maximum authorized current to drive the MOSFET becomes:

$$I_{DRV,avg} = \frac{P_D}{V_{CC}} - I_{CC2} = \frac{111\ m}{14} - 0.8\ m = 7.2\ mA \qquad \text{(eq. 13)}$$

With the help of Equation 11, we can compute the maximum allowed $Q_G$ for a junction temperature kept below 110°C in a 70-°C atmosphere:

$$Q_{G,max} = \frac{I_{DRV,avg}}{F_{SW}} = \frac{7.1\ m}{65\ k} \approx 110\ nC \qquad \text{(eq. 14)}$$

This number is fairly large and quite comfortable actually. Does it mean that the controller is capable to safely drive large gate-charge MOSFETs? Certainly not. The moderate driving capability of the NCP1256 would generate unacceptable switching losses and the total efficiency would suffer.

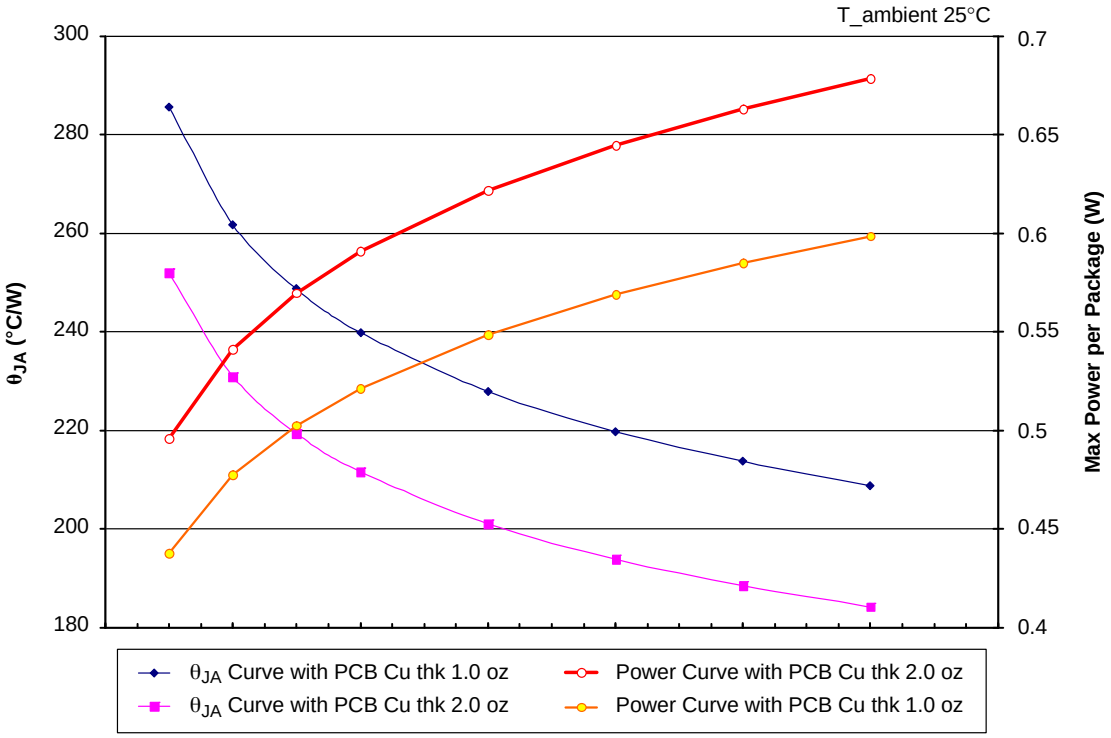



**Figure 14. The Power Dissipation on the Package Depends on the Copper Area around it**

Given this power dissipation constraints, it is important to look at the selected MOSFET data-sheet. For instance, a NDF04N60Z exhibits a total gate charge of 19 nC which is ok to be used with the NCP1256. Beyond these MOSFET sizes, for a 6-A or bigger, we recommend to add a small PNP transistor to help strengthening the turn-off discharge. This is what Figure 15 shows. In this picture, $Q_2$ is driven by $R_{16}$, adjusted to shape the turn-on time and soften the EMI signature of the converter. When pin 6 is down to ground, $Q_1$ is activated and blocks $Q_2$.

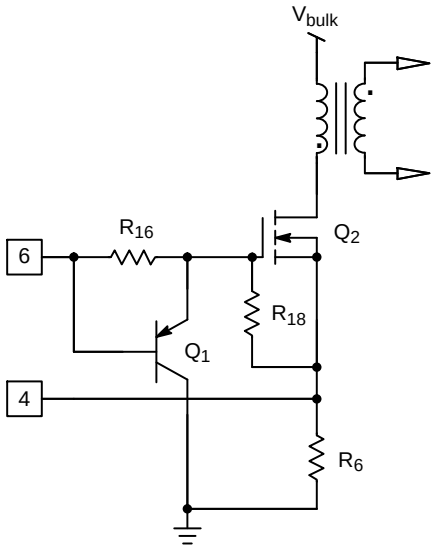



**Figure 15. A Small PNP Transistor Vigorously Pulls the Gate Down at Turn Off**

To avoid any production issues, e.g. leaving the gate open because the controller is not properly soldered, $R_{18}$ keeps the gate connected to the source whatever the circuit state. Don't use too low of a value for $R_{18}$ as standby power could suffer. A 47-kΩ will do. Please note that the addition of the external transistor helps reducing the power dissipated in the package.

**Pin 4 – The Current Sense Input**

The current sense pin routes the voltage developed across the sense resistor to a Leading Edge Blanking (LEB) circuit before reaching the PWM reset comparator. The LEB principle is to blind the current sense comparator for 300 ns and avoid false tripping because of spurious signals found on the sense voltage. The internal schematic appears in Figure 16 and discloses two switches.

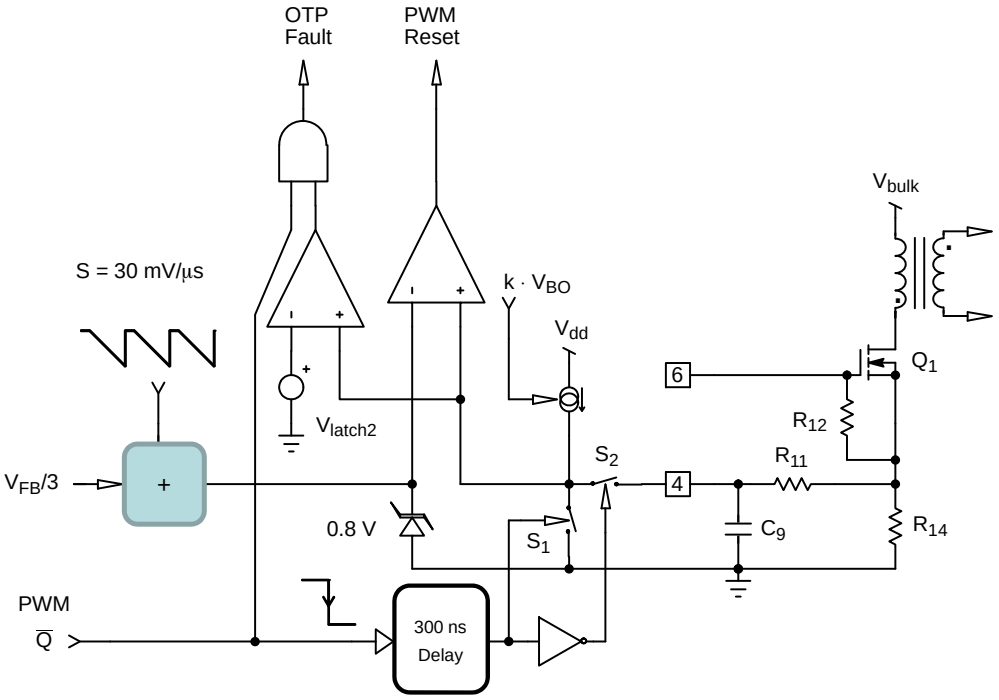



**Figure 16. The Current Sense Pin Monitors the Voltage Coming from the Sense Resistor which is Sized to Set the Maximum Inductor Output Current**

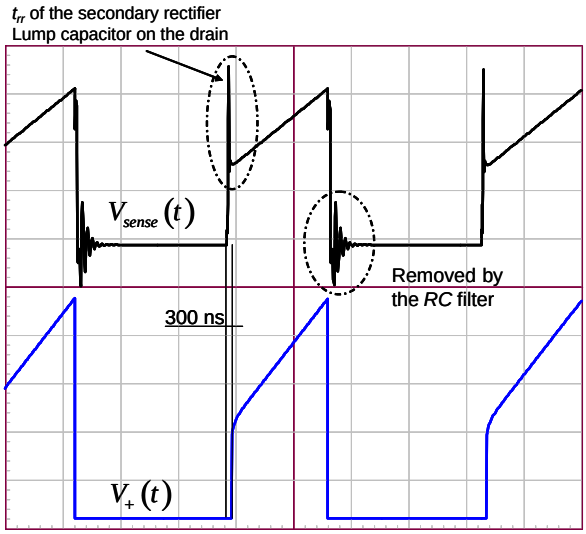



**Figure 17. The LEB Circuitry Removes All Oscillations Found on the Current Sense Signal**

When the driver output is high, the grounded switch $S_1$ is closed and the series switch $S_2$ is open. This network fully isolates the current-sense comparator from the CS pin. After 300 ns have elapsed, $S_1$ opens and $S_2$ closes, routing a clean signal to the (+) of the comparator (Figure 17).

Unlike NCP1250, the NCP1256 features an internal slope compensation signal. Slope compensation is necessary to tame sub-harmonic oscillations that occur in a current-mode converter operating in a Continuous Conduction Mode (CCM) with a duty ratio approaching or exceeding 50%.

The cure to this problem is to subtract a ramp of the correct amplitude from the feedback signal. This is the technique adopted for the NCP1256 and described in Figure 16. A ramp signal available from the clock circuitry is reversed, buffered and added to the feedback signal. The 30-mV/μs available downslope (65 kHz) is enough to cover the vast majority of CCM designs.

Assume a 19-V design in which the primary inductance $L_p$ is 600 μH and the transformer features a $N_p$:$N_s$ ratio of 1:0.25. The off-time primary current slope $S_p$ is thus given by:

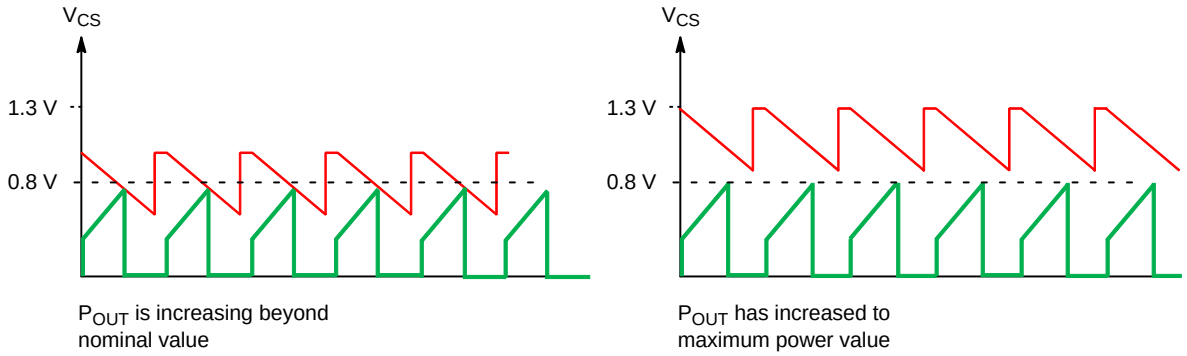
$$S_p = \frac{(V_{out} + V_f) \cdot \frac{N_p}{N_s}}{L_p} = \frac{(19 + 0.8) \cdot 4}{600\ \mu} = 132\ \text{kA/s} \quad \text{(eq. 15)}$$

Considering a sense resistor $R_{sense}$ of 330 mΩ, the above primary current ramp turns into a voltage ramp of the following amplitude:

$$S_{sense} = S_p \cdot R_{sense} = 132\ \text{k} \cdot 0.33 = \\ = 43.6\ \text{kV/s or } 43.6\ \text{mV/}\mu\text{s} \quad \text{(eq. 16)}$$

Given the internal 30-mV/μs slope, the compensation will reach 69%.

Since every design is unique, it is impossible to cover all possible cases with a fixed amount of slope compensation such as that of Equation 16. For this reason, to avoid affecting the maximum peak current setpoint despite this artificial ramp presence, the compensation ramp decreases as the output power increases. When the feedback voltage runs open-loop ($V_{FB}$ = 4 V), the ramp completely disappears, offering the maximum sense voltage of 0.8 V (assume no OPP current). This allows the usage of the NCP1256 in extremely large input ripple situations, when the bulk capacitor is small or if the converter must still operate at a low input voltage. It is likely that sub-harmonic oscillations occur in this case but it will not affect the converter's output in this extreme input voltage case. Figure 18 details this operation.




$P_{OUT}$ is increasing beyond nominal value

$P_{OUT}$ has increased to maximum power value

**Figure 18. Slope Compensation Purposely Reduces as $P_{OUT}$ Increases to Avoid Affecting the Maximum Peak Current at the Lowest Input Line**

With this typical configuration, the feedback voltage can potentially be in regulation beyond 2.4 V as the ramp compensation is gradually decreased.

### Over Power Protection

The maximum power a flyback converter can deliver depends on several variables such as the switching frequency, the primary inductance and the maximum allowable primary peak current. Among these three variables, all of them are theoretically fixed and constant. Therefore, the power the converter can deliver at high input voltage should theoretically not differ from that delivered at the lowest input voltage. In reality, we know that both values differ and sometimes, in a large proportion. If we consider the primary inductance and the switching frequency independent from the input voltage, the final peak current seen by the inductor actually depends on the input voltage. Why? Because when the internal current-sense comparator detects an over-current condition, it takes time for this information to propagate inside the controller and eventually, bring the MOSFET gate down. The needed time is called the propagation delay. Most of the data-sheets, including the NCP1256, give you the propagation delay inherent to the controller, alone, when loaded by a 1-nF capacitor. In reality, depending on the drive current capability, the various resistors in series with the gate and the MOSFET gate-charge, it can be significantly longer. Figure 19 shows the resulting signals at low and high line levels. Depending on the propagation delay, the difference in current can be quite significant, impacting the maximum power at high line:

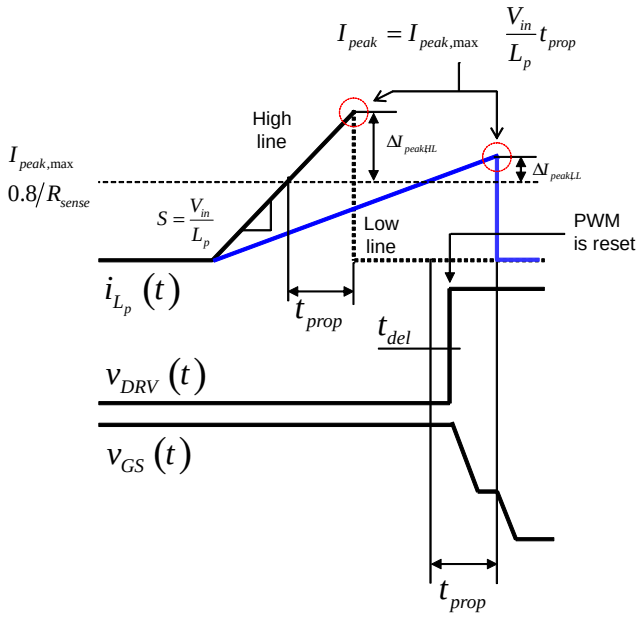



**Figure 19. The Propagation Delay Affects the Final Peak Current Value at High Line**

$$I_{peak,max} = \frac{V_{sense}}{R_{sense}} + \frac{V_{in}}{L_p} \cdot t_{prop} \qquad \text{(eq. 17)}$$

The peak current runaway at high line is only partially responsible for the power increase in this operating condition. The second culprit is the transition from Continuous Conduction Mode (CCM) to Discontinuous Conduction Mode (DCM). This phenomenon happens because the on time naturally reduces at high line and offers more off-time to demagnetize the primary inductor (the inductor downslope is constant). This is what Figure 20 shows you. In this picture, we can see that the valley current tends to decrease as the input voltage goes up. The power transmitted by a flyback converter operating in CCM obeys the following formula:

$$P_{out} = \frac{1}{2} \cdot L_p \cdot \left(I_{peak}^2 - I_{valley}^2\right) \cdot F_{SW} \cdot \eta \qquad \text{(eq. 18)}$$

Where: $L_p$ is the primary inductance, $I_{peak}$ is the maximum inductance peak current, $I_{valley}$ is the inductance valley current, $F_{sw}$ is the switching frequency and $\eta$ is the converter efficiency. Since we deal with a peak current controller, in fault condition at high line, the maximum peak current will slightly increase compared to that obtained at low line as predicted by Equation 17. What actually matters in Equation 18 is the reduction of $I_{valley}$ inherent to a longer off time. By manipulating a few equations, it is possible to calculate the valley current at high line and thus compute the power generated in this condition:

$$I_{valley,HL} = I_{peak,max,HL} - \frac{T_{SW} \cdot V_{in,HL} \cdot \left(V_f + V_{out}\right)}{L_p \cdot \left(V_f + V_{out} + NV_{in,HL}\right)} \qquad \text{(eq. 19)}$$

Where:

$T_{SW}$ is the switching period (15 µs or 65 kHz)

$V_f$ is the secondary diode forward drop at the maximum output current (0.5 V)

$V_{out}$ is the converter output voltage (19 V)

$L_p$ is the primary inductance (600 µH)

$N$ is the transformer turns ratio $N_S$ / $N_p$ (0.25)

$t_{prop}$ is the total measured propagation delay (350 ns)

$V_{in,HL}$ = 370 V

$V_{in,LL}$ = 120 V

$R_{sense}$ is the sense resistor (0.33 Ω)

$V_{peak,max,HL}$ is the maximum peak current obtained for $V_{in} = V_{in,HL}$ in Equation 17: 2.64 A

$V_{peak,max,LL}$ is the maximum peak current obtained for $V_{in} = V_{in,LL}$ in Equation 17: 2.49 A

With the above numbers, we obtain the following valley currents:

$$I_{valley,LL} = 1.28 \text{ A} \qquad \text{(eq. 20)}$$

$$I_{valley,HL} = 0.99 \text{ A} \qquad \text{(eq. 21)}$$

Based on these two numbers, we can now compute the maximum power delivered by the converter at low and high line levels:

$$P_{max,LL} = \frac{1}{2} \cdot L_p \left(I_{peak,max,LL}^2 - I_{valley,LL}^2\right) F_{SW}\, \eta_{LL} \approx \approx 76 \text{ W} \qquad \text{(eq. 22)}$$

$$P_{max,HL} = \frac{1}{2} \cdot L_p \left(I_{peak,max,HL}^2 - I_{valley,HL}^2\right) F_{SW}\, \eta_{HL} \approx \approx 104 \text{ W} \qquad \text{(eq. 23)}$$

In this equation, we considered the low-line efficiency $\eta_{LL}$ at 85% whereas it increased to 89% in high-line conditions. The power growth at high line reaches 37% compared to that at low line. In terms of currents, for a 19-V output, the maximum low-line current is 4 A and can go up to 5.5 A at the maximum input voltage. In our example, as we target a 60-W adapter ($I_{out}$ = 3.2 A), the current computed by Equation 23 is way too high and a means has to be found to reduce it.

Several techniques are available to clamp down the maximum output power. Such techniques include developing an offset on the current-sense pin in relationship to the input voltage. Unfortunately, this option wastes power and affects the standby power or the efficiency in light load conditions. The best is to directly play on the maximum peak current limit based on the bulk voltage level without sensing it directly to avoid power dissipation.

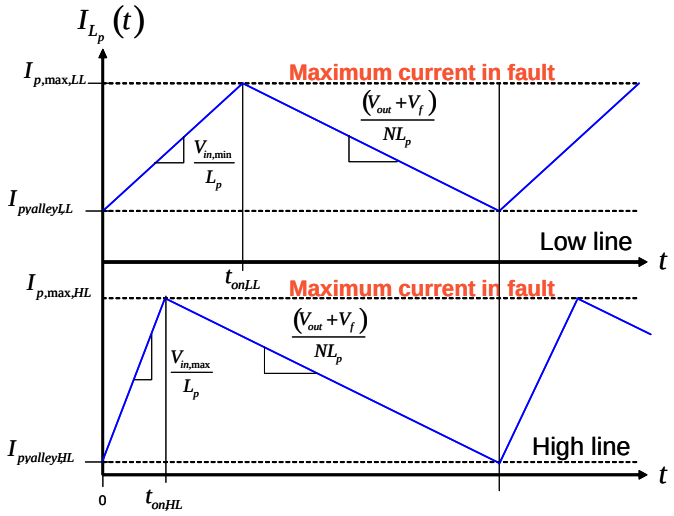



**Figure 20. As the On-Time Reduces at High Line, the Off-Time Expands and Lets the Valley Current Go Down, Making the Operating Mode Closer to DCM: the Energy Released at Turn Off Increases**

With the NCP1256, at low line and without any compensation, the maximum voltage across the current sense pin is limited to 0.8 V. To lower this signal at high line, the adopted solution is to build a dc offset on the CS pin proportional to the input voltage. This is what Figure 21 describes. The brown-out sensing network gives an image of the input voltage, further transformed into a current by the internal OTA. The obtained current in then sourced out from the CS pin to generate a voltage in series with the current sense information. The information brought to the CS pin is thus artificially increased in high-line conditions, reducing the maximum primary-side current in fault condition.

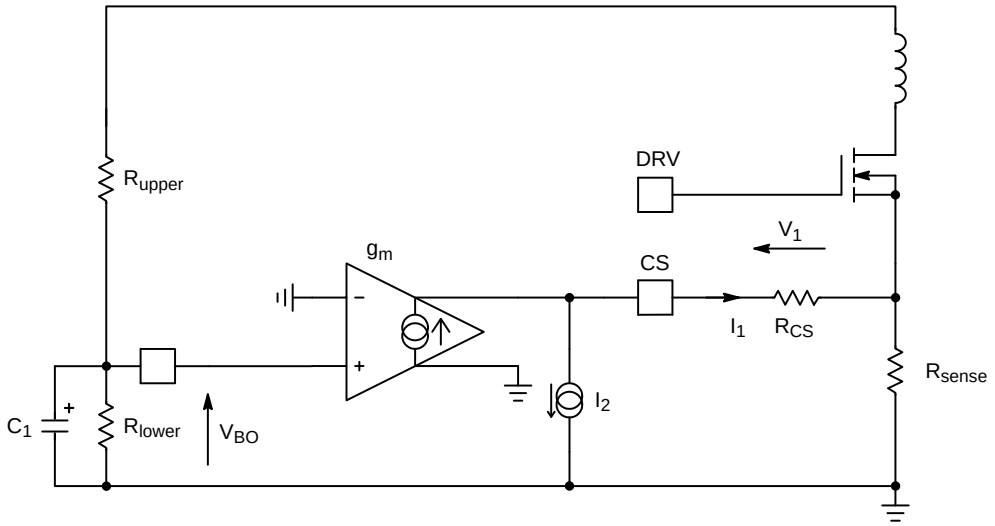



**Figure 21. The Brown-Out Divider Senses the Input Voltage and Controls a Current Leaving the CS Pin**

Current source $I_2$ absorbs the current generated for a BO voltage of 800 mV, suppressing the compensation at the lowest line input. According to the NCP1256 data sheet, the current sourced out from the CS pin at a 0.8-V bias voltage on the BO pin is almost 0. If this turn-on voltage corresponds to 80 V rms, then when this pin reaches 2.65 V ($V_{in}$ = 265 V rms), the current amounts to 185 μA.

To calculate the exact amount of OPP your design needs, we have to extract the peak current at high line producing the same output power as in low line operation. This is done by equating Equation 22 and Equation 23 then subtracting the propagation delay contribution. You obtain:

$$I_{peak,max,HL} = \frac{F_{SW}L_p\eta_{HL}\Delta I_{L_p,HL}^{\ 2} + 2P_{max,LL}}{2\eta_{HL}F_{SW}L_p\Delta I_{L_p,HL}} - \\ - \frac{V_{in,HL}}{L_p} \cdot t_{prop} = 1.93\ A \quad \text{(eq. 24)}$$

In this equation, the term $\Delta I_{Lp,HL}$ represents the inductor ripple at high line and is computed as:

$$\Delta I_{L_p,HL} = \frac{T_{SW} \cdot V_{in,HL} \cdot (V_f + V_{out})}{L_p \cdot (V_f + V_{out} + NV_{in,HL})} \quad \text{(eq. 25)}$$

Having in this example a sense resistor of 0.33 Ω, we produce a peak current of 0.8 / 0.33 = 2.42 A. To make this number go down to 1.9 A, we need to decrease the value of the reference voltage by:

$$V_{OPP} = I_{peak,max,HL} \cdot R_{sense} - V_{ref} = \\ = 1.93 \cdot 0.33 - 0.8 \approx -160\ mV \quad \text{(eq. 26)}$$

We found that a 160-mV offset will limit the output power at high line. To generate this offset from the 185-μA source, we can install a series resistance $R_{CS}$ of the following value

$$R_{CS} = \frac{160\ m}{185\ \mu} = 864\ \Omega \quad \text{(eq. 27)}$$

Despite the presence of a LEB inside the controller, we recommend to install a small 100−220-pF capacitor very close to the controller's CS and GND pins as shown below in the PCB design section. The final value in the demonstration board leads to selecting a 910-Ω series resistor.

**CS Pin Latch Input**

The CS pin offers the possibility to latch off the part in case the current sense voltage exceeds a certain value during the off time only. This technique offers a convenient means to implement over temperature protection (OTP) by connecting a negative temperature coefficient (NTC) resistor from the auxiliary diode anode to the CS pin via a resistor and a series diode. Please note that the NTC connects to the auxiliary ac voltage and not the $V_{cc}$. Should you connect the NTC to a continuous signal instead, the part could not properly latch off since a kind of primary-side regulation would be implemented by offsetting the current-sense level as the temperature increases. Figure 22 represents a typical configuration for this arrangement. The diode needs to be fast with a low parasitic capacitance. A BAV21 is a good choice and was tested with success. Series resistor $R_{80}$ adjusts the OTP level depending on the reflected voltage at turn off. Assume we select a NTC such as NTCLE100E3 from Vishay. We picked the part exhibiting a 100-kΩ resistance at a 25-°C ambient temperature. If we want to shutdown our adapter at 100°C, the resistance given by the NTC at this level is 5.8 kΩ. In our adapter, the reflected plateau level on the auxiliary winding is 14.5 V and the diode forward drop is 0.6 V. Considering a 1.5-V latch level on the CS pin and a 910-Ω OPP resistance, how do we calculate the series resistor to trip the protection when the NTC resistance is 5.8 kΩ? When CS is biased to 1.5 V and neglecting the sense resistor contribution, the current circulating in the 910-Ω CS resistor is

$$I_1 = \frac{1.5}{910} \approx 1.65\ mA \quad \text{(eq. 28)}$$

From a 14.5-V auxiliary winding, the series arrangement of the NTC and $R_{80}$ must drop

$$V_{drop} = 14.5 - 0.6 - 1.5 = 12.4\ V \quad \text{(eq. 29)}$$

The total resistance value given the current $I_1$ is

$$R_{tot} = \frac{V_{drop}}{I_1} = \frac{12.4}{1.65\ m} \approx 7.5\ k\Omega \quad \text{(eq. 30)}$$

With a 5.8-kΩ NTC resistance, the series resistance $R_{80}$ is simply

$$R_{80} = 7.5\ k - 5.8\ k = 1.7\ k\Omega \quad \text{(eq. 31)}$$

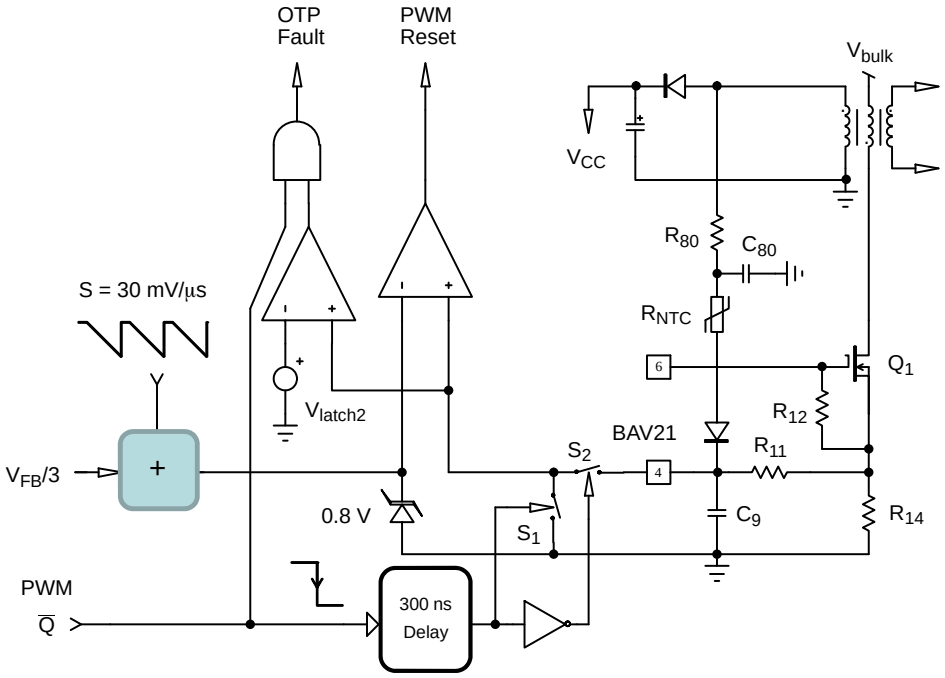



**Figure 22. A NTC Biasing the CS Pin during the Off-Time will Trip the Protection in Case an Over-Temperature is Sensed**

With the configuration shown in Figure 22, it is possible to add small filter with capacitor $C_{80}$ in case the leakage inductance contribution is too energetic. The filter time constant needs to be adjusted so that the overshoot on the auxiliary voltage goes away. Please note that the filter must be installed before the diode and not after it otherwise peak rectification will occur. $C_9$ provides additional filtering and improves noise immunity. Figure 23 shows the waveform at the BAV21 anode before and after capacitor $C_{80}$ addition. In Figure 24, the external voltage is applied during the off time and increases proportionally to the ambient temperature. Please note that the peak current setpoint (hence the delivered power) is absolutely unaffected by the off-time offset. In the right-side of Figure 24, the temperature has reached the maximum limit and latches off the part. In this mode, $V_{cc}$ hiccups and no pulses are present. Reset occurs either via a $V_{cc}$ cycling ($V_{cc}$ must fall below $VCC_{reset}$) or an input voltage cycling detected by the BO circuitry.

This OTP technique offers a very precise way for shutting off the part in case of temperature runaway. The ±3% voltage precision on the CS pin gives a precise trip point as long as the auxiliary voltage is stable. In case more precision is needed, you can always use an extra PNP transistor and connect the NTC to a precise voltage. This is what Figure 25 shows as a first option. The Zener diode creates a precise reference level to which the NTC connects. This scheme works well in the split $V_{cc}$ supply configuration where the Zener bias current does not hamper start-up time. A trick is to select a Zener voltage higher than the $V_{cc}$ value when the load is getting lighter. For instance, if at full load $V_{cc}$ is 15 V but drops to 11.5 V when the load is removed, then selecting a 13-V Zener diode is an interesting option as no extra bias will affect standby power. As temperature runaway usually occurs in high-load conditions, the Zener bias will be back in place as soon as the output power increases. Forcing the auxiliary $V_{cc}$ to slightly drop in no-load standby is possible if you insert a resistor in series with the auxiliary diode. Any resistance will limit the refueling current at turn off and $V_{cc}$ will immediately drop with a few ohms. In case the resistance is too big, the circuit will go into UVLO.

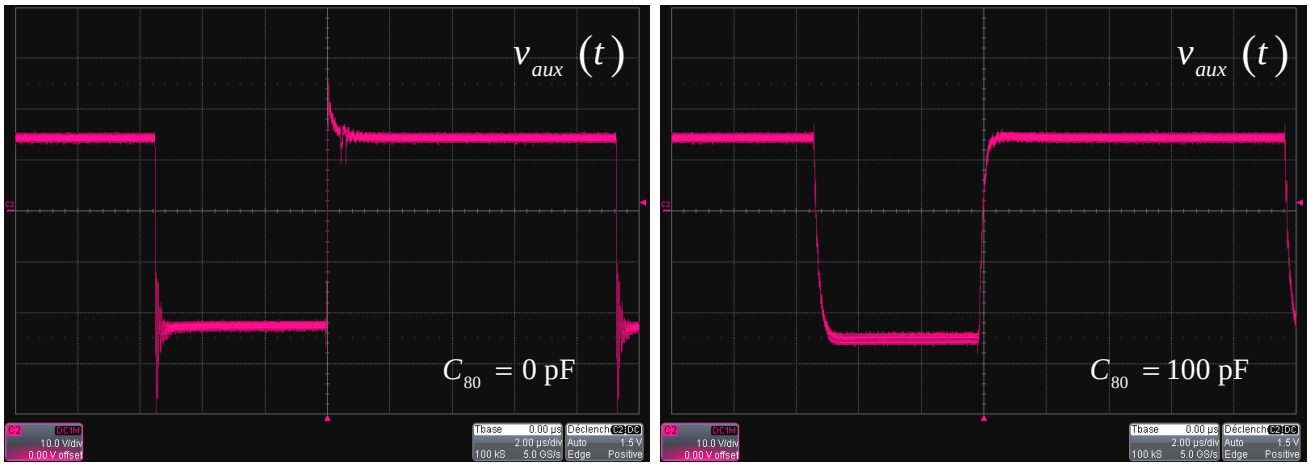



**Figure 23. A Small Capacitor Helps Filter the Leakage Contribution on the Auxiliary Voltage. A Clean Plateau Voltage Offers an Excellent OTP Precision**

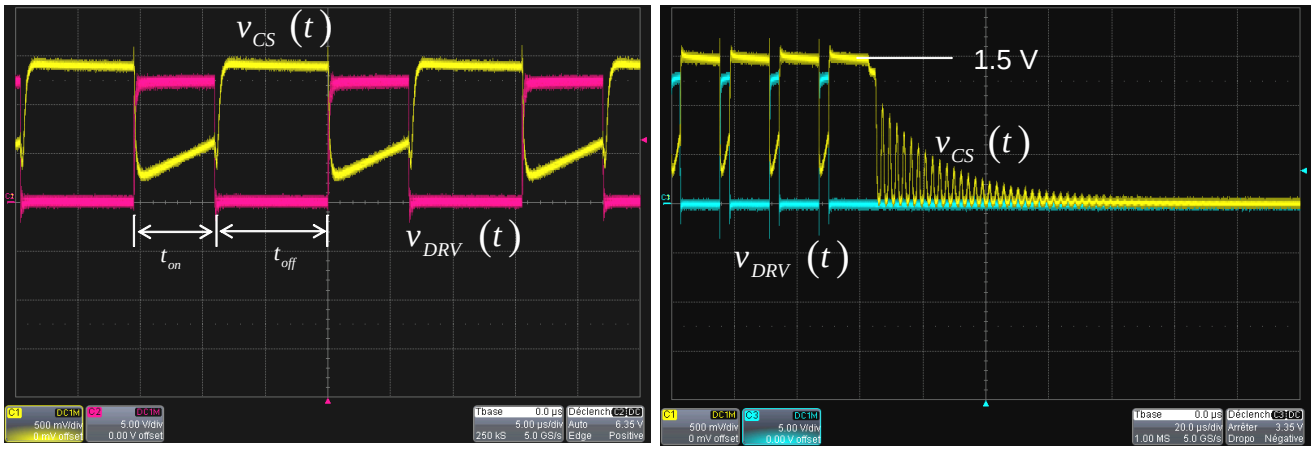



**Figure 24. When Temperature Increases, the Voltage Grows on the CS Pin during the Off Time. When it Reaches 1.5 V for Four Consecutive Times, the Part Latches Off**

For designers who want to combine OTP and OVP, the right-side of Figure 25 offers an interesting solution in which both the NTC and the Zener diode are connected to the auxiliary $V_{cc}$. Please note that this solution also requires a split $V_{cc}$ supply solution otherwise $Q_3$ will severely affect the start-up current.

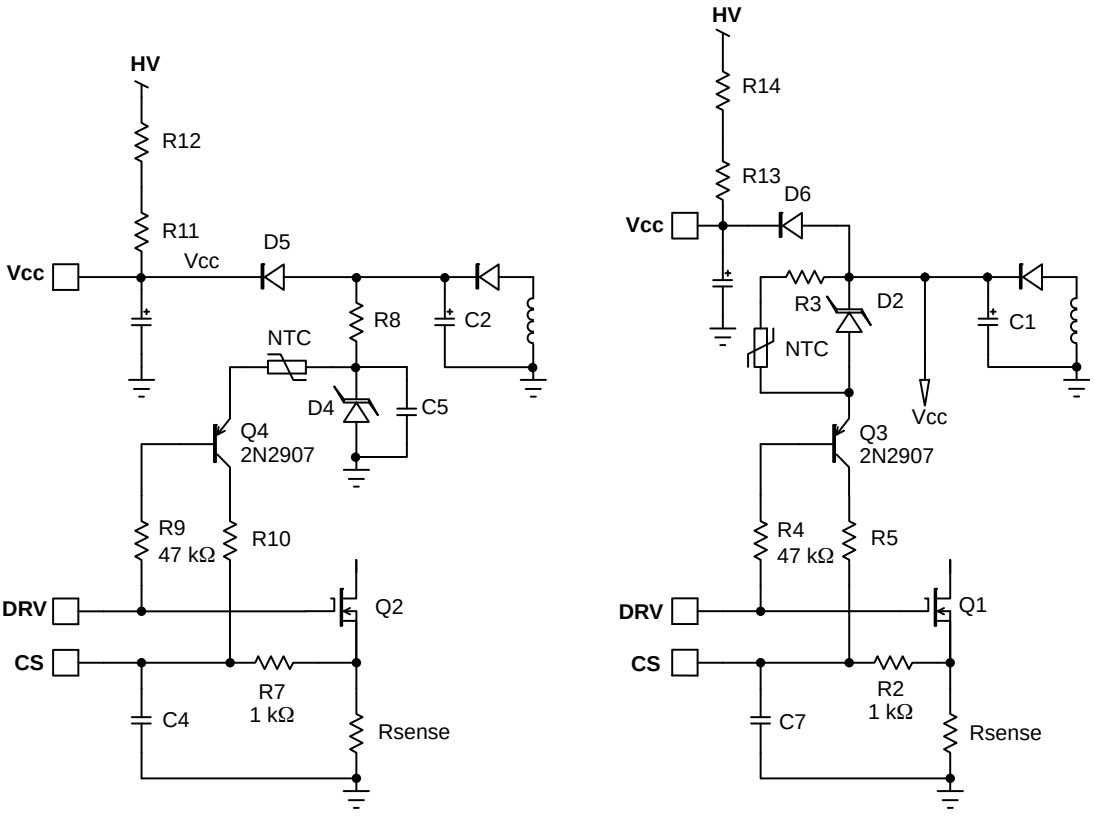



**Figure 25. Using an Extra PNP Transistor Lets you Connect the NTC to a Stable Voltage. In Case OTP and OVP have to be Combined, the Right-Side Offers another Interesting Solution**

### Maximum Peak Current Limit and Short-Circuit Protection

In case the feedback signal is lost, e.g. if the optocoupler is destroyed or the output undergoes a short-circuit, the peak current setpoint will be pushed to the maximum level. In this condition, the feedback pin is no longer pulled to ground by the optocoupler and reaches the open-loop level of 4 V. In this controller, without Over Power Protection (OPP) signal on pin 4, the maximum allowable level on the current sense pin is 0.8 V as slope compensation disappears (see Figure 18). As soon as the controller detects that the maximum peak current setpoint is reached, an internal countdown occurs. The minimum duration of this countdown is 50 ms. If within this period of time the feedback brings the peak current setpoint within operational limits (i.e. below 0.8 V, normal operation) for 8 consecutive clock times (assume a transient overload only), then the timer is reset. On the contrary, if during 50 ms (min) the controller still senses an over current condition, then at the end of the countdown, the circuitry stops all switching pulses. At this point, the auxiliary winding contribution to $V_{cc}$ disappears and the $V_{cc}$ capacitor remains alone to self-supply the controller: the voltage across its terminals falls down. Again, as the current consumed by the controller is around 400 μA, you have to make sure that the start-up current is not higher than this value otherwise $V_{cc}$ will not drop. When $V_{cc}$ finally reaches the $VCC_{(min)}$ value, around 9 V, the circuit is reset and the consumption goes back to 10 μA (max): the $V_{cc}$ level starts to rise towards $VCC_{ON}$, initiating a start-up sequence. Owing to the double hiccup, the first $VCC_{ON}$ voltage point is ignored and no pulses are issued. $V_{cc}$ falls again and at the next restart point, drive pulses are delivered as an attempt to resume operations. If the fault is gone, the power supply is back in operations: this is the auto recovery mode for the NCP1256B shown in Figure 3. The A extension latches off in presence of a fault.

### Pre-Short Protection

When a switching converter undergoes a short circuit on its output, the feedback pin goes open-loop and the peak current is pushed to the upper limit. In circuits like NCP1250, as explained in the above paragraph, a timer counts and upon completion, stops all pulses. In certain applications, this mode must be latched implying that the controller does not attempt to resume operations but simply latches off. The user must cycle the input power to restart the converter. To confirm the fault, enough time must be given to the controller to let its internal counter count down and trip the latch. If $V_{cc}$ collapses while this happens, the timer will never have the time to countdown and an auto-recovery UVLO event is detected: the part never latches off. A typical case arises when the short circuit is present at start-up: $V_{cc}$ disappears very quickly and the controller can never be latched because the timer is not given enough time to elapse.

To make sure the controller truly latches off even when the short circuit is present at start up, the NCP1256 includes the so-called pre-short logic: at the first start-up sequence, an internal latch is armed and allows the UVLO event to latch off the part while the short circuit flag is asserted. Once the feedback is in regulation, the latch is reset and UVLO becomes auto-recovery again. Practically, if at start up a short circuit is already there, the peak current is immediately set to its max value after the soft-start sequence and never reduces to a normal value since feedback is lost. When a UVLO is sensed in this condition, then the part latches off. In a normal start-up situation, should a UVLO be sensed after the part has entered regulation, then UVLO is auto-recovery, as it should be. Figure 26 illustrates this behavior in two different operating conditions: short circuit at start up with proper latch, UVLO while in operation which does not latch the part.

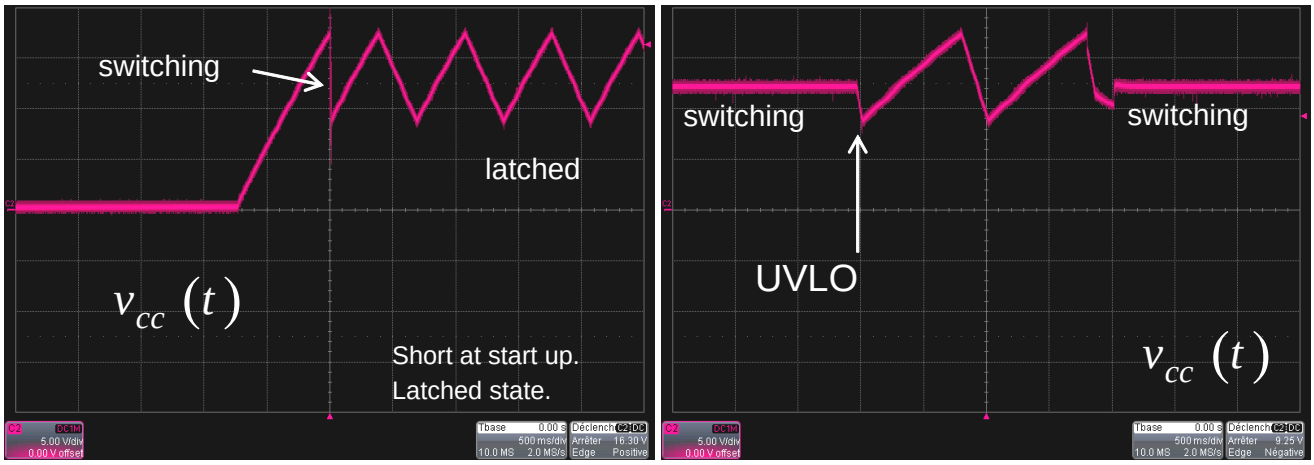



**Figure 26. NCP1256 Includes a Pre-Short Logic which Helps Protecting the Converter in Case of a Secondary-Side Short Circuit Present at Power Up**

### Pin 1 – The Circuit Ground

Usually, there is not much to say about the circuit ground. However, even if we deal with moderate-power converters, we need to apply a few rules pertinent to the power electronics world. The most important one is to make sure all ground-referenced sensitive signals returns to a quiet 0-V point, the controller ground pin. For instance, the optocoupler collector is connected to the feedback pin of the NCP1256 (pin 2) whereas its emitter pin must connect to the ground. As the optocoupler is often placed remotely from the controller, it can be tempting to connect the emitter to the closest ground trace, perhaps the sense resistor return or even the Y-capacitor line. Please do not otherwise spurious oscillations could take place and make the whole converter unstable. Rather, route a copper trace along the one that already routes the collector and connect it to the controller ground point. Make sure the compensating capacitor ($C_7$ in Figure 1) is not placed across the optocoupler, but right between the controller pins 2 and 1. These recommendations also apply for the current sense network ($C_9$ and $R_{11}$ from Figure 1) that must be placed very close to the controller. A copper trace from $R_{11}$ can then be placed to reach the sense resistor. Even if the trace is long, it is of less importance as the conveyed signal is low impedance. Figure 27 shows an example of Printed Circuit Board (PCB) routing when using the NCP1256.

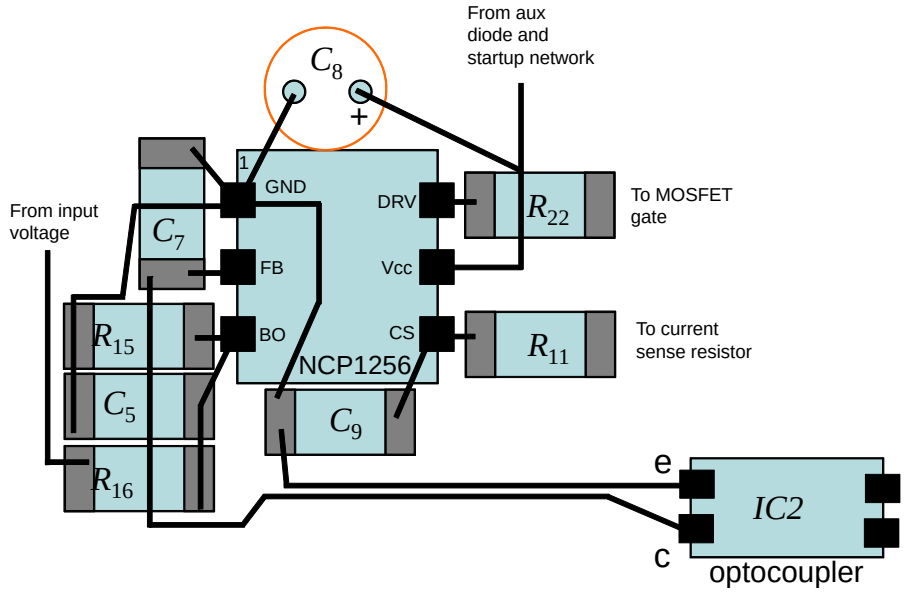



**Figure 27. Decoupling Components Must be Placed Very Close to the Controller**

### Pin 2 – The Feedback Pin

The feedback pin in a current-mode-controlled power supply is the control input that sets the inductor peak current on a cycle-by-cycle basis. The internal circuitry around pin 2 in the NCP1256 appears in Figure 28.

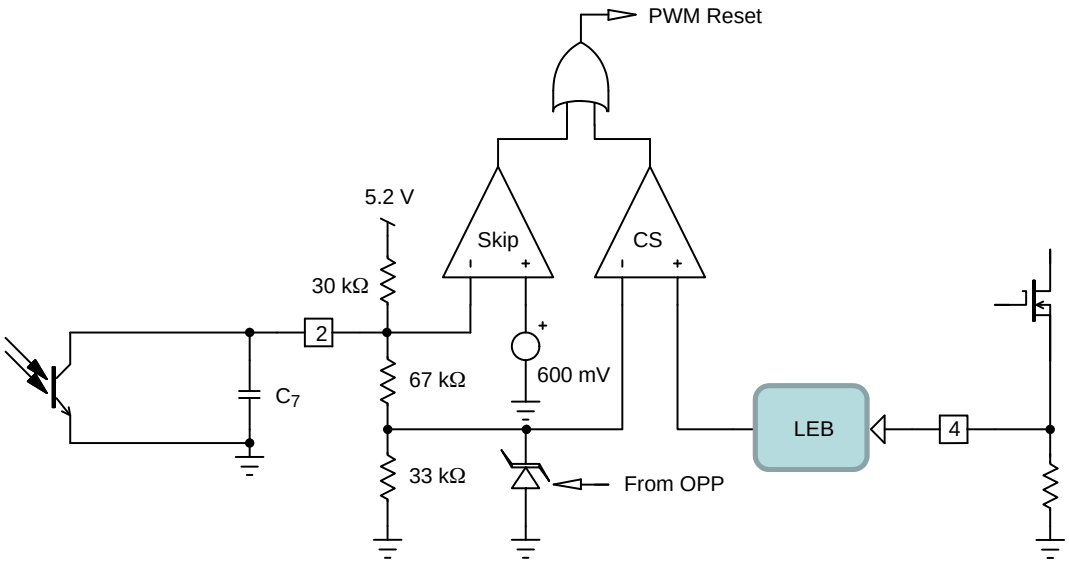



**Figure 28. The Internal Simplified Schematic of the Feedback Circuitry**

The regulation is obtained by pulling the feedback pin to ground via the optocoupler collector. The division ratio from the feedback pin to the current sense comparator is 3. However, the maximum current voltage setpoint cannot exceed 0.8 V. For ac analysis, the equivalent pull-up resistor is made by the paralleling of the upper 30-kΩ resistor with the series combination of the 67-kΩ and the 33-kΩ resistors. It forms an equivalent value $R_{eq}$ of 23 kΩ. Capacitor $C_7$ in parallel with the optocoupler parasitic pole contributes a total capacitor $C_{tot}$ equal to $C_7 \parallel C_{opto}$ and introduces a pole at a frequency of

$$f_p = \frac{1}{2\pi R_{eq}\left(C_{opto} \parallel C_7\right)} \quad \text{(eq. 32)}$$

When the load is getting lighter, the operating frequency is decreased to limit the switching losses and thus improve the efficiency in this mode. An internal Voltage Controlled Oscillator (VCO) observes pin 2. When the voltage on this pin stays above 1.5 V, the frequency is fixed and corresponds to the nominal value, 65 or 100 kHz. As the load current still decreases, so does the feedback voltage. The VCO senses this change and the switching frequency

also goes down. The lower limit is 26 kHz typically and will be reached for a feedback voltage of around 1.2 V. Between these two levels, both peak current and frequency are adjusted by the control loop. Below 1.2 V, the peak current can further go down until the feedback reaches 0.75 V. Internally, this level corresponds to a 250-mV setpoint, or (250 m / 0.8) · 100 = 31.2% of the nominal peak current. As an example, if you have a 1-Ω sense resistor, the maximum peak current in absence of OPP and internal ramp will be 0.8 / 1 = 800 mA. The skip operation will then occur at a ≈ 250-mA peak inductor current.

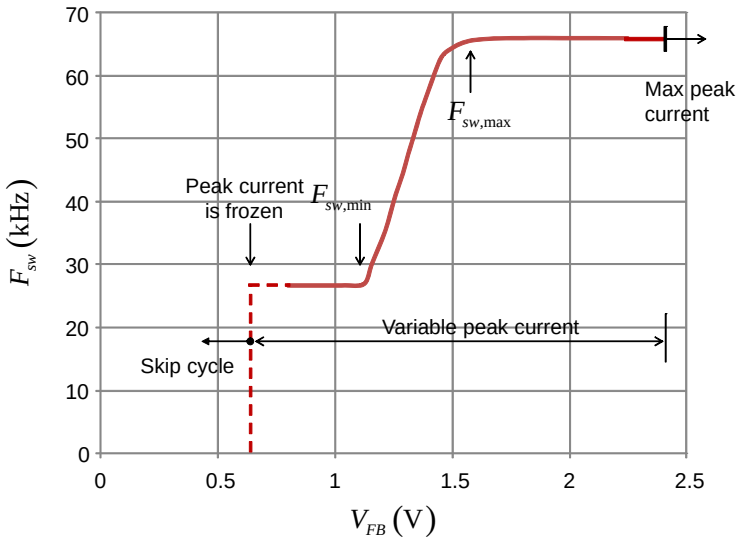



**Figure 29. The Frequency is Reduced as the Feedback Pin Passes below 1.9 V. Frequency Foldback Ends for a 1.5-V Feedback Voltage**

This value combined with a 26-kHz frequency guaranties the lowest acoustic noise in the transformer or in the *RCD* clamp network.

### Shutting Down the Controller

Thanks to the presence of the skip-cycle comparator, it is easy to stop the controller. Just permanently pull the feedback pin below 0.6 V and switching pulses are stopped. Figure 30 shows that a simple transistor whose collector or drain is connected to the feedback pin is enough to stop the controller.

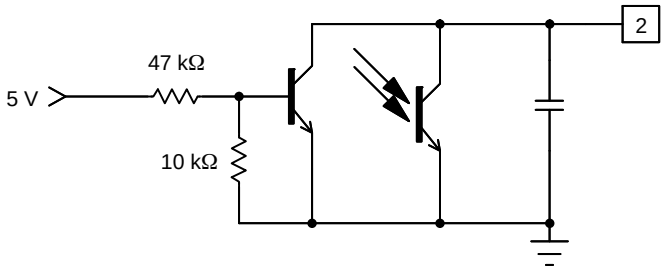



**Figure 30. A Simple Transistor, Bipolar or a MOSFET, can be Used to Stop the Controller**

### Pin 3 – The Combined OVP−BO Pin

The BO pin offers a means to select the minimum input voltage at which the converter can operate. Below this level, switching operations stop until the input voltage comes back within the normal range. Upon return of the mains, there are two options: a) $V_{cc}$ is below $VCC_{ON}$ then the controller lets $V_{cc}$ drops to UVLO and restarts pulsing at the next $VCC_{ON}$. B) $V_{cc}$ is above $VCC_{ON}$ then the controller immediately pulses upon return of the mains. There are several solutions to sense the input voltage as described by Figure 31. In the left side of the figure, this is the most classical solution in which the rectified high-voltage is sensed. The turn-on and turn-off thresholds are easily calculated by the following formulas. The first design parameter is the bridge bias current you accept to pay as extra power dissipation. Assume you accept to dissipate 20 mW at 375 V dc in the BO bridge, then the bias current is

$$I_{biasHL} = \frac{P_{BO}}{V_{in,max}} = \frac{20\ m}{375} = 53\ \mu A \qquad \text{(eq. 33)}$$

Scaled down to the selected turn-on voltage at 80 V rms (113 V dc), this bias current becomes

$$I_{biasLL} = 53\ \mu \cdot \frac{113}{375} \approx 16\ \mu A \qquad \text{(eq. 34)}$$

Considering the first threshold of 800 mV, the low-side resistor $R_2$ is calculated to the following value

$$R_2 = \frac{V_{BOon}}{I_{biasLL}} = \frac{0.8}{16\ \mu} \approx 50\ k\Omega \qquad \text{(eq. 35)}$$

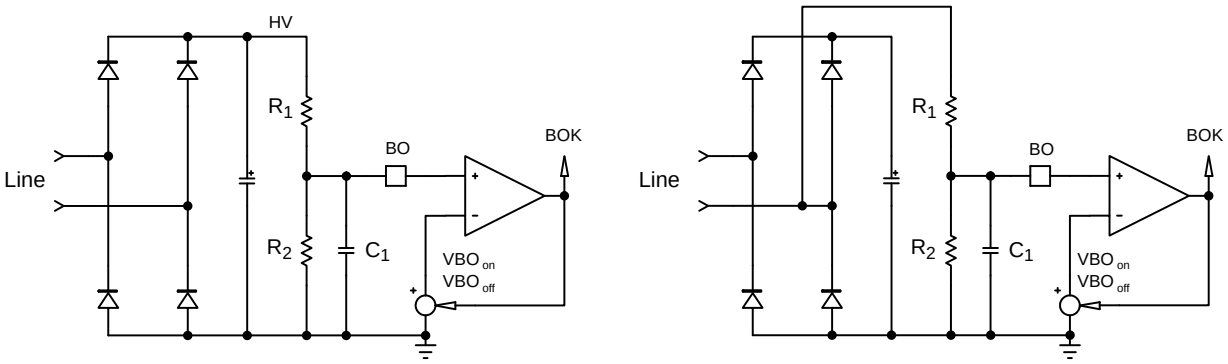



**Figure 31. There are Several Possibilities to Sense the Input Mains**

Assume a turn-on voltage of 113 V dc or 80 V rms input (neglecting the diodes $V_f$), then the upper resistor is

$$R_1 = \frac{V_{in,on} - V_{BOon}}{I_{biasLL}} = \frac{113 - 0.8}{16\ \mu} \approx 7\ M\Omega \qquad \text{(eq. 36)}$$

With this configuration, the bridge division ratio is evaluated to

$$k_{BO} = \frac{R_2}{R_1 + R_2} = \frac{50\ k}{50\ k + 7\ M} = 7.1\ m \qquad \text{(eq. 37)}$$

The 0.7-V $VBO_{off}$ will turn the converter off at

$$V_{in,min} = \frac{V_{BOoff}}{k_{BO}} = \frac{0.7}{7.1\ m} = 98.6\ V \qquad \text{(eq. 38)}$$

which correspond to an input line of roughly 70 V rms. Capacitor $C_1$ filters the ripple and makes sure it remains within the hysteresis window. This solution presents the disadvantage of having a turn-off voltage that is load-dependant: depending on the load condition, the bulk ripple will vary, severely affecting the turn-off level. The power dissipation is not that good either as the rectified input is sensed. Finally, as the BO pin is also used to reset the part in case it is latched, the bulk capacitor voltage will take time to go down and reset will be delayed. Despite its simplicity, this is not the solution of choice.

A second solution appears in the right-side of the figure where one of the mains branch is tested. This time, the sensed voltage is independent from the loading conditions, neglecting the drop brought by the EMI filter and the power cord. Capacitor $C_1$ filters the mains to generate an average value tested by the BO pin. If $C_1$ is a large value – thus assuming no ripple on the BO pin – you will have the largest hysteresis brought by the two BO levels, 0.8 and 0.7 V. For instance, should you calculate the divider network to turn the converter at 80 V rms, then the turn-off rms voltage would be (80 · (0.7 / 0.8) = 70 V). For most applications, this gap is acceptable.

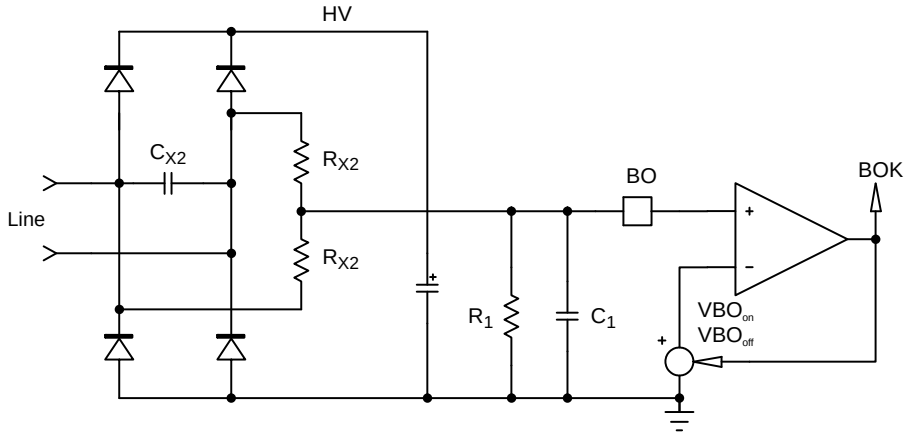



**Figure 32. In This Option, the Mains is Sensed via Two Resistors which also Serve as a X2 Capacitor Discharge Path**

Please note that brown-out measurements require care in the instruments setup. Any leakage current brought by equipments connected to the board will distort the turn on and off levels. When you test the BO levels, you have to remove all equipments linked to the board (oscilloscope probes for instance) and leave the secondary-side load only. We have seen cases where three different brown out levels were observed with three different ac sources while the oscilloscope ground was left connected. Once removed, all thresholds perfectly matched.

**Over Voltage Protection**

On top of the BO function, the pin offers a simple means to latch off the part with the help of a Zener diode. Figure 33 shows the recommended diagram. The internal latch-off level on the BO pin is 4.5 V. Should you need to protect the $V_{cc}$ excursion from a level above 21 V, then the Zener voltage must be selected at 21 − 4.5 = 16.5 V. A 16-V type will do the job if we include the 1N4148 forward drop. $R_1$ is selected to force a bias current in the Zener diode and improve the precision. A typical value of 1 kΩ can be selected. The OVP signal must be present 4 consecutive clock pulses to be validated.

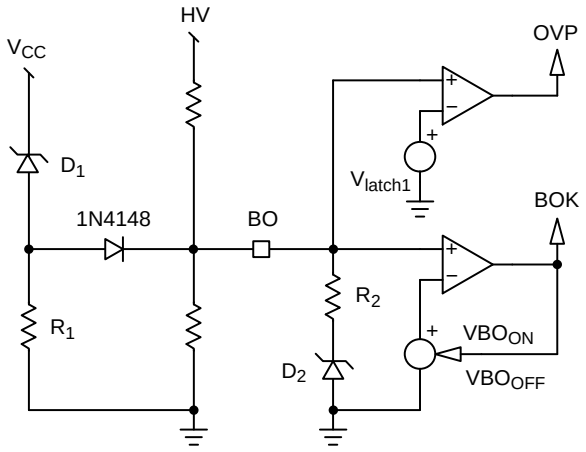



**Figure 33. The Zener Diode is Externally Biased to Improve Precision and False Tripping**

The BO is a high-impedance pin and we cannot afford to let spurious pulses (during surge tests for instance) false trip the OVP comparator. For this reason, internal diode $D_2$ and resistor $R_2$ lower the input resistance as $V_{BO}$ leaves its normal operating area, above 3.3 V typical. Below this level the input resistance is almost infinite (and does not perturb the BO operation) but above this value, the current increases, improving the converter noise immunity. Figure 34 graphs the BO input current versus the pin bias voltage.

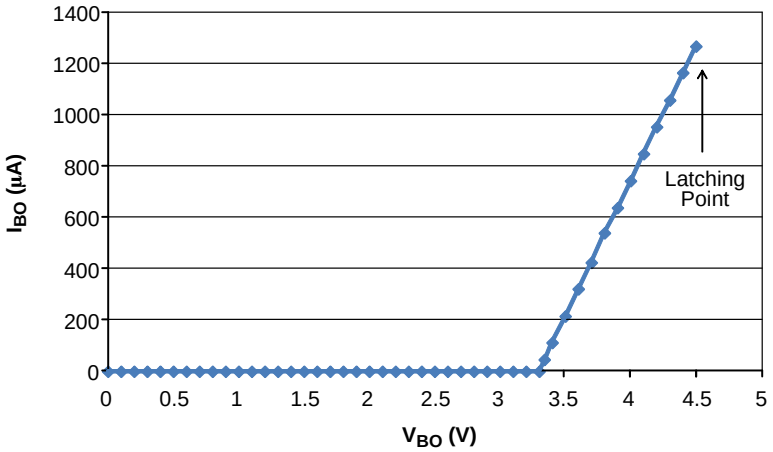



**Figure 34. The BO Pin Input Current Increases beyond a 3.3-V Bias Voltage to Improve Noise Immunity**

It is important to realize that if the latch voltage is the Zener diode breakdown level plus the internal 4.5-V threshold, the Zener will start conduct when $V_{cc}$ reaches its breakdown voltage. In normal input/output conditions, if $V_{cc}$ increases because of a strong leakage inductance for instance, the voltage across $R_1$ in Figure 33 can increase and can potentially disturb BO thresholds. For this reason, the Zener voltage must always be selected lower than the maximum $V_{cc}$ along the converter loading range so that BO thresholds remain unaffected.

A possibility also exists to connect $D_1$'s cathode in Figure 33 to the auxiliary winding via a BAV21 and, if necessary, with a small RC filter as shown in Figure 22. In this configuration, the leakage contribution is reduced.

### Latching the Controller from the Secondary Side

There are some cases where the observation of the auxiliary $V_{cc}$ does not deliver the required precision. In this case, it is possible to monitor the secondary side output voltage and bring the information on the primary side via an optocoupler. A resistor $R_1$ installed in series with the optocoupler collector limits the injected current in the BO pin when the OVP event occurs. The resistor must be sized to limit the peak current below 5 mA.

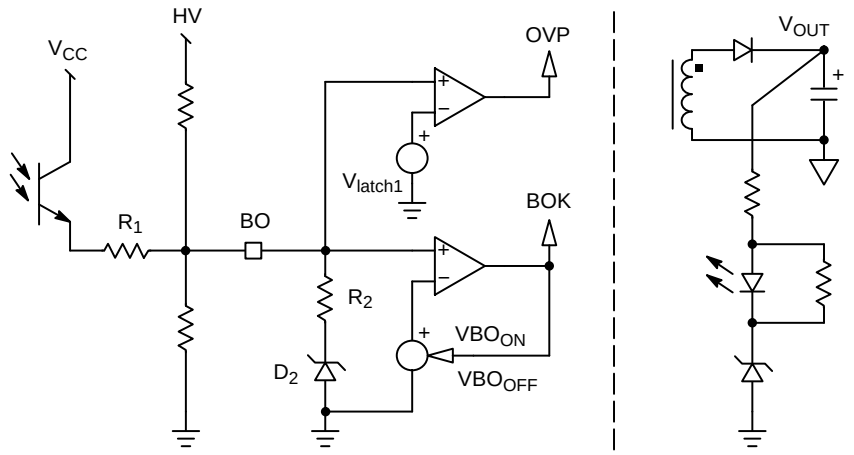



**Figure 35. Latching Off the Controller from the Secondary Side is Easy**

### Conclusion

This application note describes how a controller housed in a TSOP6 package can offer the flexibility and ease of use usually found in much larger packages. With its extended jittering capability and a combined brown-out and OPP circuitry, the NCP1256 represents a serious candidate in designs where ease of implementation and cost sensitivity are two important variables.



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