AND9208/D

Standby Power Performance of NCP1256

ON Semiconductor®

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APPLICATION NOTE

The NCP1256 has been optimized to improve converter efficiency in light−load conditions but also in no−load situations. By reducing internal bias currents as output power goes down, the part consumption decreases significantly, allowing extremely low standby power consumption figures despite the absence of high−voltage start−up current source. When brown−out sensing takes advantage of the X2 discharge resistors, the part gives excellent results as we will see.

Sources of Power Waste – Primary Side

A low−voltage die such as in NCP1256 needs energy to start−up and crank the power supply. This energy usually comes from the input mains and is stored into the V_{cc} capacitor for starting up. Several tens of milliseconds after the capacitor voltage hits the controller turn−on voltage, an auxiliary winding takes over and self−supplies the controller. A typical solution is shown in Figure 1 where resistor R_1 forces a current I_1 from the high−voltage rail to charge capacitor CV_{cc}.

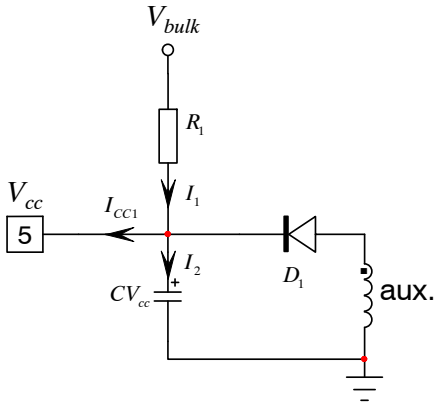


Figure 1. The Simplest Implementation to Start up the NCP1256 from the Bulk Voltage

The resistor current splits in I_2 for the capacitor but also in I_{CC1}, absorbed by the die until the V_{cc} turn−on voltage is reached. This I_{CC1} current has been reduced compared to the existing NCP125x family and is now specified at 10 μA (max) along the whole temperature range. Assume you want a start−up time less than 1.5 s at the lowest input voltage, 85 V rms. The V_{cc} capacitor is 10 μF and the controller turn−on voltage is 20 V (max). How much current do you need from a 120 V bulk voltage? For the capacitor you must deliver

$$I_2 > \frac{\Delta V \cdot C_{Vcc}}{t} = \frac{20 \times 10u}{1.5} \approx 133\ \mu A \qquad \text{(eq. 1)}$$

To this value, you must add the IC own consumption of 10 μA, pushing I_2 to 145 μA with some margin. To deliver these 145 μA from the bulk rail, resistance R_1 must be of the following value

$$R_1 < \frac{120-20}{145u} = 690\ k\Omega \qquad \text{(eq. 2)}$$

Considering a normalized 680 kΩ resistance, a high−line dc level on the bulk capacitor of 375 V and a 14 V operating V_{cc}, then the power permanently dissipated is

$$P_d = \frac{(375-14)^2}{680k} \approx 191\ mW \qquad \text{(eq. 3)}$$

This value may be considered low depending on the performance you want to achieve. If you try to beat the 300 mW limit, you may have a chance to meet this number providing the converter's consumption is reduced at no load. If you now want to be way less than this value, there are several options:

1. Trade a slightly larger start−up time: by increasing the start−up time to 3 s, the charging current drops to 75 μA, the resistance becomes 1.3 MΩ and the dissipated power drops to 100 mW.
2. Decrease the V_{cc} capacitor to 4.7 μF. For instance, increasing a little the auxiliary winding turns ratio may improve the auxiliary V_{cc} take−over time and a 4.7 μF capacitor is enough to start up in all conditions. In this case, you approach values obtained with those obtained in point 1.

Besides excessive power dissipation, another drawback of this solution is the maintaining of V_{cc} a long time while the converter has been unplugged from the mains outlet. If the IC is latched and the user wants a quick reset, this solution lengthens the reset time quite significantly as V_{cc} does not immediately drop to its reset value.

A second possibility is to connect the start−up resistance to the input line directly. One of the bridge diode will ensure half−wave rectification and the rms voltage value across the resistance will be significantly reduced to the benefit of the dissipated power. Figure 2 represents this solution widely implemented in ac−dc adapters.

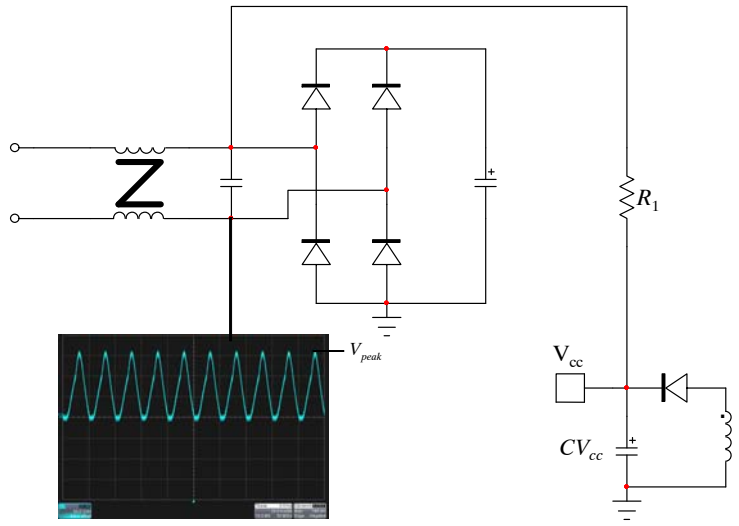


Figure 2. Connecting the Start−up Resistor to the Half−wave reduces the Dissipated Power Budget on R_1

The approximate calculation of R_1 in this case slightly varies. Neglecting the 10 μA I_{CC1} consumption, the resistor value can be determined using

$$R_1 = \frac{t_{start}}{C_{V_{cc}} \ln\left(\frac{V_{pLL}}{V_{pLL} - \pi V_{CC(on),max}}\right)} = \frac{1.5}{10u \cdot \ln\left(\frac{120}{120 - \pi \cdot 20}\right)} = 202\ k\Omega \quad \text{(eq. 4)}$$

With this value on hand, the dissipated power is more complicated to calculate as we need the rms voltage across the load resistor

$$V_{rms} = \sqrt{\frac{1}{T_{line}} \int_0^{\frac{T_{line}}{2}} \left(V_{pHL} \sin(\omega t) - V_{cc}\right)^2 dt} \quad \text{(eq. 5)}$$

If we neglect the V_{cc} contribution at the highest line level, this equation can be replaced by

$$P_{R_1} \approx \frac{V_{pHL}^2}{4R_1} \quad \text{(eq. 6)}$$

In this case, the power dissipated by R_1 when connected in a half−wave configuration slightly decreases to

$$P_d = \frac{V_{R_1,rms}^2}{R_1} = 158\ mW \quad \text{(eq. 7)}$$

If the start−up time is relaxed to 2.9 s while the V_{cc} capacitor is reduced to 4.7 μF, then R_1 becomes a 832 kΩ resistor and dissipates 38 mW at high line. Figure 3 shows the dissipated power between a direct bulk connection and the half−wave connection for a 4.7 μF capacitor. Should you reduce the capacitor to 2.2 μF, then the half−wave connection shows greater improvement versus the bulk solution. The picture shows component values computed for a 2.9 s start−up time.

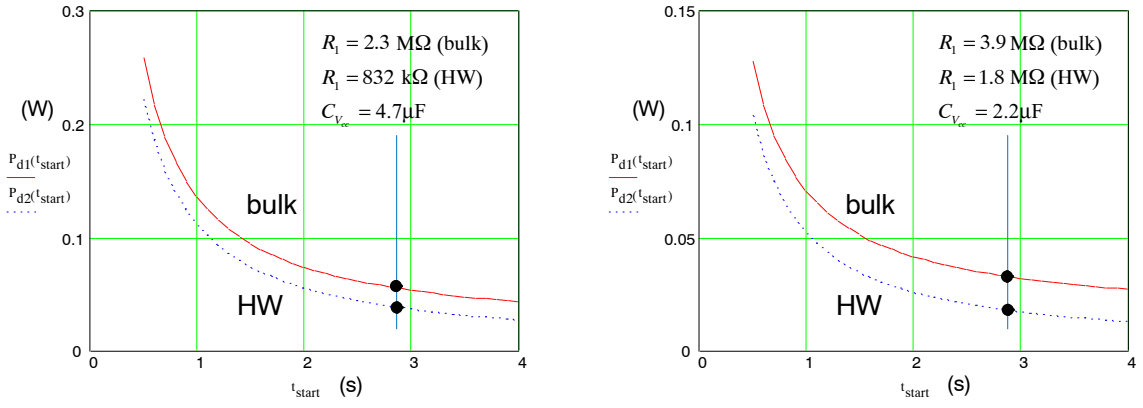


Figure 3. The Half−wave Connection helps reduce the Dissipated Power for longer Start−up Times

These numbers and curves are pure theoretical numbers considering a nice half−wave sinusoid biasing the upper end of the start−up resistor. In reality, during start up, the bridge diodes conducts a very small amount of time, especially when the bulk capacitor is fully charged and the controller is still not cranked. The current charging the V_{cc} capacitor is thus mainly provided by parasitic capacitances in the diodes. Therefore, the values we gave in the above graphs have to be cautiously considered and practical implementation results may differ quite a bit. You will see in the next section how measurements can be affected by the bench setup.

Capacitive Start Up

To further reduce the start−up network contribution, a possible solution uses high−voltage capacitors. The circuit takes advantage of series capacitors impedances at the 50 Hz line frequency which do not dissipate power. A typical implementation appears in Figure 4 with waveforms captured during the start−up sequence. The total current delivered by the two series capacitors of equal value, C_1 and C_2, can be approximated by

$$I_{tot} \approx 2V_p \cdot C \cdot F_{line} = 2V_pC_1F_{line} \quad \text{(eq. 8)}$$

If we consider 4.7 nF capacitors and considering a 10 μA current absorbed by the controller at start up, then the current charging the V_{cc} capacitor for a 85 V rms input voltage approximates to

$$I_{tot} \approx 2 \times 120 \times 4.7n \times 50 - 10u \approx 46\ \mu A \quad \text{(eq. 9)}$$

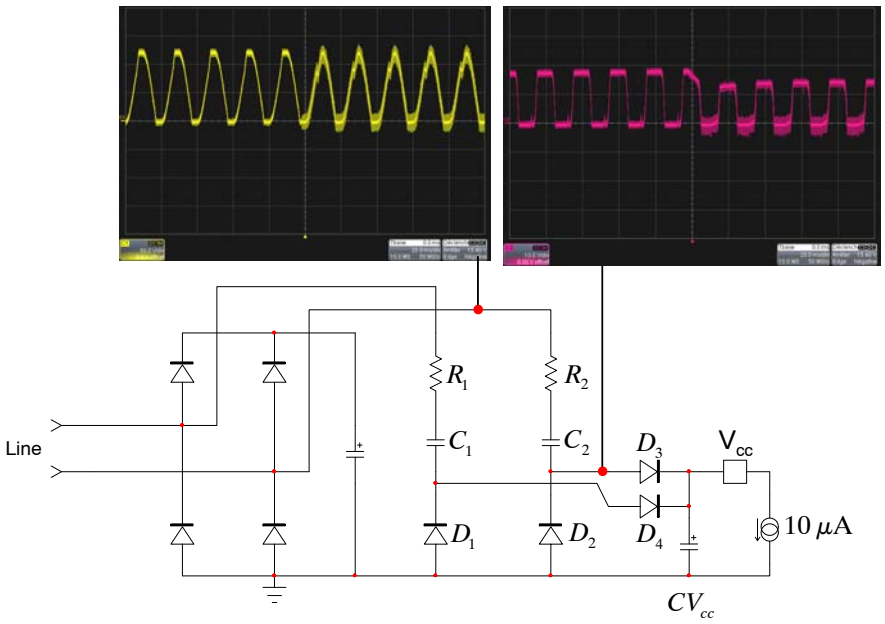


Figure 4. A Capacitive Start up involves two High−voltage Capacitors dropping the Line Voltage at a very Low Dissipation Cost

The capacitors must be of high−voltage types to survive input surges. This solution is interesting in case you need to meet extremely stringent standby power criteria.

Measuring Start−Up Time

The start−up time is the time measured from the moment the mains is applied to the time the feedback loop is closed, confirming V_{out} is on target. Practically, start−up time is often considered from the moment the V_{cc} capacitors takes off from 0 V to the point where the controller starts switching. The few tens of ms needed to close the loop are usually negligible if you target start−up times below 3 s at the lowest input line (for notebook adapters for instance). However, the measurement can sometimes be tricky, especially if you implement the half−wave configuration shown in Figure 2. In theory, the waveform driving the resistor should be a nice half−wave sinusoid. In reality, the circulating current depends mostly on the diodes parasitic capacitances and heavily varies with the various leakages. If you connect an oscilloscope ground clip while running the measurement, you may distort the result by introducing a parasitic circulating current. The situation may vary depending on the setup: how does this ac source leaks to earth, how these currents circulate when the oscilloscope ground clip is connected etc. We have example where the ac source is turned off from the front panel and with only one single wire connected to the source outlet, the V_{cc} capacitor swings up and down, solely driven by the leak.

To avoid this problem, we recommend operating the board without any connection to measuring instruments or even an electronic load. If you can load the converter with a simple power resistor, this is the best situation as shown in Figure 4. The input line current is monitored by a current probe. When you power the board, usually 85 V rms, there is a sharp spike (in−rush current) then a quite period (the

bulk capacitor is charged to the peak input) and then current again, testifying of operations. The time between the in−rush detection and the current activity is the start−up time (neglecting V_{out} rising up to target). By triggering the oscilloscope when the in−rush current occurs, you record the start−up sequence the proper way. Configurations involving the capacitive start−up and the direct bulk connection are less sensitive to leaks. Before powering the board, make sure all capacitors (V_{cc}, bulk and brown−out) are fully discharged.

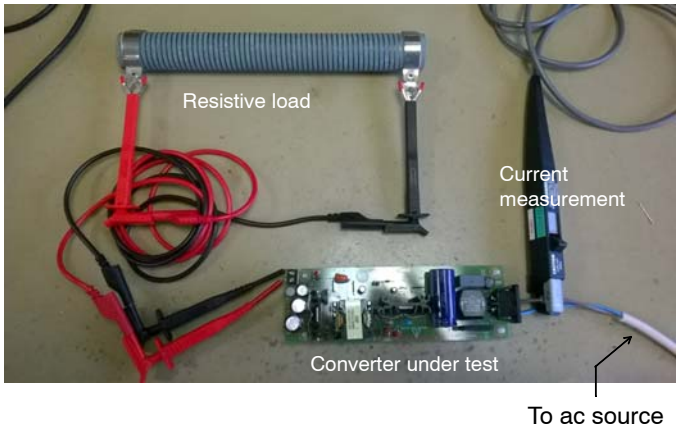
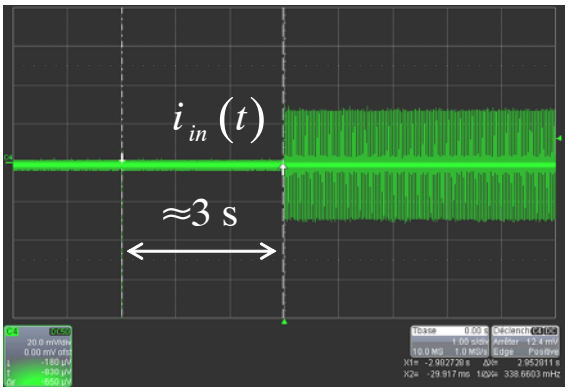


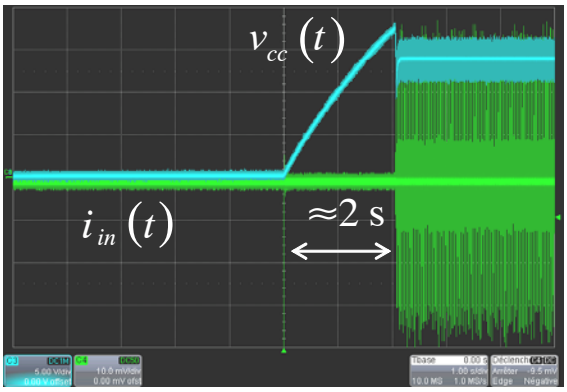
Figure 5. To Avoid any possible Leakage Issues, it is best to Test the Start−up Sequence with a fully Isolated Converter, not connected to a Measuring Instrument or grounded via an Oscilloscope Probe

We have gathered a few sequences and compared results obtained when monitoring V_{cc} and using Figure 5 test fixture. The V_{cc} capacitor is 4.7 μF and we calculated with (eq.4) a start−up resistance of 832 kΩ (normalized to 820 kΩ) for the half−wave connection and 2.3 MΩ for the bulk connection (adjusted to 2.9 MΩ). The target start−up time is around 3 s at the lowest input, 85 V rms.

In Figure 6, the start−up time evaluated using the in−rush current as a trigger signal gives 3 s. If we connect the (isolated) oscilloscope ground, the start−up time is reduced to 2 s, giving you the assumption that you can increase the start−up resistor further to save losses.



V_{in} = 85 V rms, R_{HW} = 820 kΩ



V_{in} = 85 V rms, R_{HW} = 820 kΩ

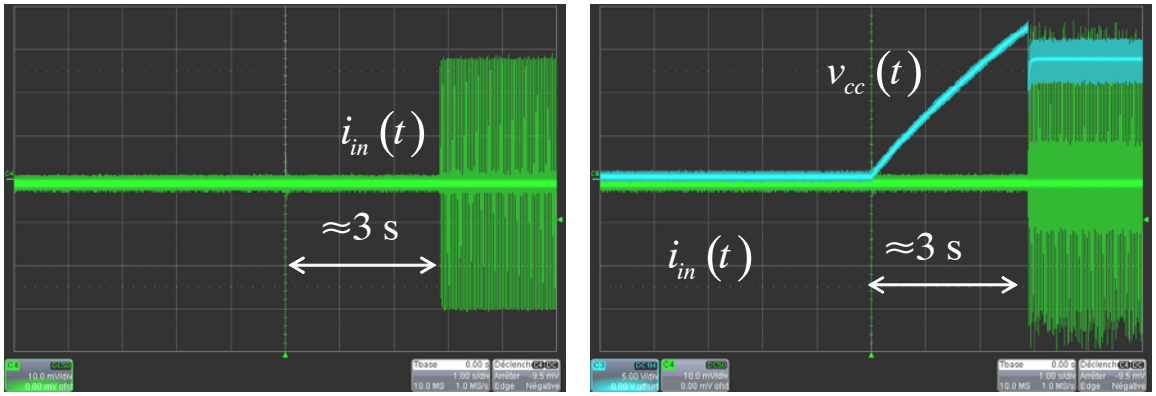
Oscilloscope ground is connected

Figure 6. The Half−wave Configuration can be Sensitive to a Leaky AC Source as shown in the Right Shot. The V_{cc} Capacitor is 4.7 μF

In Figure 7, the V_{cc} capacitor is charged via a resistor connected to the bulk this time. Its value is adjusted to match the 3 s start−up time obtained from the half−wave connection. We have 3 s as expected and the ground connection does not bother the sequence. Finally, in Figure 8, the capacitor is charged with the capacitive start−up circuit and shows an improved start−up time. A 2 s start−up time with a 4.7 μF capacitor approximately translates to a charging current of

$$I_{charge} \approx \frac{4.7u \times 17.7}{2} \approx 42\ \mu A \qquad \text{(eq. 10)}$$

to which the controller start−up consumption is added (less than 10 μA) and it matches (eq.9) quite well.

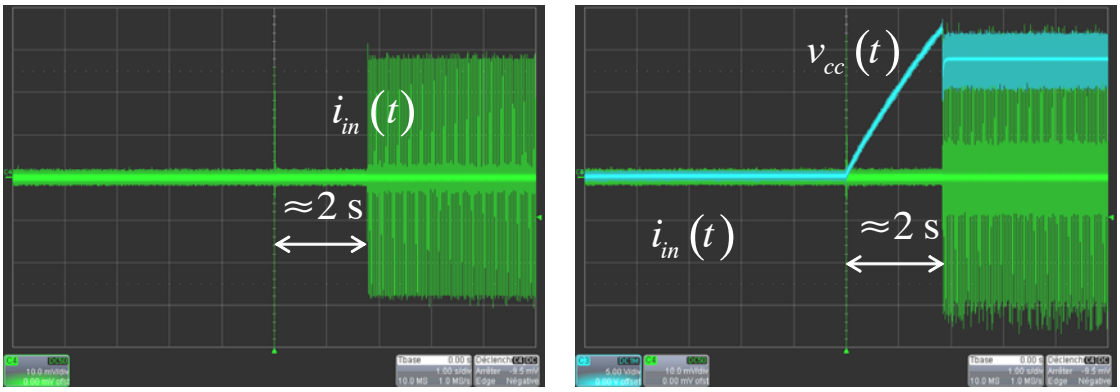


V_{in} = 85 V rms, R_{bulk} = 2.9 MΩ

V_{in} = 85 V rms, R_{bulk} = 2.9 MΩ

Oscilloscope ground is connected

Figure 7. When the Start−up Resistor is Connected to the DC Bulk Voltage, adding the Oscilloscope Ground does not bother the Measurement



V_{in} = 85 V rms, capacitive start−up

V_{in} = 85 V rms, capacitive start−up

Oscilloscope ground is connected

Figure 8. The Capacitive Start−up gives a slightly better Timing, allowing Cranking the Power Supply in 2 s at no extra Power Loss

The standby power is affected by the configuration choice. We have run no−load standby power measurements with the three options in a 60 W NCP1256−based adapter powered from a 230 V rms source. The results are below:

P_{in} = 58 mW HW
P_{in} = 63 mW bulk
P_{in} = 34 mW capacitive network

The HW offers good results but not so far from the bulk connection. Best results are actually obtained with the capacitive start−up network.

Controller Consumption

Ensuring the lowest standby power implies chasing milliwatts everywhere on the converter board. One source of consumption is obviously the controller itself. To excel in the low−standby power arena, the NCP1256 has been the object of special care when designing its internal circuitry. In particular, numerous bias currents are purposely reduced when standby power mode is entered. Figure 9 shows data collected in the demonstration board while the 1256 drove a 600 V / 10 A power MOSFET. The board is operated and delivers a 19 V output whose loading conditions are changed. When the load is removed, the IC consumption drops to slightly less than 400 μA which, together with a 12 V V_{cc} level brings the controller contribution to less than 5 mW in standby.

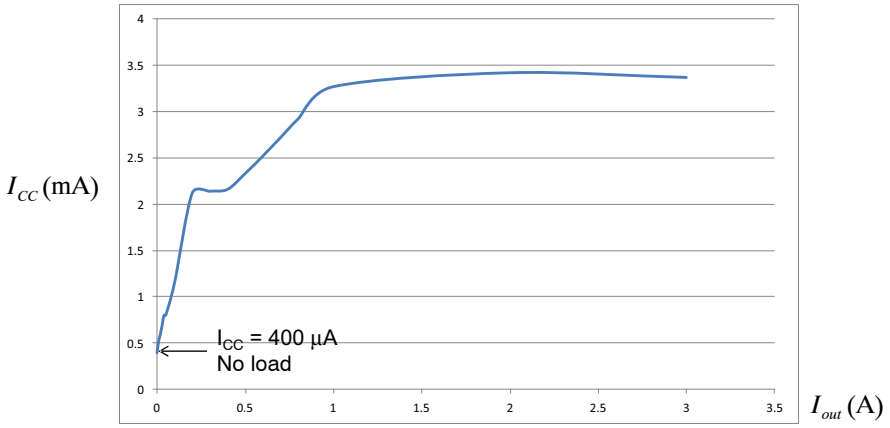


Figure 9. Reducing Internal Bias Currents as Pout goes down helps improving the Controller Consumption in Light− or No−Load Situations

Needless to underline the role of this static consumption when you chase milliwatts on the board!

Brown−Out Sensing Network

The NCP1256 includes a brown−out pin letting you sense the input mains for safety purposes. Again, sensing a high−voltage input induces losses that will later play a role in the final standby power measurement. It is your interest to minimize the energy lost in this network. One possible option is to reuse the X2−discharge resistors installed on the converter board. These resistors are tailored so that the time constant involving the X2 capacitor and the resistors is less than 1 s. For instance, assuming a 0.22 µF capacitor, you must install an ohmic path across the capacitor of less than 4.5 MΩ. This network is useless in normal operation and only plays its role when the user unplugs the converter. Why not reusing these resistors to perform BO sensing? This is what Figure 10 suggests.

The configuration is very close to the half−wave start−up network presented in Figure 2. Therefore, connecting an oscilloscope probe to the circuit is likely to perturb operations, leading to wrong turn on and off voltages. Testing the BO levels in this mode can be done with a simple load resistance first and an electronic load later on. If you measure similar operating levels in either configuration, then the leak induced by the instrument is negligible. If you need to measure the level across R_1, a hand−held multimeter is the way to go with this configuration. At a 230 V rms input voltage, the power loss contributed by the 4 MΩ resistors is roughly equal to

$$P_{loss} \approx \frac{V_{in}^2}{R_{X_2}} = \frac{230^2}{4Meg} = 13\ mW \qquad \text{(eq. 11)}$$

This configuration represents the best tradeoff between component count and standby power performance.

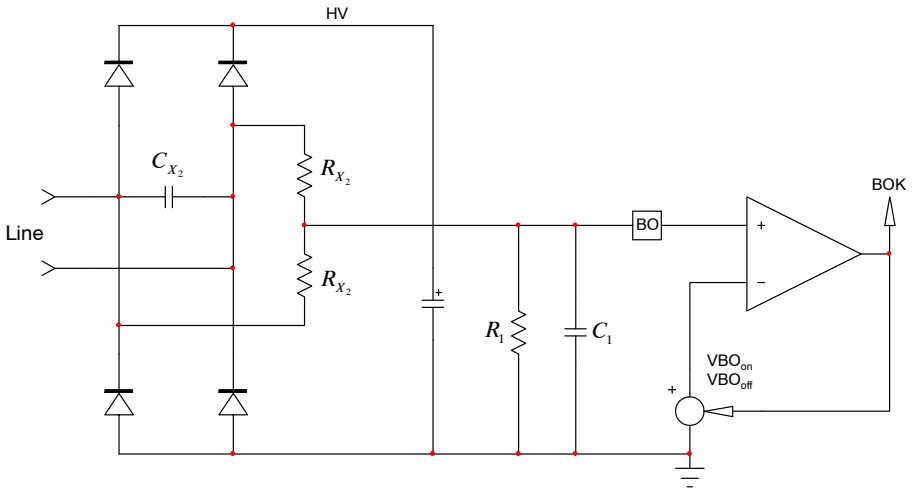


Figure 10. Using the X2 Resistors is a Possibility to Build the BO Function at no extra Power Cost

Sources of Power Waste – Secondary Side

The loss in the secondary side depends on several factors, mainly dc bias currents flowing in the control circuitry. Figure 11 shows the split of these contributions in a classical TL431−based control circuit.

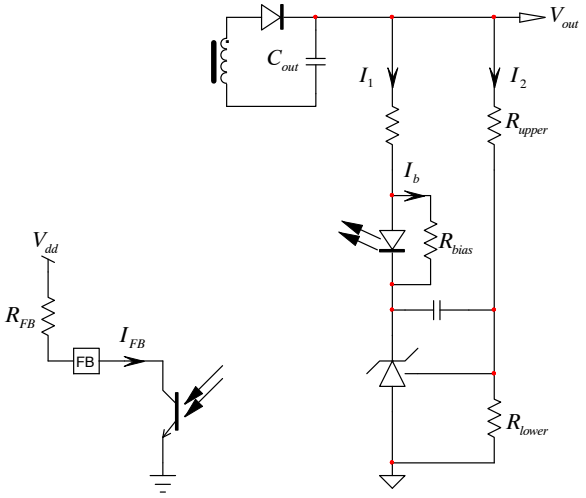


Figure 11. The Secondary−side Control Circuit in a Switching Converter is a Source of Loss that must be considered when Looking for Milliwatts

In the primary side, the feedback current in the worst case, I_{load} = 0, is equal to

$$I_{FB} = \frac{V_{dd} - V_{skip}}{R_{FB}} \quad \text{(eq. 12)}$$

In the NCP1256, the feedback resistor is 30 kΩ and the internal V_{dd} is 5.5 V. The part skips cycles for a feedback voltage below 0.6 V. The maximum feedback current is thus obtained in a no−load condition where the part skips cycle. This current is thus equal to

$$I_{FB} = \frac{5.5 - 0.6}{30k} \approx 163\ \mu A \quad \text{(eq. 13)}$$

This current is reflected to the secondary side via the optocoupler current transfer ratio (CTR):

$$I_{LED} = \frac{I_{FB}}{CTR} \quad \text{(eq. 14)}$$

The optocoupler CTR heavily depends on the collector current. For currents such as a few hundred of micro−amperes as in (eq.13), the CTR can degrade down to 20−30% easily. A popular SFH615A−2 optocoupler will show a CTR of 25% when the converter works in standby. The 163 μA is thus accordingly increased to

$$I_{LED} = \frac{163u}{0.25} \approx 652\ \mu A \quad \text{(eq. 15)}$$

If you account for the 1 mA bias current I_b necessary to bias the TL431, we end up with a total current equal to 1.65 mA. Multiplied by the 19 V output voltage, it contributes to a power loss of

$$P_{loss} = 19 \times 1.65m \approx 124\ mW \quad \text{(eq. 16)}$$

A way exists to further lower this contribution: select higher−CTR optocouplers such as SFH615A−4 for instance. In this case, the LED current drops to

$$I_{LED} = \frac{163u}{0.43} \approx 379\ \mu A \quad \text{(eq. 17)}$$

Selecting another type of optocoupler, the FOD817S, the CTR increases to 75% and the LED current is even lower

$$I_{LED} = \frac{163u}{0.75} \approx 217\ \mu A \quad \text{(eq. 18)}$$

However, keep in mind that high−CTR optocouplers are usually slower than their low−CTR counterparts. If you decide to upgrade the optocoupler to gain in standby power, do not forget to either characterize the new optocoupler pole or test the loop gain with the newly−installed component. A quick load transient step can reveal an abnormality if needed as shown in Figure 12: the loop response is slower in the right side and the undershoot slighty more pronounced.

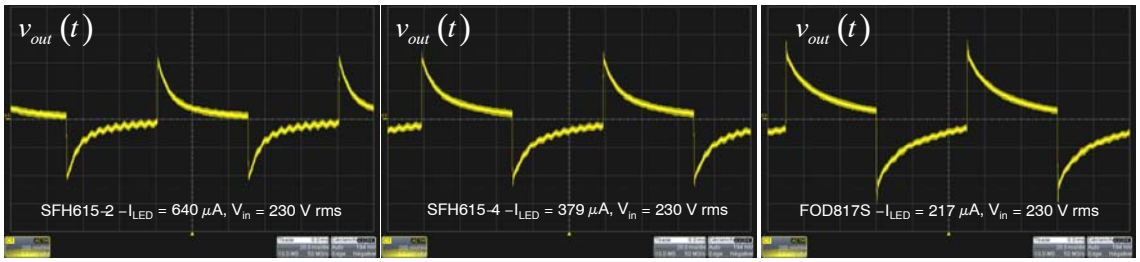


Figure 12. A Transient Step with different Optocouplers can reveal a Reduced Phase Margin or Crossover when a High−CTR Optocoupler is installed

The below numbers show the improvements brought by upgrading the optocoupler CTR (capacitive start−up network):

P_{in} = 47 mW SFH615A−2
P_{in} = 42 mW SFH615A−4
P_{in} = 34 mW FOD817S

Reducing the TL431 Bias Contribution

With a minimum operating current of 1 mA, the TL431 is a big piece of loss in (eq.16). Why keeping the bias in no−load standby power? Suppressing the bias will surely degrade the TL431 open−loop gain but this is not a big deal in a no−load situation. A possible ON Semiconductor proprietary bias suppression technique exists and is shown in Figure 13. The principle consists of building a peak rectifier with diode D_1 and capacitor C_1. You select C_1 so that the valley voltage decreases as the distance between switching pulses increases. When D_1 conducts, C_1's voltage peaks to V_{out} but quickly drops during the off−time because of R_1. As the valley level drops, so do the average voltage and the bias current: in deep skip−cycle conditions, the bias current has disappeared and power consumption is optimized. As the bias immediately comes back in case the load is reapplied, the transient response does not suffer.

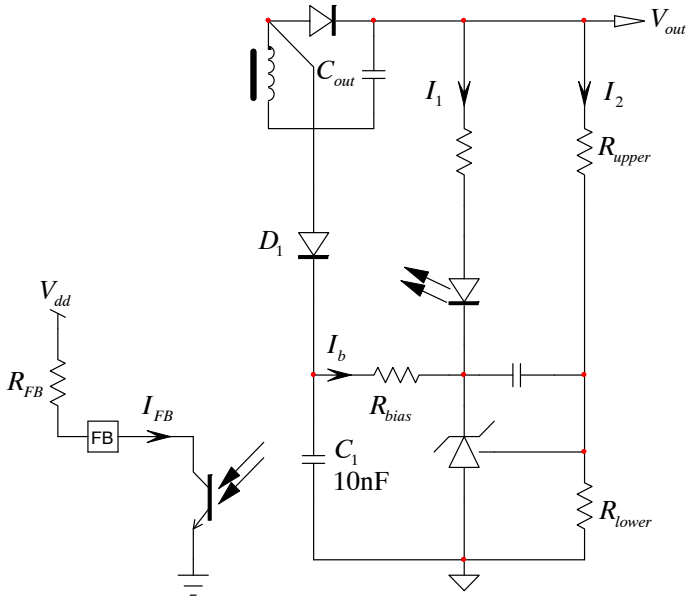


Figure 13. A Simple Peak Rectifier helps removing the Bias Current in a No−Load Situation

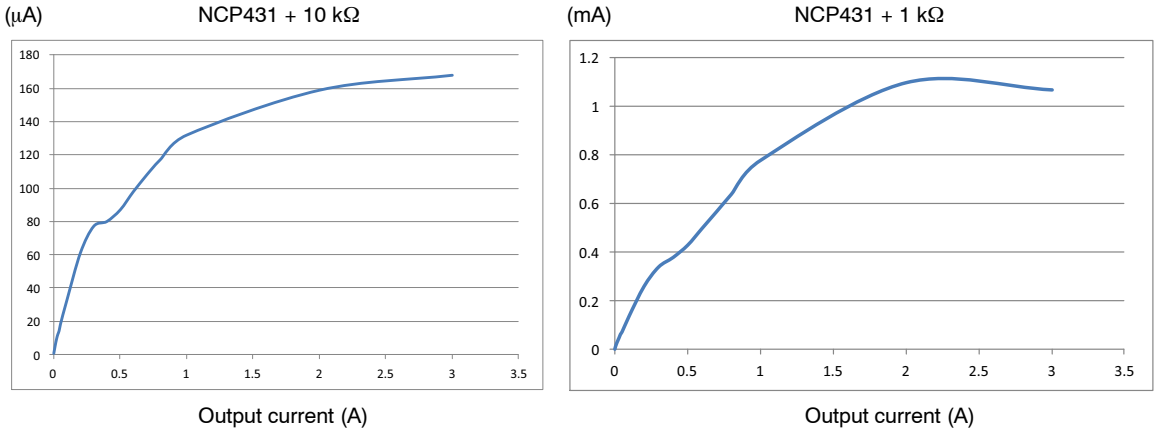


Figure 14. In Skip Cycle, the TL431 Bias disappears, nicely improving the Standby Figure in No Load

In Figure 14, you can see the bias current variations in relationship to the output current. The bias is maximal at full power which is good for the output impedance and the static error. As I_{out} decreases, the bias also goes down to completely disappear in no load. A 1 kΩ resistor provides 1 mA or so and is perfect for a TL431 (1 mA minimum bias current). In case a lower bias is wanted, a NCP431 will be the right candidate (40 μA minimum bias current) together with a 10 kΩ resistor.

Increasing the Output Voltage Sensing Network

The sensing network made of R_{upper} and R_{lower} in Figure 13 is permanently connected to the output voltage. In a 19 V adapter, the bias current can be a significant source of loss and must be monitored. This current is equal to

$$I_{R_{upper}} = \frac{V_{out} - V_{ref}}{R_{upper}} \quad \text{(eq. 19)}$$

and induces a loss of

$$P_d = I_{R_{upper}} \cdot V_{out} \quad \text{(eq. 20)}$$

This current splits into the TL431 input circuitry (5.2 μA max at 25°C for the C version) and R_{lower}. If we select a bridge current in which the TL431 bias can be neglected, we can write

$$I_{R_{upper}} \approx \frac{V_{out}}{R_{lower} + R_{upper}} \quad \text{(eq. 21)}$$

A strong bias current is desirable to strengthen the control section noise immunity. However, it goes against a good standby power performance. In previous designs, we arbitrarily selected a 10 kΩ R_{lower} resistance for a 250 μA bias current. With a 19 V output, the permanent consumption was

$$P_d = 19 \times 250u \approx 4.8\ mW \quad \text{(eq. 22)}$$

most likely seen on the primary side by an extra 10 mW consumption.

To reduce this power budget, we will divide it by two in the next steps. Assume a 113 μA bias current with a 2.5 V reference voltage. The lower side resistor is thus equal to

$$R_{lower} = \frac{V_{ref}}{I_{bias}} = \frac{2.5}{113u} \approx 22\ k\Omega \quad \text{(eq. 23)}$$

The upper−side component is thus selected as

$$R_{lower} = \frac{V_{out} - V_{ref}}{I_{bias}} = \frac{19 - 2.5}{113u} = 146\ k\Omega \quad \text{(eq. 24)}$$

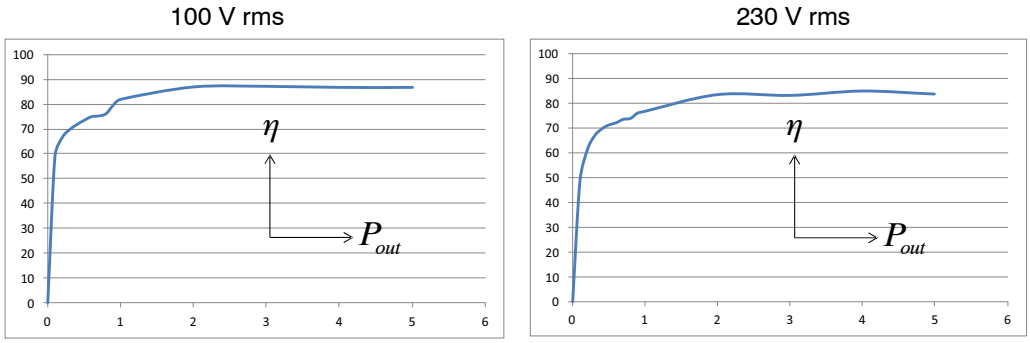
With this bridge value, (eq.22) reduces to

$$P_d = 19 \times 113u \approx 2.15\ mW \quad \text{(eq. 25)}$$

which is another step towards the lowering of the secondary−side power loss in standby.

Performance of the NCP1256 Evaluation Board

The below charts show the efficiency performance of the NCP1256 demonstration board (60 W/19 V) when loaded from 5 W to 0 W at low and high line. It uses the capacitive start−up network and a SFH615A−4 optocoupler. Please note the measurement results with a LED kept on at all times (≈10 mW load), they are excellent and compete against other higher pin count controllers featuring high−voltage capabilities.



P_{in} no-load:

21 mW – 100 V rms
41 mW – 230 V rms

P_{in} 10-mW LED on:

46 mW – 100 V rms
55 mW – 230 V rms

P_{out}	P_{in} (100 V)	P_{out}	P_{in} (230 V)
0.6 W	0.8 W	0.6 W	0.83 W
0.5 W	0.68 W	0.5 W	0.7 W
0.4 W	0.56 W	0.4 W	0.58 W
0.3 W	0.43 W	0.3 W	0.45 W
0.2 W	0.3 W	0.2 W	0.33 W

NCP1256 – 65 kHz – SFH615A-4 – capacitive startup

Figure 15. Excellent Performance of the NCP1256 in Light− to No−Load Situations

Conclusion

This application note investigates the sources of loss in a switching converter operated with a low−voltage controller such as NCP1256. Carefully taking care of these losses and working towards their reduction helps meeting excellent standby power figures as testified by practical measurements.

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