AND9176/D

Designing a Quasi-Resonant Adaptor Driven by the NCP1339

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APPLICATION NOTE

Quasi-square wave resonant converters also known as Quasi-Resonant (QR) converter are widely used in the adaptor market. They allow designing flyback Switched-Mode Power Supply (SMPS) with reduced Electro-Magnetic Interference (EMI) signature and improved efficiency. However, a major drawback of the structure is that the frequency can become dramatically high at light load.

In traditional QR converters, the frequency is limited by a frequency clamp. But, when the switching frequency of the system reaches the frequency clamp limit, valley jumping occurs: the controller hesitates between two valleys resulting in an instable operation and noise in the transformer at medium and light output loads.

In order to overcome this problem, the NCP1339 features a proprietary “valley lockout” circuit: the switching frequency is decreased step by step by changing valley from valley n to valley (n+1) as the load decreases. Once the controller selects a valley, it stays locked in this valley until the output power changes significantly. This technique extends the QR operation of the system towards lighter loads without degrading the efficiency.

In addition, in order to limit the stand-by consumption, the NCP1339 integrates an HV current source that charges the V_{CC} capacitor during start-up phase and an automatic X2-capacitor discharge circuitry that saves the need for power-consuming discharge resistors across the front-end filtering capacitors.

This application note focuses on the design of an adapter driven by the NCP1339.

The equations developed are further used to design a 45-W adapter.

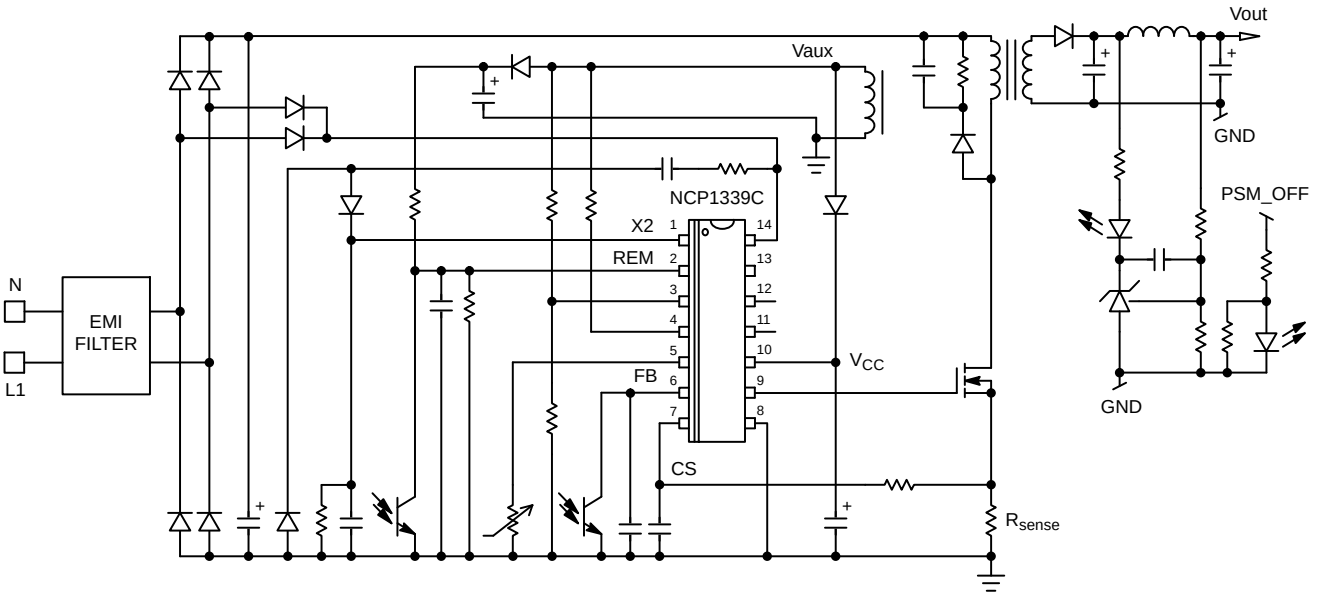

Figure 1. Application Schematic

INTRODUCTION

The NCP1339 implements a standard quasi-resonant current-mode architecture. This component represents the ideal candidate where low part-count and cost effectiveness are the key parameters, particularly in low-cost ac-dc adapters, open-frame power supplies etc. The NCP1339 brings all the necessary components normally needed in modern power supply designs, bringing several enhancements such as non-dissipative OPP, brown-out protection or sophisticated frequency reduction management for an optimized efficiency over the power range. Accounting for the new needs of extremely low standby power requirements, the part includes an automatic X2-capacitor discharge circuitry which can save the power-consuming resistors otherwise needed across the front-end filtering capacitors. The controller is also able to enter Power Savings Mode (PSM) that is, a deep sleep mode via its dedicated remote (“REM”) pin.

- ***High-Voltage Start-Up:*** low standby power results cannot be obtained with the classical resistive start-up network. In this part, a high-voltage current-source provides the necessary current at start-up and turns off afterwards.
- ***Internal Brown-Out Protection:*** the bulk voltage is internally sensed via the high-voltage pin monitoring (pin 14). When V_{pin14} is too low, the part stops pulsing. No re-start attempt is made until V_{pin14} recovers its normal range. At that moment, the brown-out comparator sends a general reset to the controller (de-latch occurs) and authorizes to re-start.
- ***X2-Capacitors Discharge Capability:*** per IEC-950 standard, the time constant of the front-end filter capacitors and their associated discharge resistors must be less than 1 s. This is to avoid electrical stress when users unplug the converter and inadvertently touch the power cord terminals. The circuitry for discharging the X2 capacitors can save the need for discharge resistors, helping to further save power.
- ***PSM Control:*** a dedicated pin allows the IC to enter a deep sleep mode when the REM input pin is brought above a certain level. This option offers an efficient means to operate the adapter in a power savings mode and draw the least input power from the mains in this mode. When the REM is actively pulled down via a dedicated optocoupler, the adapter immediately re-starts. The component that controls PSM is then active in normal operation (active-ON) and OFF in PSM (wasting no energy).
- ***Quasi-Resonant, Current-Mode Operation:*** QR operation is an efficient mode where the MOSFET turns on when its drain-source is at the minimum (valley). However, at light load, the switching frequency tends to get high. The NCP1339 valley lock-out and frequency foldback technique eliminate this drawback so that the efficiency remains at the highest over the power range.
- ***Valley Lockout:*** a continuous flow of pulses is not compatible with no-load/light-load standby power requirements. To excel in this domain, the controller observes the feedback pin voltage (FB) and when it reaches a level of 1.4 V, the circuit enters a valley lockout mode where the circuit skips a valley. If FB further decreases, more valleys are skipped until 6th valley is reached.
- ***Frequency Fold-Back:*** if FB continues declining and reaches 0.8 V, the current setpoint is frozen to V_{freeze} and the circuit regulates by modulating the switching frequency until it reaches 25 kHz (typically).
- ***Skip Cycle:*** to avoid acoustic noise, the circuit prevents the switching frequency from decaying below 25 kHz. Instead, the circuit contains the power delivery by entering skip cycle mode when the system would otherwise need to further lower the switching frequency below 25 kHz.
- ***Internal OPP (Over Power Protection):*** by routing a portion of the negative voltage present during the on-time on the auxiliary winding to the OPP pin (pin 3), the user has a simple and non-dissipative means to alter the maximum current setpoint as the bulk voltage increases. If the pin is grounded, no OPP compensation occurs.
- ***Internal Soft-Start:*** a 4-ms soft-start precludes the main power switch from being stressed upon start-up. It is activated whenever a startup sequence occurs including autorecovery hiccup.
- ***Fault Input:*** the NCP1339 includes a dedicated fault input (pin 5). It can be used to sense an overvoltage condition and latch off the controller by pulling up the pin above the upper fault threshold, $V_{Fault(OVP)}$, typically 3.0 V. The controller is also disabled if the Fault pin voltage, V_{Fault}, is pulled below the lower fault threshold, $V_{Fault(OTP\_in)}$, typically 0.4 V. The lower threshold is normally used for detecting an overtemperature fault (by the means of an NTC).
- ***Short-Circuit/Overload Protection:*** short-circuit and especially overload protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). Here, every time the internal 0.8-V maximum peak current limit is activated (or less when OPP is used), an error flag is asserted and a 160-ms timer begins counting. When the timer has elapsed, the fault is validated. Please note that the NCP1339C offers an low duty-cycle (< 10%), auto-recovery mode.

SPECIFICATIONS OF THE ADAPTER

In order to illustrate this application note, a 19-V, 45-W adapter will be the design example. The specifications are detailed in Table 1.

The experimental results of the 45-W adapter are detailed in the evaluation board user's manual EVBUM2248 [1].

For details concerning the QR transformer calculation, you can refer to the tutorial TND348 [2].

Table 1. SPECIFICATIONS OF THE 19-V, 45-W ADAPTER

Parameter	Symbol	Value
Minimum Input Voltage	$V_{in,min}$	85 Vrms
Maximum Input Voltage	$V_{in,max}$	265 Vrms
Output Voltage	V_{out}	19 V
Nominal Output Power	$P_{out(nom)}$	45 W
Switching Frequency at $V_{in,min}$, $P_{out(nom)}$	F_{sw}	45 kHz
Maximum Startup Time	$T_{startup}$	< 1 s

PREDICTING THE SWITCHING FREQUENCY

As the controller changes valley as the load decreases, the switching frequency of the power supply is naturally limited by the valley lockout. But equations are needed to predict the switching frequency evolution with respect with the output power.

The datasheet gives the FB thresholds at which the controller transitions from valley n to valley (n+1), P_{out} falling and at which the controller transitions from valley (n+1) to valley n, P_{out} rising.

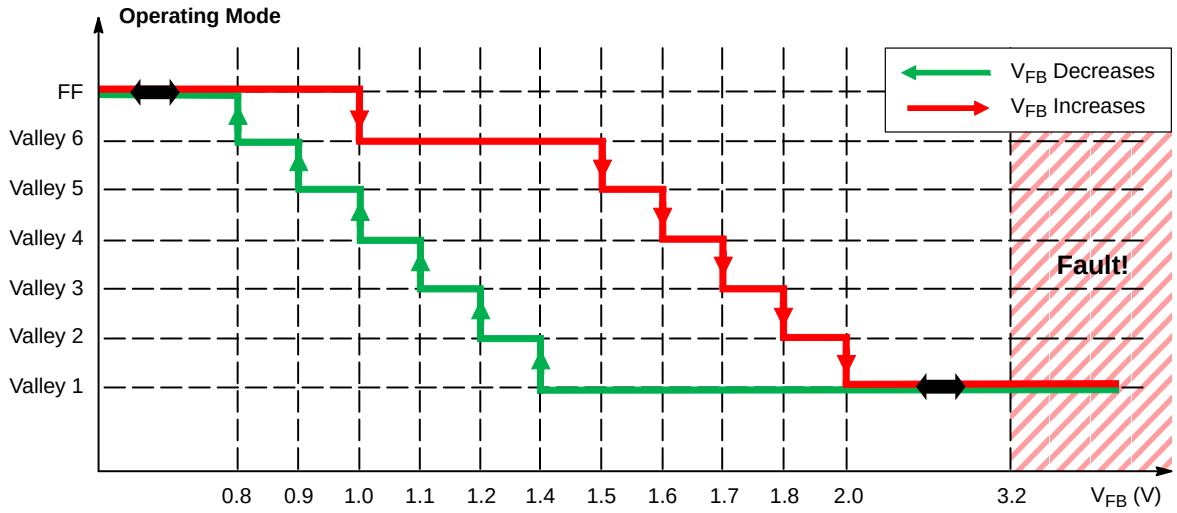

Figure 2. Operating Valley According to FB Voltage

With these thresholds, we can calculate the maximum switching frequency inside each valley depending if the output power decreases or increases:

$$F_{SW} = \frac{1}{\left(\frac{V_{FB}}{4R_{sense}} + V_{in,rms} \cdot \sqrt{2} \cdot \frac{t_{prop}}{L_p}\right) \cdot L_p \cdot \left(\frac{1}{V_{in,rms} \cdot \sqrt{2}} + \frac{N_{ps}}{V_{out} + V_f}\right) + (2n - 1) \cdot \pi \cdot \sqrt{L_p \cdot C_{lump}}} \quad \text{(eq. 1)}$$

Where:

- V_{FB} is the FB threshold at which the controller changes valley
- R_{sense} is the sense resistor value
- $V_{in,rms}$ is the rms value of the input voltage
- t_{prop} is the propagation delay
- L_p is the primary inductance
- V_{out} is the output voltage
- V_f is the forward voltage drop of the output diode
- C_{lump} regroups all capacitances surrounding the drain node (MOSFET capacitor, transformer parasitics…). As a first approximation, the MOSFET drain-source capacitance C_{OSS} can be used instead of C_{lump}.

- *n* is an integer representing the operating valley: n = 1 for 1st valley, n = 2 for 2nd valley, n = 3 for 3rd valley and n = 4 for the 4th valley, n = 5 for 5rd valley and n = 6 for the 6th valley.
- N_{PS} is the N_S/N_P turns ratio where N_S and N_P respectively, are the secondary and primary number of turns.
- T_{prop} is the propagation delay between the moment when the MOSFET current exceeds the setpoint target and the actual MOSFET turn off.

The corresponding output power can be calculated using the traditional formula:

$$P_{out} = \frac{1}{2} L_p \cdot \left(\frac{V_{FB}}{4R_{sense}} + V_{in,rms} \sqrt{2} \frac{t_{prop}}{L_p} \right)^2 \cdot F_{sw} \eta \quad \text{(eq. 2)}$$

Using the previous equations, we can calculate the maxima of the switching frequency and the corresponding output power for our 45-W adapter.

In order to help the power supply designer, the previous equations have been entered inside a *Mathcad* spreadsheet that automatically predicts the evolution of the switching frequency as a function of the output power (Figure 3).

For more calculation details, please refer to the Mathcad file on website.

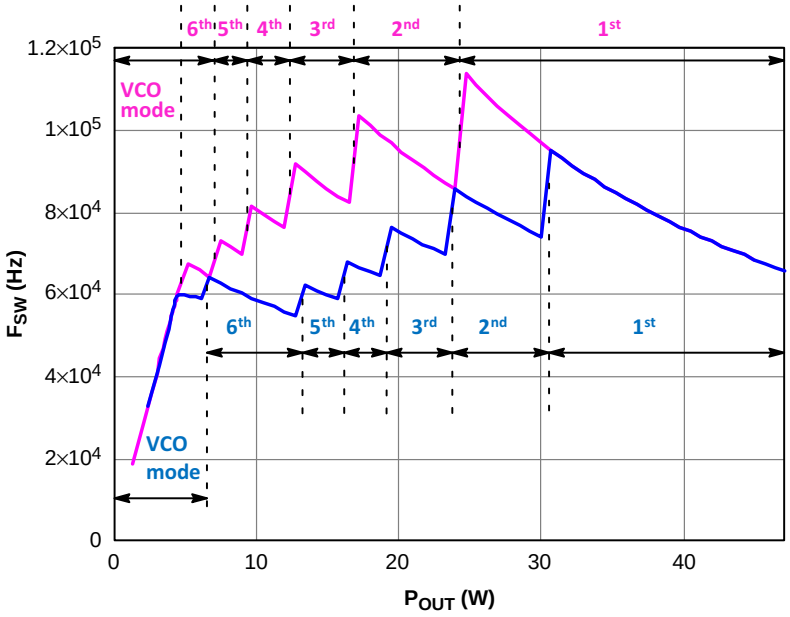

Figure 3. Switching Frequency vs. Output Power at V_{in} = 115 V_{rms}

FREQUENCY FOLDBACK MODE

Operating Details

At nominal power, the power supply operates in a variable frequency system where discrete frequency steps occur as the controller looks for the different valley positions.

At low output power, the controller enters a Frequency Foldback (FF) mode. This mode is entered when V_{FB} drops below 0.8 V. The controller remains in this mode until V_{FB} increases above 1 V. During the FF operation (V_{FB} < 0.8 V), the peak current is frozen to 25% of its maximum value and the frequency diminishes as the output power decreases. To reduce the switching frequency, the system adds some dead-time controlled by a ramp. The ramp is grounded from MOSFET turn on until the 6th valley is detected. Hence, there is no discontinuity and the frequency smoothly reduces as FB goes below 0.8 V. The ramp slope is proportional to the FB voltage. Practically, the circuit embeds a current source that depends on the FB pin voltage: $I_{source} = FB / R$ where R is an internal resistor. A second current $I_{sink} = (0.4\ V / R)$ is subtracted to the first current so that $(I_{source} - I_{sink} = (FB - 0.4\ V) / R)$ charges the ramp. When the ramp reaches an internal threshold, the dead-time is finished and a clock is generated so that a new DRV pulse can be generated.

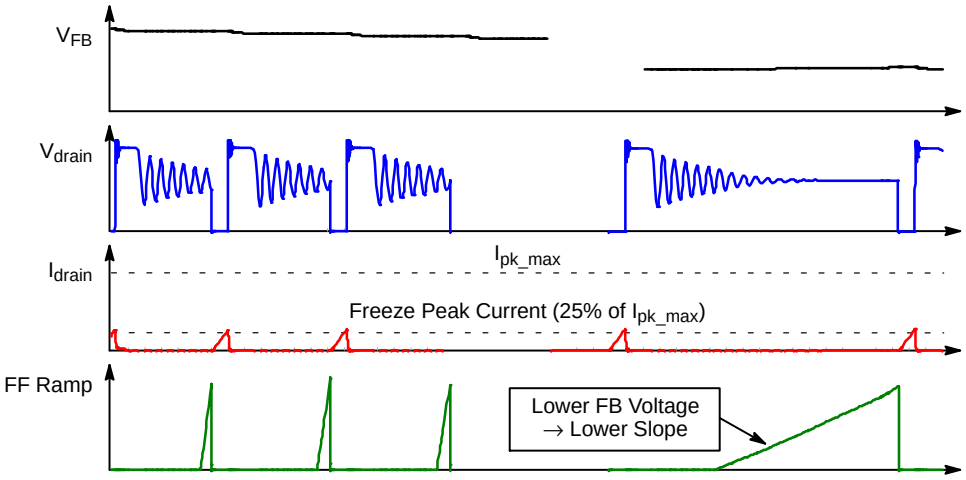

Figure 4. V_{FB}, I_{drain}, V_{drain}, FF Ramp, at Different Output Loads in VCO Mode

ZERO CROSSING DETECTION

The NCP1339 integrates the inductor reset (or Zero Current) detection (ZCD). ZCD is achieved by observing the auxiliary winding voltage (V_{AUX}).

The V_{AUX} positive part (when the MOSFET is off) is used for zero crossing detection. The schematic of the zero-crossing detection block is shown in Figure 5.

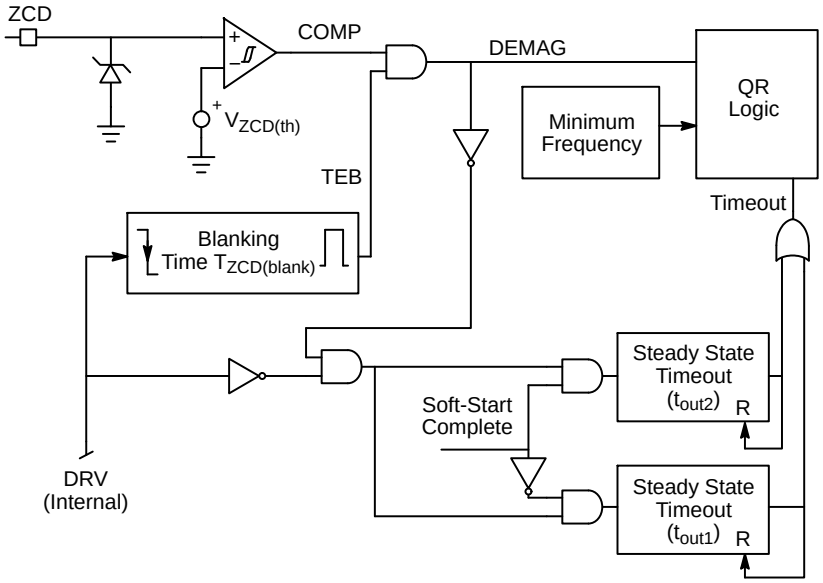

Figure 5. Zero-crossing Detection Bloc Schematic

In case of extremely damped free oscillations, the ZCD comparator can be unable to detect valleys. To avoid such a situation, NCP1339 integrates a Time Out function that acts as a substitute clock for the decimal counter inside the logic block. The controller thus continues its normal operation. To avoid having a too big step in frequency, the time out duration is set to 6 μs.

The NCP1339 also features an extended time out during the soft-start. Indeed, at startup, the output voltage reflected on the auxiliary winding is low, the ZCD comparator might be unable to detect the valleys. If the 6-μs steady-state timeout was used in this condition, a DRV pulse would be generated every 6 μs. This delay is generally too short that leads to a continuous conduction mode operation (CCM) when the power supply enters operation. To cope with this situation (that only lasts for a few cycles until the voltage on ZCD pin becomes high enough to be detected by the ZCD comparator), the time-out duration is extended to 100 μs during the soft-start period in order to ensure that the transformer is fully demagnetized before the MOSFET is turned-on.

OVER POWER PROTECTION

Operating Details

The power capability of a flyback operated in Quasi Resonance is not constant over the line range. Instead, as suggested by Eq. 2, it dramatically increases when the input voltage rises. Two main reasons cause this:

- The peak current is higher at high line due to the T_{prop} propagation delay between the moment when the MOSFET current reaches the target and the moment when the MOSFET actually opens.
- The frequency is also higher at high line leading to a higher power capability

To cope with safety requirements, the designer needs to limit the power output capability over the input voltage range. The NCP1339 features a function named Over Power Protection (OPP) to contain the power variations. It generally gives the capability of maintaining the power deviation within ±20% in a universal mains application. Higher accuracy can be obtained in narrow mains applications.

The technique implemented in the NCP1339 takes benefit of the auxiliary winding voltage whose negative amplitude is proportional to the input rail voltage. When the power MOSFET is on, the auxiliary winding voltage becomes the input voltage V_{in} affected by the auxiliary to primary turn ratio $(N_{p,aux} = N_{aux} / N_p)$:

$$V_{aux} = - N_{p,aux} \cdot V_{in} \quad \text{(eq. 3)}$$

By applying this voltage through a resistor divider on the OPP pin, we have an image of the input voltage transferred to the controller via this pin. This voltage is added internally to the 0.8-V reference and affects the maximum peak current (Figure 6). As the OPP voltage is negative, an increase of input voltage implies a decrease of the maximum peak current setpoint:

$$V_{CS,max} = 0.8 + V_{OPP} \quad \text{(eq. 4)}$$

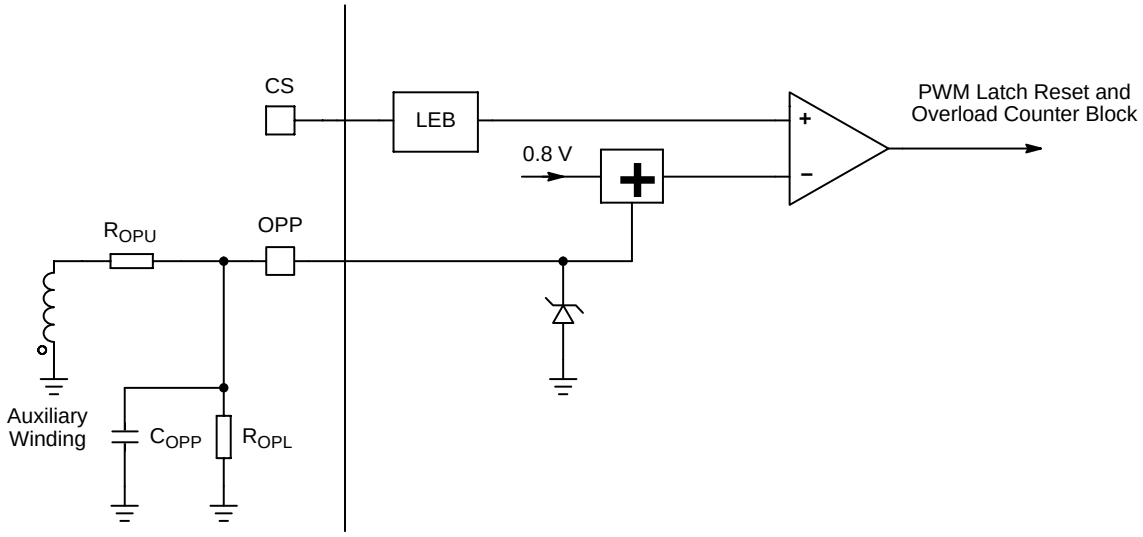

Figure 6. OPP Circuit

The maximum OPP voltage that can be applied to OPP pin is –250 mV, which corresponds to peak current decrease of 31.25%.

The auxiliary winding voltage can be the seat of ringing. Therefore, it may be needed to add a capacitor (C_{OPP} of Figure 6) to filter the voltage.

It is wise noting that this capacitor delays the OPP voltage settling to its final value. It is then necessary to check that this delay is shorter than the on-time at full load.

Calculating the Needed OPP Amount for the Design

Because of the propagation delay, the maximum peak current at high line is:

$$I_{pk(high)} = \frac{0.8}{R_{sense}} + V_{in(max),dc} \cdot \frac{t_{prop}}{L_p} \qquad \text{(eq. 5)}$$

The corresponding switching period and output power can be deduced from Eq. 1 and Eq. 2:

$$T_{sw(high)} = I_{pk(high)} \cdot L_p \cdot \left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out} + V_f} \right) + \qquad \text{(eq. 6)}$$

$$+ \pi \cdot \sqrt{L_p \cdot C_{lump}}$$

$$P_{out(high)} = \frac{1}{2} \cdot L_p \cdot I_{pk(high)}{}^2 \cdot \frac{1}{T_{sw(high)}} \cdot \eta \qquad \text{(eq. 7)}$$

We would like to limit the output power to $P_{out(limit)} > P_{out(nom)}$ at maximum input voltage. In order to perform over power compensation, we need to calculate the peak current $I_{pk(limit)}$ corresponding to $P_{out(limit)}$.

$$I_{pk(limit)} = \frac{L_p \cdot \left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out}+V_f} \right) + \sqrt{L_p{}^2 \cdot \left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out}+V_f} \right)^2 + 2 \cdot \frac{L_p \cdot \eta}{P_{out(limit)}} \cdot \pi \cdot \sqrt{L_p \cdot C_{lump}}}}{\frac{L_p \cdot \eta}{P_{out(limit)}}} \qquad \text{(eq. 8)}$$

The amount of OPP voltage needed is thus:

$$V_{OPP} = -0.8 \cdot \left(1 - \frac{I_{pk(limit)}}{I_{pk(max)}} \right) \qquad \text{(eq. 9)}$$

As an example, in order to provide a 25% power margin to our 45-W adapter, we want to limit the output power to 57 W at high line.

Using equations Eq. 5 to Eq. 7, we obtain:

$$I_{pk(high)} = \frac{0.8}{R_{sense}} + V_{in(max),dc} \cdot \frac{t_{prop}}{L_p} = \frac{0.8}{0.31} + 375 \cdot \frac{600 \cdot 10^{-9}}{345 \cdot 10^{-6}} = 3.23 \text{ A} \qquad \text{(eq. 10)}$$

$$T_{sw(high)} = I_{pk(high)} \cdot L_p \cdot \left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out} + V_f} \right) + \pi \cdot \sqrt{L_p \cdot C_{lamp}} = \qquad \text{(eq. 11)}$$

$$= 3.23 \cdot 345 \cdot 10^{-6} \cdot \left(\frac{1}{375} + \frac{0.25}{19 + 0.8} \right) + \pi \cdot \sqrt{345 \cdot 10^{-6} \cdot 250 \cdot 10^{-12}} = 18.0 \,\mu\text{s}$$

$$P_{out(high)} = \frac{1}{2} \cdot L_p \cdot I_{pk(high)}{}^2 \cdot \frac{1}{T_{sw(high)}} \cdot \eta = \frac{1}{2} \cdot 345 \cdot 10^{-6} \cdot 3.23^2 \cdot \frac{1}{18.0 \cdot 10^{-6}} \cdot 0.85 = 85 \text{ W} \qquad \text{(eq. 12)}$$

If no over power compensation is applied, the adapter will be able to deliver 85 W at high line! In order to limit the output power to 57 W at 265 Vrms, the peak current must be reduced to:

$$I_{pk(limit)} = \frac{L_p \cdot \left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out}+V_f} \right) + \sqrt{L_p{}^2 \cdot \left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out}+V_f} \right)^2 + 2 \cdot \frac{L_p \cdot \eta}{P_{out(limit)}} \cdot \pi \cdot \sqrt{L_p \cdot C_{lump}}}}{\frac{L_p \cdot \eta}{P_{out(limit)}}} = \qquad \text{(eq. 13)}$$

$$= \frac{345 \times 10^{-6} \cdot \left(\frac{1}{375} + \frac{0.25}{19+0.8} \right) + \sqrt{(345 \times 10^{-6})^2 \cdot \left(\frac{1}{375} + \frac{0.25}{19+0.8} \right)^2 + 2 \cdot \frac{345 \times 10^{-6} \cdot 0.85}{57} \cdot \pi \cdot \sqrt{345 \cdot 10^{-6} \cdot 250 \cdot 10^{-12}}}}{\frac{345 \cdot 10^{-6} \cdot 0.85}{57}} =$$

$$= 2.21 \text{ A}$$

The amount of OPP voltage that must be applied to the design is:

$$V_{OPP} = -0.8 \cdot \left(1 - \frac{I_{pk(limit)}}{I_{pk(max)}} \right) = -0.8 \cdot \left(1 - \frac{2.21}{3.23} \right) = -253 \text{ mV} \qquad \text{(eq. 14)}$$

Calculating the OPP Resistors

Looking at Figure 6, if we apply the resistor divider law on the pin 2 during the on-time, we obtain the following relationship:

$$\frac{R_{opu}}{R_{opl}} = \frac{-N_{p,aux} \cdot V_{in,dc} - V_{OPP}}{V_{OPP}} \qquad \text{(eq. 15)}$$

By choosing a value for R_{opl} (for example 1.5 kΩ), we can easily deduce R_{opu} value.

Following our example from before, we need 253 mV of OPP voltage to limit the output power to 57 W at 265 Vrms.

We choose:

$$R_{opl} = 1.5\ k\Omega$$

$$R_{opu} = \frac{N_{p,aux} \cdot V_{in,dc} - (V_{OPP})}{V_{OPP}} \cdot R_{opl} = \qquad \text{(eq. 16)}$$

$$= \frac{0.18 \cdot 375 - (-0.253)}{(-0.253)} \cdot 1500 = 399\ k\Omega$$

Finally, we choose a 300-kΩ resistor for R_{opu}.

A Non-dissipative OPP

The input voltage information is given by the auxiliary winding which offers lower voltage values compared to the bulk rail.

In addition, in frequency foldback mode, the switching frequency reduces. Thus, the average current in the OPP bridge decreases. Let us calculate the average current circulating in the OPP bridge at light load:

$$I_{bridge,mean} = \frac{1}{T_{sw}} \int_0^{T_{sw}} \left| \frac{V_{aux}(t)}{R_{opu} + R_{opl}} \right| dt \qquad \text{(eq. 17)}$$

We obtain:

$$I_{bridge,avg} = \frac{1}{R_{opu} + R_{opl}} \cdot \frac{t_{on}}{T_{sw}} \cdot N_{p,aux} \cdot V_{in} \cdot \sqrt{2} + \qquad \text{(eq. 18)}$$

$$+ \frac{1}{R_{opu} + R_{opl}} \cdot \frac{t_{demag}}{T_{sw}} \cdot (V_{CC} + V_f)$$

On our 45-W adapter, for an output power of 8 W, we measured:

- t_{on} = 1.1 μs
- t_{off} = 29.2 μs
- t_{demag} = 5.6 μs
- T_{sw} = 30.3 μs
- $V_{CC} + V_f$ = 13.45 V

We can calculate the OPP bridge current at highest input voltage (265 V rms):

$$I_{bridge,mean} = \frac{1}{R_{opu} + R_{opl}} \cdot \frac{t_{on}}{T_{sw}} \cdot N_{p,aux} \cdot V_{in} \cdot \sqrt{2} + \frac{1}{R_{opu} + R_{opl}} \cdot \frac{t_{demag}}{T_{sw}} \cdot (V_{CC} + V_f) = \qquad \text{(eq. 19)}$$

$$= \frac{1}{300k + 1k} \cdot \frac{1.1\mu}{30.3\mu} \cdot 0.18 \cdot 265 \cdot \sqrt{2} + \frac{1}{300k + 1k} \cdot \frac{5.6\mu}{30.3\mu} \cdot 13.45 = 16.4\ \mu A$$

As the average current it sees, is very low, the power dissipated by the OPP bridge can be neglected.

FAULT PIN

The Fault pin combines two different safety features to help design a compact power supply. The first one is an Over Voltage Protection (OVP) and the second one is an Over Temperature Protection (OTP).

Over Temperature Protection

The adapter operating in a confined area, e.g. the plastic case protecting the converter, it is important to monitor the internal ambient temperature. If this temperature increases beyond a certain point, catastrophic failures can occur through semiconductors thermal runaway or transformer saturation. To prevent this, the NCP1339 embeds an Over Temperature Protection (OTP) circuitry which can be combined with an Over Voltage Protection as sketched by Figure 7.

The $I_{Fault(OTP)}$ current (45.5 μA typ.) biases the Negative Temperature Coefficient sensor (NTC), naturally imposing a dc voltage on the OTP pin. When the temperature increases, the NTC's resistance reduces bringing the pin 5 voltage down until it reaches a typical value of 0.4 V: the comparator trips and latches-off the controller. During the latch-off phase, the V_{CC} drops to the 5.5-V $V_{CC(bias)}$ voltage level. The power supply needs to be un-plugged to reset the part.

During start-up and soft-start, the output of the OTP comparator is blanked to give the OTP pin voltage time to reach its steady-state value if a filtering capacitor is installed across the NTC. The filtering capacitor value should be 1 nF.

In the NCP1339, the OTP trip point corresponds to a resistance of:

$$R_{NTC} = \frac{V_{OTP}}{I_{OTP(REF)}} = \frac{0.4}{45.5\mu} = 8.79\ k\Omega \qquad \text{(eq. 20)}$$

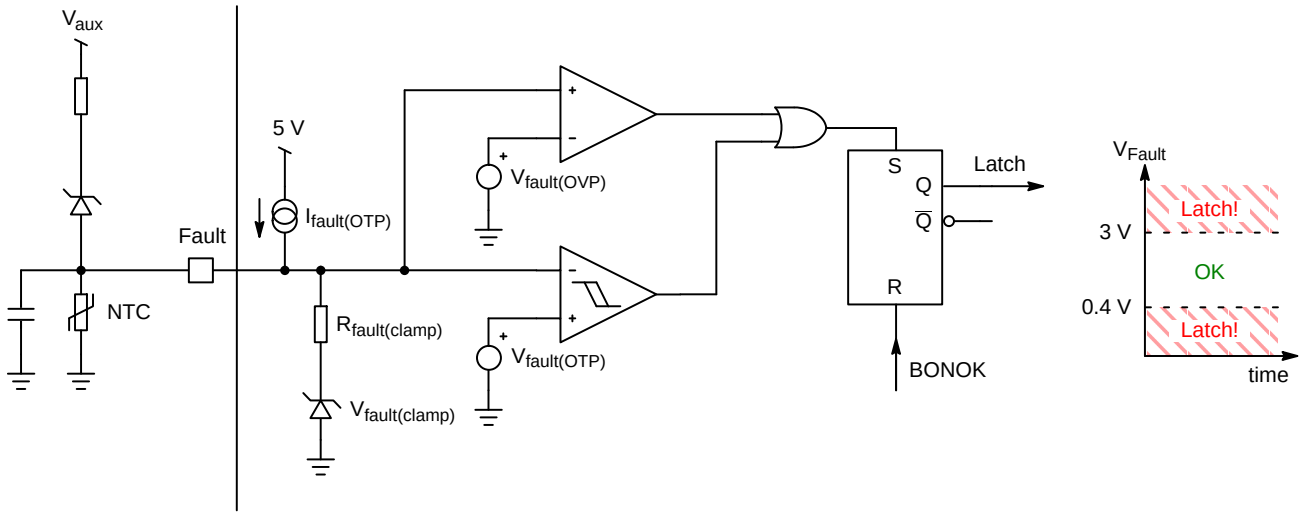

Figure 7. OTP/OPP Combination in NCP1339

Over Voltage Protection

The NCP1339 features a protection against an over voltage condition, e.g in case of the optocoupler destruction.

This over voltage protection is combined with an OTP as shown previously on Figure 7**.**

Only a Zener diode needs to be added between the V_{CC} rail and the Fault pin in order to detect an over voltage condition.

In case of over voltage, the Zener diode starts to conduct and injects current inside the internal clamp resistor $R_{Fault(clamp)}$ thus causing the pin 5 voltage to increase. When this voltage reaches the OVP threshold (3 V typ.), the controller is latched-off.

The amount of current that must be injected inside the controller by the zener diode can be calculated as follows:

$$I_{Fault} = \frac{V_{OVP} - V_{Fault(Clamp)}}{R_{Fault(Clamp)}} = \frac{3 - 1.7}{1.55 \cdot 10^{3}} = 838.7\ \mu A \quad \text{(eq. 21)}$$

CONCLUSION

This application note has described the equations needed to design a QR adapter driven by the NCP1339.

All the equations presented have been implemented inside a Mathcad spreadsheet that can be downloaded from our website: http://www.onsemi.com/

REFERENCES

[1] Yann Vaquette, “A 45-W adaptor with NCP1339 Quasi-Resonant controller”, Evaluation Board User’s Manual EVBUM2248/D.

[2] Stéphanie Conseil, “QR − Analysis and Design of Quasi-Resonant Converters”, Tutorial TND348.

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