AND9364/D

How to Select the Frequency Foldback Product Option When Designing a Compact, High-Efficiency PFC Stage Using the NCP1602

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APPLICATION NOTE

This paper describes how to select one of the frequency foldback product options out of the A, B, C, D, E, F, G, H, I list in order to design a Discontinuous Conduction Mode PFC stage driven by the NCP1602.

Introduction

Housed in a TSOP−6 package, the NCP1602 is designed to optimize the efficiency of your PFC stage throughout the load range. Incorporating protection features for rugged operation, it is ideal in systems where cost−effectiveness, reliability, low stand−by power and high efficiency are key requirements:

- **Valley Synchronized Frequency Fold−back (VSFF)**:
  The circuit operates in Critical conduction Mode (CrM) when the VCTRL pin voltage is above a preset level. When the VCTRL pin voltage goes lower than the preset level, the controller enters a Discontinuous conduction Mode and starts adding dead−time after the inductor demagnetization phase. The lower the VCTRL pin voltage, the higher the value of the dead time added. As a result, the frequency linearly decays to about 33 kHz.
- **Skip Mode**:
  SKIP Mode is optional, versions NCP1602−[B**] and NCP1602−[D**] have the SKIP mode feature, but versions NCP1602−[A**] and NCP1602−[C**] have the SKIP mode feature disabled. To optimize the Power Efficiency at low output power, a controller version using a SKIP Mode is available. When VCTRL pin voltage gets lower than the SKIP Mode threshold voltage, the power mosfet drive is disabled. As a result the output voltage of the controller goes down , making in turn the VCTRL voltage go up and eventually above the SKIP mode threshold. VCTRL pin voltage being now above the SKIP mode threshold, the drive of the power mosfet is enabled.
- **Low Start−up Current and Large V_{CC} Range**:
  The extra low start−up consumption of the NCP1602−[**A]&[**B] versions allows the use of high−impedance resistors for charging the V_{CC} capacitor. The NCP1602−[**C]&[**D] versions are targeted in applications where the circuit is fed by an auxiliary power source. Its start−up level is lower than 11.25 V to allow the circuit to be powering from a 12−V rail. Both versions feature a large V_{CC} operating range (9.5 V to 30 V).
- **Fast Line / Load Transient Compensation (Dynamic Response Enhancer and Soft OVP)**:
  Due to the slow loop response of traditional PFC stages, abrupt changes in the load or in the input voltage may cause significant over or under−shoots. This circuit drastically limits these possible deviations from the regulation point.
- **Safety Protections**:
  NCP1602 features make the PFC stage extremely robust. Among them, we can mention the Brown−Out Detection block (see NOTE below) that stops operation when the ac line is too low and the 2−level Current Sensing, that forces a low duty−ratio operation mode in the event that the current exceeds 150% of the current limit which may be caused by the inductor saturation or by a short of the bypass or boost diode.

NOTE: The voltage of the Brown−out detection block input pin (CS/ZCD) is also used to detect the line range and reduce the loop gain in high−line conditions (2−step feed−forward)

- **Eased Manufacturing and Safety Testing**:
  Elements of the PFC stage can be accidently shorted, badly soldered or damaged as a result of manufacturing or handling incidents, excessive operating stress or other troubles. In particular, adjacent pins of controllers can be shorted, a pin, grounded or badly connected. It is often required that such open/short situations do not cause fire, smoke nor loud noise. The NCP1602 integrates enhanced functions that help address requirement, for instance, in case of an improper pin connection (including GND) or of a short of the boost or bypass diode.

PFC Stage Dimensioning

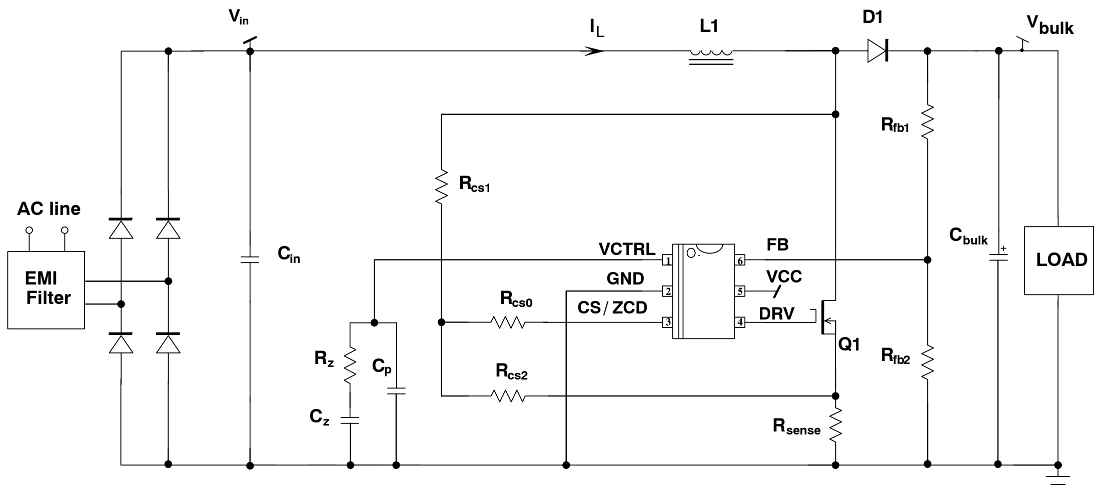


Figure 1. EVB Schematic with Power and Control Circuitry

Step 1: Define the Input Parameters Values

- $(V_{line,rms})_{LSL}$: Lower operating line voltage. This is the minimum rms input voltage for which the PFC stage operates in nominal conditions.
- $(V_{line,rms})_{USL}$: Higher operating line voltage. This is the maximum input rms voltage for which the PFC stage operates in nominal conditions.
- P_{eff} : Power efficiency defined by

$$P_{eff} = \frac{P_{out,avg}}{P_{in,avg}}$$

- $(P_{out,avg})_{LSL}$: Lower operating input power
- $(P_{out,avg})_{USL}$: Higher operating input power
- $(P_{out,avg})_{FF}$: Input power at which the CrM to DCM transition occurs
- L : Power inductor

Step 2: Calculate the Maximum Inductor Value

Average input power is related to line voltage power inductor value and $t_{ON,max}$ by the following and well known equation:

$$P_{in,avg} = \frac{\left(V_{in,rms}\right)^2}{2 \cdot L} \cdot t_{ON,max} \qquad \text{(eq. 1)}$$

A more well known equation is the definition of power efficiency (eq.2)

$$P_{eff} = \frac{P_{out,avg}}{P_{in,avg}} \qquad \text{(eq. 2)}$$

Now, if we want to chose an inductor value to be able to provide at least 50 percent more output power than the higher operating input power, it will be a maximum inductor value given by the following equation.

$$L_{max} = \frac{\left(V_{in,rms}\right)^2_{LSL}}{2 \cdot \frac{\left(P_{out,avg}\right)_{USL}}{\left(P_{eff}\right)_{USL}} 1.5} \cdot t_{ON,max} \qquad \text{(eq. 3)}$$

$t_{ON,max}$ in the above equation will depend on High Line or Low Line condition.

Low Line/High Line condition is normally sensed by the controller when the resistor divider ratio of the pin CSZCD is equal to 138 so for example a 110 V line application will be sensed as Low Line (LL) and a 230 V line application will be sensed High Line (HL).

Low Line condition can also be forced by using a resistor divider ratio of the pin CSZCD equal to 2 x 138, at the expense of loosing OVP2 functionality and not being able to use a Brown−out option. Forcing Low Line means the controller will internally set Low Line condition even if the mains voltage is equal to 230 V.

Because Frequency Foldback options are set based on $t_{ON,max}$ value and Low Line / High Line condition, the L_{max} value will be calculated using the $t_{ON,max}$ values of Table 1.

Table 1. NCP1602 FREQUENCY FOLDBACK OPTIONS

NCP1602 Option	$V_{REF,DT}$ (V)	$t_{ON,max,LL}$ (s)	$t_{ON,max,HL}$ (s)	$t_{ON,FF,LL}$ (μs)	$t_{ON,FF,HL}$ (μs)
A	0.27	25.00	8.33	1.97	0.658
B	0.45	25.00	8.33	3.29	1.100
C	0.68	25.00	8.33	4.97	1.660
D	0.54	12.50	4.17	1.97	0.658
E	0.90	12.50	4.17	3.29	1.100
F	1.35	12.50	4.17	4.93	1.640
G	0.82	8.33	2.78	2.00	0.666
H	1.35	8.33	2.78	3.29	1.100
I	2.00	8.33	2.78	4.87	1.620

For example for 207 V mains minimum operating voltage, 36 W $(P_{out,avg})_{USL}$ = 36 W, $(P_{eff})_{USL}$ = 0.9 and Option G the L_{max} value will be given for High Line and Low Line by:

$$L_{max,G,HL} = \frac{207^2}{2 \cdot \frac{36}{0.9} 1.5} \cdot 2.78e-6 = 0.993\ \text{mH} \qquad \text{(eq. 4)}$$

$$L_{max,G,LL} = \frac{207^2}{2 \cdot \frac{36}{0.9} 1.5} \cdot 8.33e-6 = 2.98\ \text{mH} \qquad \text{(eq. 5)}$$

Step 3: Select the Product Options Compatible with a Maximum Switching Frequency at Line Zero Crossing

If we start at maximum power and we reduce this power, the maximum switching frequency, which is obtained close to line zero crossing, increases because we are in CrM mode. The maximum of this maximum switching frequency is obtained just before the PFC controller enters into DCM mode. After entering the DCM mode the switching frequency starts to reduce (Frequency Foldback) because a VCTRL based dead time is added after the end of inductor demagnetization. The controller operates at constant t_{ON}, and the CrM−DCM border is reached for a t_{ON} value equal to $t_{ON,FF}$ which depends on product option depicted in Table 1. Theoretically and using a very simple model not taking into account the ringing frequency of the drain voltage after the end of demagnetization, at line zero crossing the t_{OFF} is almost zero and the maximum switching frequency is given by:

$$F_{sw,max} = \frac{1}{t_{ON}} \qquad \text{(eq. 6)}$$

However t_{OFF} is not equal to zero at line zero crossing but given by:

$$t_{OFF,ZC} = \pi \sqrt{L \cdot C_{drain}} \qquad \text{(eq. 7)}$$

Where L is the boost PFC inductor and C_{drain} the total capacitance between powermosfet drain node and ground.

So the maximum of the maximum switching frequency at line zero crossing is given by:

$$F_{sw,max,FF,i} = \frac{1}{t_{ON,FF,i} + \pi \sqrt{L \cdot C_{drain}}} \qquad \text{(eq. 8)}$$

The maximum of $F_{sw,max}$ named $F_{sw,max,FF,i}$ is given by the t_{ON} value at CrM−DCM border $t_{ON,FF,LL,i}$ or $t_{ON,FF,HL,i}$ and depends on NCP1602 option i shown in Table 1.

For example, using option E, Max(Fsw,max) is given by:

$$F_{sw,max,FF,E} = \frac{1}{t_{ON,FF,LL,E} + \pi \sqrt{L \cdot C_{drain}}} \qquad \text{(eq. 9)}$$

with $t_{ON,FF,LL,E}$ = 3.29 μs @ Low Line

$$F_{sw,max,FF,E} = \frac{1}{t_{ON,FF,HL,E} + \pi \sqrt{L \cdot C_{drain}}} \qquad \text{(eq. 10)}$$

with $t_{ON,FF,HL,E}$ = 1.10 μs @ High Line

Assuming Low Line can be forced, there are 2x9=18 $t_{ON,FF}$ values corresponding to the product options of Table 1 so 18 cases will have to be check with respect to line zero crossing frequency criteria. Only a certain number of product option will be acceptable.

Step 4: Select the Product Options Compatible with the Input Power at which the Switching Transitions from CrM to DCM

The input power at which the transition from CrM to DCM mode occurs (see Figure 2) is given by:

$$P_{in,avg,FF,i} = \frac{\left(V_{line,rms}\right)^2}{2L} t_{ON,FF,i} \qquad \text{(eq. 11)}$$

It can be clearly seen that for a given line voltage and inductor value, the product option i, through the parameter $t_{ON,FF}$, controls the $P_{in,avg,FF}$ value.

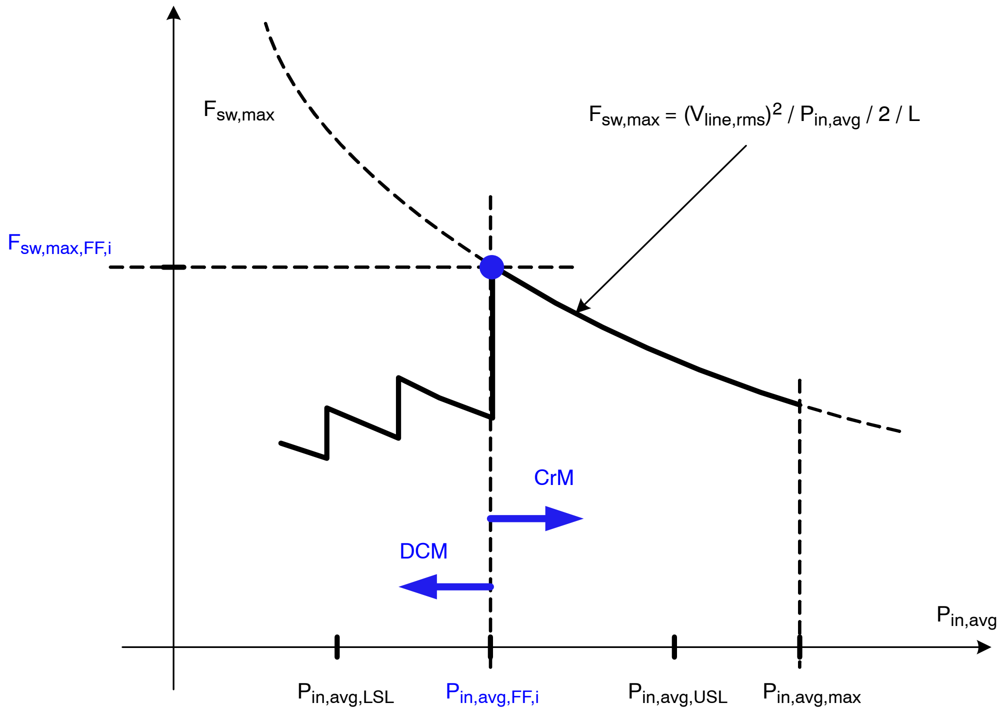


Figure 2. Line Zero Crossing Frequency versus Input Power

NOTE: The saw tooth shape of $F_{sw,max}$ versus $P_{in,avg}$ in DCM is due to the number of valleys

Step 5: Check if Minimum Frequency at Maximum Line Voltage Fulfils Requirements

We have been checking so far for the maximum of line zero crossing frequency, but there is also the minimum switching frequency $F_{sw,min}$ which appears at maximum line voltage (see Figure 3) and as it carries more power is worth to check.

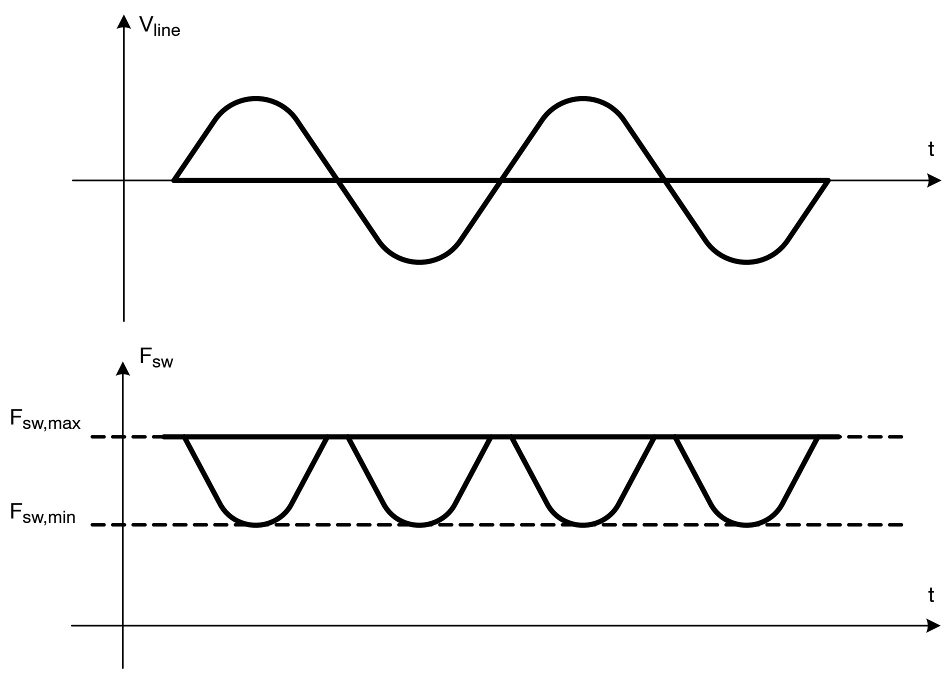


Figure 3. Switching Frequency versus Line Voltage versus Time

In CrM the minimum swiching frequency Fsw,min is given by:

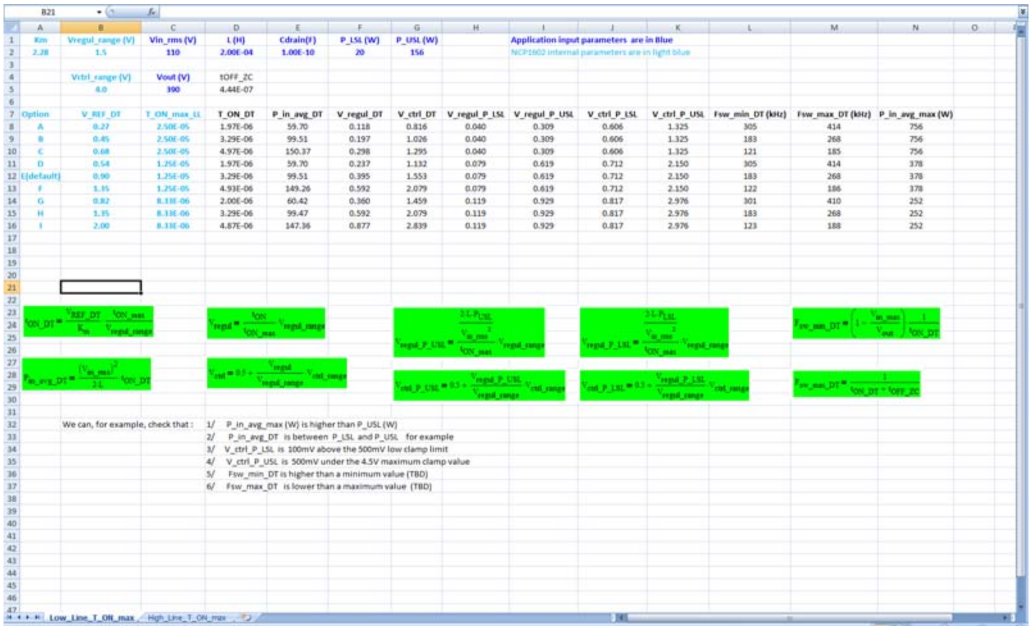
$$F_{sw,min} = \left(1 - \frac{V_{line,rms}\sqrt{2}}{V_{out}}\right) \cdot \frac{1}{t_{ON}} \qquad \text{(eq. 12)}$$

The maximum of $F_{sw,min}$ is reached at the CrM−DCM boundary and is given by:

$$F_{sw,min,FF,i} = \left(1 - \frac{V_{line,rms}\sqrt{2}}{V_{out}}\right) \cdot \frac{1}{t_{ON,FF,i}} \qquad \text{(eq. 13)}$$

Step 5: Using the Excel Spreadsheet

A special Excel Spreadsheet named AN1602_FFB_OPTIONS.xlsx has been written for helping choosing the inductor value and product option, for a given application. It contains all the formulas given in this document.



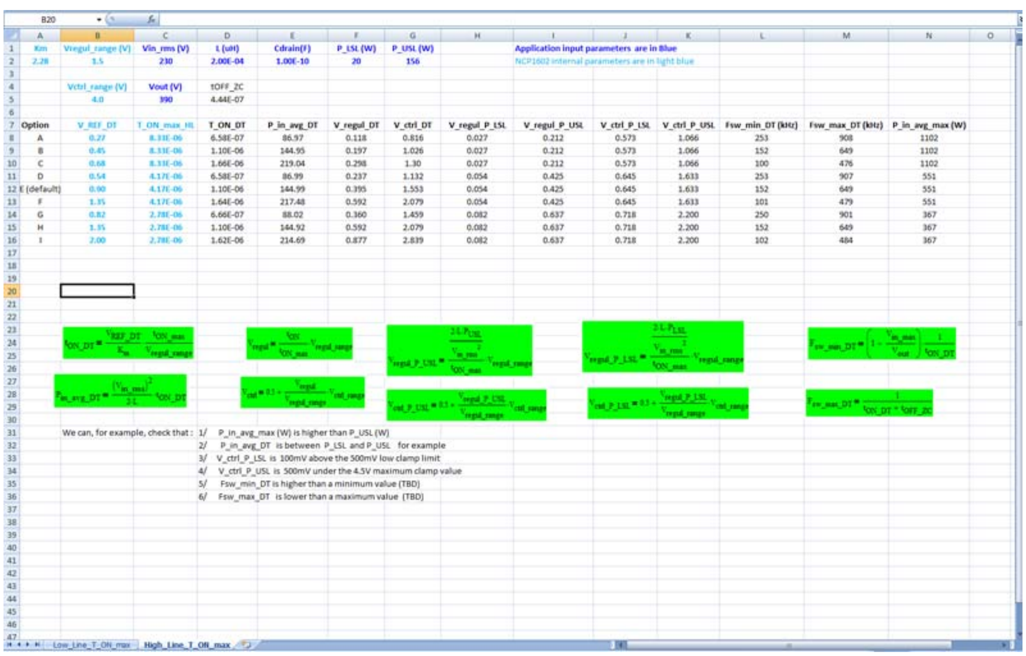
Km	Vregul_range (V)	Vin_rms (V)	L (H)	Cdrain(F)	P_LSL (W)	P_USL (W)
2.28	1.5	110	2.00E-04	1.00E-10	20	156
	Vctrl_range (V)	Vout (V)	tOFF_ZC			
	4.0	390	4.44E-07			

Application input parameters are in Blue
NCP1602 internal parameters are in light blue

Option	V_REF_DT	T_ON_max_LL	T_ON_DT	P_in_avg_DT	V_regul_DT	V_ctrl_DT	V_regul_P_LSL	V_regul_P_USL	V_ctrl_P_LSL	V_ctrl_P_USL	Fsw_min_DT (kHz)	Fsw_max_DT (kHz)	P_in_avg_max (W)
A	0.27	2.50E-05	1.97E-06	59.70	0.118	0.816	0.040	0.309	0.606	1.325	305	414	756
B	0.45	2.50E-05	3.29E-06	99.51	0.197	1.026	0.040	0.309	0.606	1.325	183	268	756
C	0.68	2.50E-05	4.97E-06	150.37	0.298	1.295	0.040	0.309	0.606	1.325	121	185	756
D	0.54	1.25E-05	1.97E-06	59.70	0.237	1.132	0.079	0.619	0.712	2.150	305	414	378
E(default)	0.90	1.25E-05	3.29E-06	99.51	0.395	1.553	0.079	0.619	0.712	2.150	183	268	378
F	1.35	1.25E-05	4.93E-06	149.26	0.592	2.079	0.079	0.619	0.712	2.150	122	186	378
G	0.82	8.33E-06	2.00E-06	60.42	0.360	1.459	0.119	0.929	0.817	2.976	301	410	252
H	1.35	8.33E-06	3.29E-06	99.47	0.592	2.079	0.119	0.929	0.817	2.976	183	268	252
I	2.00	8.33E-06	4.87E-06	147.36	0.877	2.839	0.119	0.929	0.817	2.976	123	188	252

We can, for example, check that :
1/ P_in_avg_max (W) is higher than P_USL (W)
2/ P_in_avg_DT is between P_LSL and P_USL for example
3/ V_ctrl_P_LSL is 100mV above the 500mV low clamp limit
4/ V_ctrl_P_USL is 500mV under the 4.5V maximum clamp value
5/ Fsw_min_DT is higher than a minimum value (TBD)
6/ Fsw_max_DT is lower than a maximum value (TBD)

Figure 4. Screenshot of the Excel Spreadsheet for Low Line State



Km	Vregul_range (V)	Vin_rms (V)	L (uH)	Cdrain(F)	P_LSL (W)	P_USL (W)
2.28	1.5	230	2.00E-04	1.00E-10	20	156
	Vctrl_range (V)	Vout (V)	tOFF_ZC			
	4.0	390	4.44E-07			

Application input parameters are in Blue
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Option	V_REF_DT	T_ON_max_HL	T_ON_DT	P_in_avg_DT	V_regul_DT	V_ctrl_DT	V_regul_P_LSL	V_regul_P_USL	V_ctrl_P_LSL	V_ctrl_P_USL	Fsw_min_DT (kHz)	Fsw_max_DT (kHz)	P_in_avg_max (W)
A	0.27	8.33E-06	6.58E-07	86.97	0.118	0.816	0.027	0.212	0.573	1.066	253	908	1102
B	0.45	8.33E-06	1.10E-06	144.95	0.197	1.026	0.027	0.212	0.573	1.066	152	649	1102
C	0.68	8.33E-06	1.66E-06	219.04	0.298	1.30	0.027	0.212	0.573	1.066	100	476	1102
D	0.54	4.17E-06	6.58E-07	86.99	0.237	1.132	0.054	0.425	0.645	1.633	253	907	551
E (default)	0.90	4.17E-06	1.10E-06	144.99	0.395	1.553	0.054	0.425	0.645	1.633	152	649	551
F	1.35	4.17E-06	1.64E-06	217.48	0.592	2.079	0.054	0.425	0.645	1.633	101	479	551
G	0.82	2.78E-06	6.66E-07	88.02	0.360	1.459	0.082	0.637	0.718	2.200	250	901	367
H	1.35	2.78E-06	1.10E-06	144.92	0.592	2.079	0.082	0.637	0.718	2.200	152	649	367
I	2.00	2.78E-06	1.62E-06	214.69	0.877	2.839	0.082	0.637	0.718	2.200	102	484	367

We can, for example, check that :
1/ P_in_avg_max (W) is higher than P_USL (W)
2/ P_in_avg_DT is between P_LSL and P_USL for example
3/ V_ctrl_P_LSL is 100mV above the 500mV low clamp limit
4/ V_ctrl_P_USL is 500mV under the 4.5V maximum clamp value
5/ Fsw_min_DT is higher than a minimum value (TBD)
6/ Fsw_max_DT is lower than a maximum value (TBD)

Figure 5. Screenshot of the Excel Spreadsheet for High Line State

PUBLICATION ORDERING INFORMATION

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