AND9218/D

5 Key Steps to Designing a Compact, High-Efficiency PFC Stage Using the NCP1602

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APPLICATION NOTE

Description

This paper describes the key steps to rapidly design a Discontinuous Conduction Mode PFC stage driven by the NCP1602. The process is illustrated in a practical 160-W, universal mains application:

- Maximum Output Power: 160 W
- Rms Line Voltage Range: from 86 V to 265 V
- Regulation output voltage: 400 V
- Frequency Fold-Back when the Line Current is Less than 400 mA

Introduction

Housed in a TSOP−6 package, the NCP1602 is designed to optimize the efficiency of your PFC stage throughout the load range. Incorporating protection features for rugged operation, it is ideal in systems where cost-effectiveness, reliability, low stand-by power and high efficiency are key requirements:

- *Valley Synchronized Frequency Fold-Back (VSFF):* The circuit operates in Critical conduction Mode (CrM) when the VCTRL pin voltage is above a preset level. When the VCTRL pin voltage goes lower than the preset level, the controller enters a Discontinuous conduction Mode and starts adding dead-time after the inductor demagnetization phase. The lower the VCTRL pin voltage, the higher the value of the dead time added. As a result, switching frequency linearly decays to about 33 kHz.
- *Skip Mode:* SKIP Mode is optional, versions NCP1602−[B**] and NCP1602−[D**] have the SKIP mode feature, but versions NCP1602−[A**] and NCP1602−[C**] have the SKIP mode feature disabled. To optimize the Power Efficiency at low output power, a controller version using a SKIP Mode is available. When VCTRL pin voltage gets lower than the SKIP Mode threshold voltage, the power MOSFET drive is disabled. As a result the output voltage of the controller goes down, making in turn the VCTRL voltage go up and eventually above the SKIP mode threshold. VCTRL pin voltage being now above the SKIP mode threshold, the power MOSFET drive is enabled.
- *Low Start-Up Current and Large V_{CC} Range:* The extra low start-up consumption of the NCP1602−[**A]&[**B] versions allows the use of high-value resistors for charging the V_{CC} capacitor. The NCP1602−[**C]&[**D] versions are targeted in applications where the circuit is fed by an auxiliary power source. Its start-up level is lower than 11.25 V, allowing the circuit to be powering from a 12-V rail. Both versions feature a large V_{CC} operating range (9.5 V to 30 V).
- *Fast Line/Load Transient Compensation (Dynamic Response Enhancer and Soft OVP):* Due to the slow loop response of traditional PFC stages, abrupt changes in the load or in the input voltage may cause significant over or under-shoots. This proprietary circuit drastically limits these possible deviations from the regulation point.
- *Safety Protections:* NCP1602 features make the PFC stage extremely robust. Among them, we can mention the Brown-Out Detection block[1] that stops operation when the ac line is too low and the 2-level Current Sensing, that forces a low duty-ratio operation mode in the event that the inductor current exceeds 150% of the current limit. This situation can be caused by inductor saturation or by the bypass or boost diode short circuit.
- *Eased Manufacturing and Safety Testing:* Some elements of the PFC stage can be accidently shorted, badly soldered or damaged as a result of manufacturing or handling incidents, excessive mechanical stress or other troubles. In particular, some adjacent pins can be shorted, a single pin can be grounded or badly connected. It is often required that such open/short situations do not cause fire, smoke nor loud noise. The NCP1602 integrates enhanced functions that help address these requirements, for instance, in case of an improper pin connection (including GND) or of a short of the boost or bypass diode. Application note AND9079/D details the behavior of a NCP1612-driven PFC stage under safety tests [1].

[1]The voltage of the brown-out detection block input pin (CS/ZCD) is also used to detect the line range and reduce the loop gain in high-line conditions (2-step feed-forward).

PFC STAGE DIMENSIONING

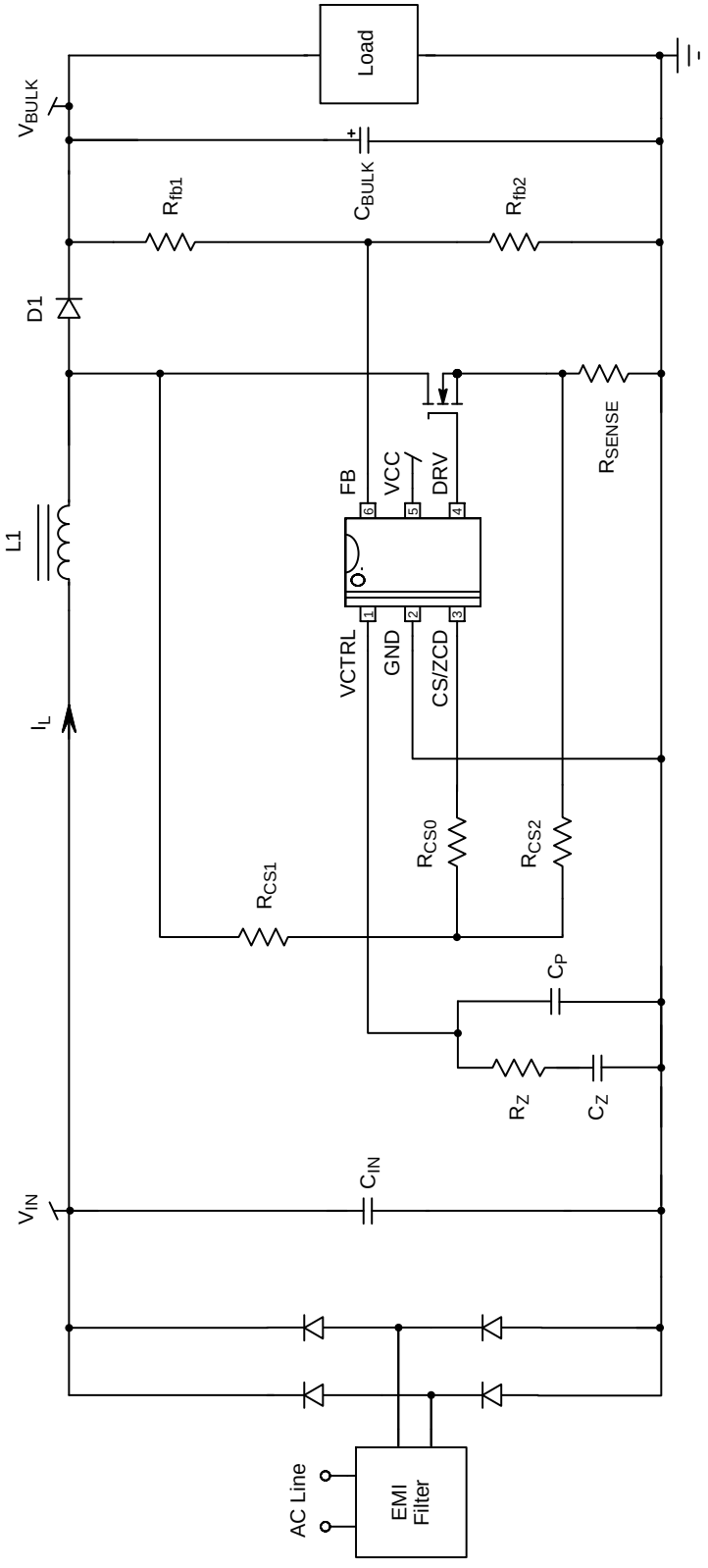

Figure 1. Evaluation Board Schematic with Power and Control Circuitry

STEP 1: DEFINE THE KEY SPECIFICATIONS

- f_{line}: Line frequency. 50 Hz/60 Hz applications are targeted. Practically, they are often specified in a range of 47−63 Hz and for calculations such as hold-up time, one has to factor in the lowest specified value.
- $(V_{line,rms})_{min}$: Lowest level of the line voltage. This is the minimum rms input voltage for which the PFC stage must operate. Such a level is usually 10−12% below the minimum typical voltage which could be 100 V in many countries.
  We will take: $(V_{line,rms})_{min}$ = 90 V
- $(V_{line,rms})_{max}$: Highest level for the line voltage. This is the maximum input rms voltage. It is usually 10% above the maximum typical voltage (240 V in many countries).
  We select: $(V_{line,rms})_{max}$ = 264 V.
- High Line $(V_{line,rms})_{HL}$ and Low Line $(V_{line,rms})_{LL}$ thresholds for internal line feedforward. Operating line voltage must be well above $(V_{line,rms})_{HL}$ or well below $(V_{line,rms})_{LL}$. These thresholds values cannot be changed because V_{HL} et V_{LL} internal reference voltage are fixed, and they must not be changed by changing K_{CS} value $K_{CS} = ((R_{CS1} + R_{CS2}) / (K_{CS1}))$ because K_{CS} value also controls OVP2 level and line Brown-out levels.

  ♦ $$\left(V_{line,rms}\right)_{LL} = \frac{K_{CS}V_{LL}}{\sqrt{2}} = \frac{138 \cdot 1.392}{\sqrt{2}} = 135.9\ V_{rms}$$ (eq. 1)

  ♦ $$\left(V_{line,rms}\right)_{HL} = \frac{K_{CS}V_{HL}}{\sqrt{2}} = \frac{138 \cdot 1.801}{\sqrt{2}} = 175.8\ V_{rms}$$ (eq. 2)

- $(V_{line,rms})_{boH}$: Brown-out line upper threshold (In case the controller is using an option featuring the brown-out protection. For controller option not featuring the brown-out protection, the following lines don't apply). The circuit prevents operation until the line rms voltage exceeds $(V_{line,rms})_{boH}$. The NCP1602 offers a 10% hysteresis. Hence, if no specific action is taken, it will detect a brown-out situation and stop operation when the rms line voltage goes below $(V_{line,rms})_{boL}$ that equates $((90\% \cdot V_{line,rms})_{boH})$. A brown-out event is sensed through the CS/ZCD pin and the parameter K_{CS}, $K_{CS} = ((R_{CS1} + R_{CS2}) / (K_{CS1})) = 138$. Internal brown-out fixed value reference voltages $V_{boH} = 819\ mV$ and $V_{boH} = 737\ mV$ are used for calculating the line brown-out thresholds:

  ♦ $$\left(V_{line,rms}\right)_{boH} = \frac{K_{CS}V_{boH}}{\sqrt{2}} = 80\ V$$ (eq. 3)

  ♦ $$\left(V_{line,rms}\right)_{boL} = \frac{K_{CS}V_{boL}}{\sqrt{2}} = 72\ V$$ (eq. 4)

  NOTE: Line brown-out thresholds cannot be modified using K_{CS} because K_{CS} also controls OVP2 threshold and internal line feedforward thresholds.

- $V_{out,nom}$: Nominal output voltage. This is the regulation level for the PFC output voltage (also designated as the bulk voltage). $V_{out,nom}$ must be higher than $(\sqrt{2} \cdot (V_{line,rms})_{HL}) = 373\ V$. 400 V is our target value (tu utilises 399 V dans les calculs)
- $(\delta V_{out})_{pk-pk}$: Peak-to-peak output voltage ripple. This parameter is often specified in percentage of output voltage. It must be selected equal or lower than 8% to avoid triggering the Dynamic Response Enhancer (DRE) in normal operation.
- P_{out}: Output power. This is the power consumed by the PFC load.
- $P_{out,max}$: Maximum output power. This is the maximum output power level which is 160 W in our application.
- $(P_{in,avg})_{max}$: Maximum input power. This is the maximum power that can be absorbed from the mains in normal operation. This level is obtained at full load, low line. Assuming an efficiency of 95% in these conditions, we will use:
  $(P_{in,avg})_{max} = 160/95\% \approx 170\ W$
- $I_{line,max}$: Maximum line current obtained at full load, low line.
- $V_{ctrl,th,*}$: CTRL pin voltage threshold below which the circuit reduces the frequency (VSFF). If the CTRL pin voltage V_{ctrl} is lower than $V_{ctrl,th,*}$, the PFC stage will permanently operates with a reduced frequency. Conversely if V_{ctrl} is higher than $V_{ctrl,th,*}$, then the PFC stage will operate in CrM (no frequency fold-back).

STEP 2: POWER COMPONENTS SELECTION

In heavy load conditions, the NCP1602 operates in Critical conduction Mode (CrM). Hence, the inductor, the bulk capacitor and the power silicon devices are dimensioned as usually done with any other CrM PFC. This chapter does not detail this process, but simply highlights key points.

Inductor Selection

The on-time of the circuit is internally limited. The power the PFC stage can deliver depends on the inductor since L will determine the current rise for a given on-time. More specifically, the following equation gives the power capability of the PFC stage:

$$\left(P_{in,avg}\right)_{HL} = \frac{V_{line,rms}^{2}}{2L} \cdot T_{on,max}$$ (eq. 5)

The smaller the inductor, the higher the PFC stage power capability. Hence, L must be low enough so that the full power can be provided at the lowest line level:

$$L \le \frac{\left(V_{line,rms}\right)_{LL}^{2}}{2 \cdot \left(P_{in,avg}\right)_{max}} \cdot T_{on,max} \quad \text{(eq. 6)}$$

Like in traditional CrM applications, the following equations give the other parameters of importance:

- Maximum Peak Current:

$$\left(I_{L,pk}\right)_{max} = 2 \cdot \sqrt{2} \cdot \frac{\left(P_{in,avg}\right)_{max}}{\left(V_{line,rms}\right)_{LL}} \quad \text{(eq. 7)}$$

- Maximum rms Current:

$$\left(I_{L,rms}\right)_{max} = \frac{\left(I_{L,pk}\right)_{max}}{\sqrt{6}} \quad \text{(eq. 8)}$$

In our application, the inductor must then meet the following requirements:

NOTE: $T_{ON,max,LL}$ = 12.5 μs corresponds to the version NCP1602−AEA (2nd digit E) which is used on the EVB.

$$L \le \frac{90^2}{2 \cdot 170} \cdot 12.5\,\mu = 295\ \mu H$$

$$\left(I_{L,pk}\right)_{max} = 2 \cdot \sqrt{2} \cdot \frac{170}{90} \cong 5.3\ A \quad \text{(eq. 9)}$$

$$\left(I_{L,rms}\right)_{max} = \frac{5.3}{\sqrt{6}} \cong 2.2\ A$$

($T_{on,max}$ = 12.5 μs) is the value for NCP1602−AEA version and it is used in Equation 9. However, the worst case for $T_{on,max}$ when used in Equation 9 is for product versions NCP1602−*G*,NCP1602−*H* and NCP1602−*I* for which the $T_{on,max}$ @ Low Line is equal to 8.33 μs. When these low $T_{on,max}$ versions are used, the inductor value must satisfy the criteria:

$$L \le \frac{90^2}{2 \cdot 170} \cdot 8.5\,\mu = 202\ \mu H \quad \text{(eq. 10)}$$

It is, in addition, recommended to select an inductor value that is at least 25% less than that returned by Equation 9 for a healthy margin.

A 200-μH/6-A_{pk} inductor (ref: 750370081 from WÜRTH ELEKTRONIK) is selected. It consists of a 10:1 auxiliary winding for zero current detection.

One can note that the switching frequency in CrM operation depends on the inductor value:

$$f_{SW} = \frac{V_{line}(t)^2 \cdot \left(V_{out} - V_{line}(t)\right)}{4 \cdot P_{in,avg} \cdot V_{out} \cdot L} \cdot 8.5\,\mu = 202\ \mu H \quad \text{(eq. 11)}$$

For instance, at low line, full load (top of the sinusoid), the switching frequency is:

$$f_{SW} = \frac{\left(\sqrt{2} \cdot 90\right)^2 \cdot \left(390 - \sqrt{2} \cdot 90\right)}{4 \cdot 170 \cdot 390 \cdot 200 \cdot 10^{-6}} \cong 80\ kHz \quad \text{(eq. 12)}$$

Power Silicon Devices

Generally, the diode bridge and the power MOSFET are placed on the same heat-sink.

As a rule of the thumb, one can estimate that the heat-sink will have to dissipate around:

- 4% of the output power in wide mains applications (95% being generally the targeted minimum efficiency)
- 2% of the output power in single mains applications.

In our wide-mains application, about 6.4 W are then to be dissipated. We selected a low-profile heat-sink from COLUMBIA-STAVER (reference: TP207ST/120/12.5/NA/SP/03) whose thermal resistance has been measured to be in the range of 6°C/W.

Among the sources of losses that contribute to this heating, one can list:

- The diodes bridge conduction losses that can be estimated by the following equation:

$$P_{bridge} = 2 \cdot V_f \cdot \frac{2\frac{\sqrt{2}}{\pi} \cdot \frac{P_{out}}{\eta}}{V_{line,rms}} \approx \frac{1.8 \cdot V_f}{V_{line,rms}} \cdot \frac{P_{out}}{\eta} \quad \text{(eq. 13)}$$

  where V_f is the forward voltage of the bridge diodes at the rated current.

- The MOSFET conduction losses are given by:

$$(P_{on})_{max} = \frac{4}{3} \cdot R_{DS(on)} \cdot \left(\frac{P_{out,max}}{\eta \cdot \left(V_{line,rms}\right)_{LL}}\right)^2 \cdot \left(1 - \frac{8\sqrt{2} \cdot \left(V_{line,rms}\right)_{LL}}{3\pi \cdot V_{out,nom}}\right) \quad \text{(eq. 14)}$$

In our application, we have:

- P_{BRIDGE} = 3.4 W, assuming that V_f is 1 V.
- $(p_{on})_{max} = 3.4 \cdot R_{DS(on)}$. In our application, a low $R_{DS(on)}$ MOSFET (0.25 Ω @ 25°C) is selected to avoid excessive conduction losses. Assuming that $R_{DS(on)}$ doubles at high temperature, the maximum conduction losses peak to about 1.7 W.

The total conduction losses for the MOSFET and the diode bridge can be as high as 5.1 W.

Switching losses cannot be easily computed. We will not attempt to predict them. Instead, as a rule of the thumb, we will assume a loss budget equal to that of the MOSFET conduction ones. Experimental tests will check that they are not under-estimated.

The boost diode is the source of the following conduction losses:$(I_{OUT} \cdot V_f)$, where I_{OUT} is the load current and V_f the diode forward voltage. The maximum output current being

nearly 0.4 A, the diode conduction losses are in the range of 0.4 W (assuming V_f = 1 V). P_{DIODE} = 0.4 W

Output Bulk Capacitor

There generally are three main criteria / constraints when defining the bulk capacitor:

- Peak-to-Peak Low Frequency Ripple:

$$\left(\delta V_{out}\right)_{pk-pk} = \frac{P_{out,max}}{C_{bulk} \cdot \omega \cdot V_{out,nom}} \qquad \text{(eq. 15)}$$

where $(\omega = 2\pi \cdot f_{line})$ is the line angular frequency. This ripple must keep lower than ±4% of the output voltage (8% peak-to-peak) in order to avoid triggering the Dynamic Response Enhancer (DRE) system while in steady state. Taking into account the line frequency minimum value (47 Hz), this leads to:

$$C_{bulk} \geq \frac{160}{8\% \cdot 2\pi \cdot 47 \cdot 399^2} \cong 42\ \mu F \qquad \text{(eq. 16)}$$

- Hold-Up Time Specification:

$$C_{bulk} \geq \frac{2 \cdot P_{out,max} \cdot t_{HOLD-UP}}{V_{out,nom}^{\ 2} - V_{out,min}^{\ 2}} \qquad \text{(eq. 17)}$$

Hence, a 10-ms hold-up time imposes:

$$C_{bulk} \geq \frac{2 \cdot 160 \cdot 10\ m}{399^2 - 350^2} \cong 87\ \mu F \qquad \text{(eq. 18)}$$

- Rms Capacitor Current:
The rms current depends on the load characteristic. Assuming a resistive load, we can derive the following approximate expression of its magnitude[2]:

$$\left(I_{c,rms}\right)_{max} \cong \qquad \text{(eq. 19)}$$

$$\cong \sqrt{\left(\sqrt{\frac{32\sqrt{2}}{9\pi}} \cdot \frac{\left(P_{in,avg}\right)_{max}}{\sqrt{\left(V_{line,rms}\right)_{LL} \cdot V_{out,nom}}}\right)^2 - \left(\frac{P_{out,max}}{V_{out,nom}}\right)^2}$$

In our application, we have:

$$I_{c,rms} \cong \sqrt{\left(\sqrt{\frac{32\sqrt{2}}{9\pi}} \cdot \frac{170}{\sqrt{90 \cdot 399}}\right)^2 - \left(\frac{160}{399}\right)^2} \cong \qquad \text{(eq. 20)}$$

$$\cong 1.06\ A$$

[2]It remains wise to verify the bulk capacitor heating on the bench!

STEP 3: BULK VOLTAGE MONITORING AND REGULATION LOOP

As shown by Figure 1, the feedback arrangement consists of:

- A resistor divider that scales down the bulk voltage to provide pin FB with the feedback signal. The upper resistor of the divider generally consists of three or four series resistors for safety considerations (see R_8, R_9 and R_{10} of Figure 7). If not, any accidental shortage of this element would apply the high voltage output to the controller low-voltage pin and destroy it.
- A filtering capacitor that is often placed between pin FB and ground to prevent switching noise from distorting the feedback signal. A 1-nF capacitor is often implemented. Generally speaking, the pole it forms with the feedback resistors must remain at a very high-frequency compared to the line one. Practically,

$$C_{fb} \leq \frac{1}{150 \cdot \left(R_{fb1} \parallel R_{fb2}\right) \cdot f_{line}}$$

generally give good results.

- A type-2 compensation network. Consisting of two capacitors and of one resistor, this circuitry sets the crossover frequency and the loop characteristic.

In steady-state the feedback being in the range of the 2.5-V regulation reference voltage, the feedback bottom resistor (R_{fb2} of Figure 1 or R_{11} of Figure 8) sets the bias current in the feedback resistors as follows:

$$I_{FB} = \frac{V_{REF}}{R_{fb2}} = \frac{2.5}{R_{fb2}} \qquad \text{(eq. 21)}$$

Trade-off between losses and noise immunity dictate the choice of this resistor. Resistors up to 56 kΩ ($I_{FB} \approx 50\ \mu A$) generally give good results. Higher values can be considered if allowed by the board PCB layout. Please note anyway that a 250-nA sink current (500 nA max. on the −40° to 125°C temperature range) is built-in to pull the feedback pin down and disable the driver if the pin is accidently open. If I_{FB} is set below 50 μA, the regulation level may be significantly impacted by the 250-nA sink current.

When the bottom resistor is selected, select the upper resistor as follows:

$$R_{fb1} = R_{fb2} \cdot \left(\frac{V_{out,nom}}{V_{REF}} - 1\right) \qquad \text{(eq. 22)}$$

In our application, we select a 27-kΩ value for R_{fb2} ($I_{FB} \approx 92\ \mu A$). As for R_{fb1}, two 1800-kΩ resistors are placed in series with a 680-kΩ one. These normalized values precisely give: (R_{fb1} = 4.28 MΩ), leading to a nominal 399-V regulation level, which is acceptable.

Compensating the Loop

The loop gain of a PFC boost converter is proportional to the square of the line magnitude if no feed-forward is applied. Hence, this gain almost varies by an order of magnitude in universal mains conditions. The CS/ZCD pin

voltage is processed by the NCP1602 in order to get an internal voltage representative of the line voltage value. The NCP1602 uses this information to perform a 2-level feed-forward function: in high-line that is detected when $V_{line,rms}$ happens to exceed $(V_{in,rms})_{HL}$, the PWM gain is divided by 3 (actually the $t_{ON,max}$ value is divided by 3) compared to a low-line state (which is set if $V_{line,rms}$ is less than $(V_{in,rms})_{HL}$ for 25 ms – see Figure 2 and Figure 4). Not only the PWM gain is modified,

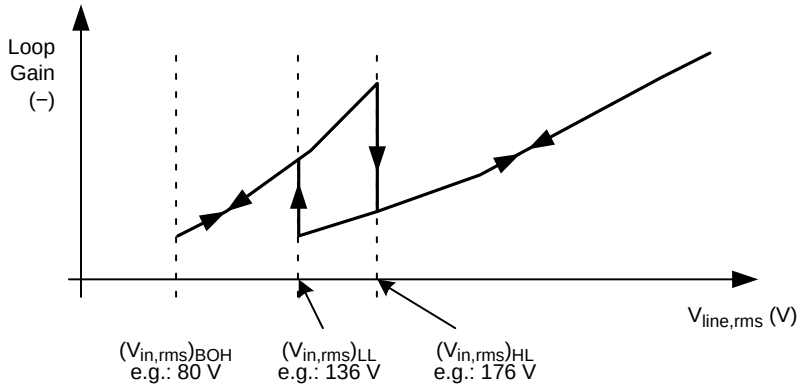

Figure 2. 2-Step Feed-Forward Limits the Loop Gain Variation with Respect to Line

Using small signal methods described in [1] and [2], we can derive two small-signal transfer functions of our PFC stage (one for High Line, one for Low Line):

- Low-Line Small Signal Transfer Function:

(eq. 23)

$$\frac{V_{out}(s)}{V_{control}(s)} = \frac{V_{in,rms}^{2} \cdot R_{load}}{640000 \cdot L \cdot V_{out,nom}} \cdot \frac{1}{1 + s \cdot \frac{R_{load} \cdot C_{bulk}}{2}}$$

- High-Line Small Signal Transfer Function:

(eq. 24)

$$\frac{V_{out}(s)}{V_{control}(s)} = \frac{V_{in,rms}^{2} \cdot R_{load}}{1920000 \cdot L \cdot V_{out,nom}} \cdot \frac{1}{1 + s \cdot \frac{R_{load} \cdot C_{bulk}}{2}}$$

Where:

C_{bulk} is the bulk capacitor.

R_{load} is the load equivalent resistance.

L is the PFC coil inductance.

$V_{out,nom}$ is the nominal regulation level of the PFC output.

The coefficient 640000 is for $t_{ON,max}$ = 12.5 μs and 1920000 for $t_{ON,max}$ = 12.5 μs/3 (product versions [*D*],[*E*]&[*F*] (The EVB is provided with the [*F*] version which is the default version), for other product versions with different $t_{ON,max}$, just calculate the new coefficient using the formula 8 V/$t_{ON,max}$ e.g. 640000 = 8 V/12.5 μs).

PFC stages must be slow. More practically, high PF ratios require the low regulation bandwidth to be in the range of 20 Hz or lower. Hence, sharp variations of the load result in excessive over and under-shoots. These deviations are effectively contained by the NCP1602 ***Dynamic Response Enhancer*** together with its accurate over-voltage protection.

Still however, a type-2 compensation (R_1,C_1,C_2) is recommended as shown in Figure 3.

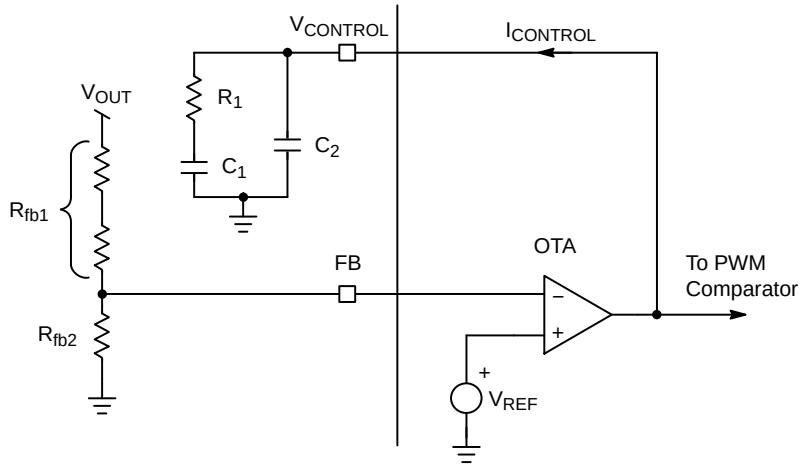

Figure 3. Regulation Trans-Conductance Error Amplifier, Feed-Back and Compensation Network

The output to control transfer function brought by the type-2 compensator is:

$$\frac{V_{control}(s)}{V_{out}(s)} = \frac{R_1 C_1}{R_0 (C_1 + C_2)} \cdot \frac{1 + \frac{1}{sR_1C_1}}{\left(1 + sR_1 \cdot \frac{C_1C_2}{C_1+C_2}\right)} \quad \text{(eq. 25)}$$

Where ($R_0 = V_{out,nom} / (V_{ref} \cdot G_{EA})$), G_{EA} being the 200-µS error amplifier transconductance gain, $V_{out,nom}$, the bulk nominal voltage and V_{REF}, the OTA 2.5-V voltage reference.

Applying the compensation method described in [2] and [3] we obtain the following dimensioning equations:

$$G_0 = \frac{\left(V_{line,rms}\right)_{LL}^{2} \cdot R_{load,min}}{640000 \cdot L \cdot V_{out,nom}} \quad \text{(eq. 26)}$$

$$C_2 = \frac{G_0 \cdot \tan\left(\frac{\pi}{2} - \phi_m\right)}{2 \cdot \pi^2 \cdot f_c^{\,2} \cdot R_{load,min} \cdot C_{bulk} \cdot R_0}$$

$$C_1 = \frac{G_0}{2 \cdot \pi \cdot f_c \cdot R_0} - C_2$$

$$R_1 = \frac{R_{load,min} \cdot C_{bulk}}{2 \cdot C_1}$$

Where:

$(V_{line,rms})_{LL}$ is the rms voltage of the line when at its lowest level (90 V in our case).

G_0 is static gain at the lowest level of the line ($(V_{line,rms})_{LL}$).

ϕ_m is phase margin (in radians).

f_c is the targeted crossover frequency

$R_{load,min}$ is the load equivalent resistor at full load:

$$R_{load,min} = \frac{V_{out,nom}^{\,2}}{P_{out,max}} = \frac{399^2}{160} \cong 995$$

The crossover frequency is selected as low as possible but higher or equal to the PFC boost stage pole at full load:

$$f_p = \frac{1}{\pi \cdot R_{load,min} \cdot C_{bulk}} \cong 2.4 \text{ Hz}$$

The phase margin is generally set between 45 and 70 degrees.

In our application, if we target a 15-Hz crossover frequency and a 60-degree phase margin (π/3 in radians), we have:

$$G_0 = \frac{90^2 \cdot 950}{640000 \cdot 200 \cdot 10^{-6} \cdot 390} \cong 154 \quad \text{(eq. 27)}$$

$$C_2 = \frac{154 \cdot \tan\left(\frac{\pi}{2} - \frac{\pi}{3}\right)}{2 \cdot \pi^2 \cdot 14^2 \cdot 950 \cdot 136 \cdot 10^{-6} \cdot 780 \cdot 10^3} \cong$$

$$\cong 200 \text{ nF} \Rightarrow \text{ Let's Choose 220 nF.}$$

$$C_1 = \frac{154}{2 \cdot \pi \cdot 15 \cdot 780 \cdot 10^3} - C_2 \cong$$

$$\cong 1.9 \text{ µF} \Rightarrow \text{ Let's Choose 2.2 µF.}$$

$$R_1 = \frac{950 \cdot 136 \cdot 10^{-6}}{2 \cdot 2.2 \cdot 10^{-6}} \cong 29 \text{ kΩ} \Rightarrow \text{Let's Choose 22 kΩ.}$$

Soft and Fast Overvoltage Protection (SOVP & FOVP):

These functions check that the output voltage is within the proper regulation window by the monitoring of FB pin voltage:

- The Fast Over-Voltage Protection (FOVP) trips if the bulk voltage reaches an abnormally high level ($V_{out,fovp}$ = 107% · $V_{out,nom}$) and disables de DRV pin (t_{ON} = 0) hence the name Fast.

When the feedback network is properly designed and correctly connected, the bulk voltage cannot exceed the level set by the Soft OVP function ($V_{out,sovp}$ = 105% · $V_{out,nom}$). If soft OVP threshold is reached, for example during no-load start-up, the on-time is gradually reduced instead of disabling the drive pin (t_{ON} = 0) hence the name soft. The FOVP threshold is set 2% higher than the soft OVP comparator.

Undervoltage Protection (UVP):

At start-up, the DRV pin is enabled if V_{FB} rises above an internal threshold voltage named V_{UVPH} (V_{UVPH} = 625 mV).

After start-up, the DRV pin is disabled if V_{FB} drops below an internal threshold voltage named V_{UVPL} (V_{UVPL} = 300 mV).

Second Overvoltage Protection (OVP2):

A second overvoltage protection (OVP2) is added for redundancy and safety reasons. The OVP2 is using the pin CS/ZCD voltage. During demagnetization time, the CS/ZCD voltage is roughly equal to $K_{CS}V_{out}$ if we neglect the voltage drop across the boost diode. If the CS/ZCD voltage rises above an internal OVP2 threshold named V_{OVP2H} the power MOSFET drive is disabled for 800 µs and enabled after the 800-µs period if the CS/ZCD voltage sensed during demagnetization time has fallen under V_{OVP2H} internal low voltage reference for OVP2 protection.

It is recommended that the parameter K_{CS} be equal to the value 138 for the circuitry processing the CS/ZCD voltage to work well.

$$K_{CS} = \frac{R_{CS1} + R_{CS2}}{R_{CS2}} \quad \text{(eq. 28)}$$

Targeting K_{CS} = 138, the following values have been found:

R_{CS1} = 5.1 MΩ + 240 kΩ + 240 kΩ

R_{CS2} = 39 kΩ

We finally get:

K_{CS} = 143.1

It has to be mentioned that [(R_{CS2} || R_{CS1}) + R_{CS0}]. C_{CS} must be kept close to a 500-ns time constant.

C_{CS} being the total capacitance between pin CS/ZCD and pin GND. The parasitic capacitance of this pin being estimated to be 10 pF then, if no external capacitor is added:

$$\left[\left(R_{CS2} \parallel R_{CS1}\right) + R_{CS0}\right] \cdot C_{CS} = 487\ \text{ns} \quad \text{(eq. 29)}$$

If an additional ceramic capacitor is added between pin CS/ZCD and pin GND, its capacitance value must be added to the 10-pF parasitic capacitance of the previous formulas.

The reason of meeting this time constant value is that there is an internal circuitry connected to the pin CS/ZCD which cancels the pole made by R_{CS2} + R_{CS0} and the CS/ZCD to GND total capacitance (C_{CS}).

Taking K_{CS} = 143.1 and the OVP2 internal threshold levels V_{OVP2H} = 3.175 V and V_{OVP2L} = 3.093 V we can calculate the two OVP2 thresholds for V_{out} (also named V_{bulk}):

$$V_{out,OVP2H} = K_{CS} \cdot V_{OVP2H} = 143.1 \cdot 3.175 = 454.3\ \text{V} \quad \text{(eq. 30)}$$

$$V_{out,OVP2L} = K_{CS} \cdot V_{OVP2L} = 143.1 \cdot 3.093 = 442.6\ \text{V} \quad \text{(eq. 31)}$$

These threshold must be placed well above the Fast OVP threshold in order to be operational in case of an OVP failure, due for example to wrong FB resistor value or to FB resistor failure. The higher Fast OVP threshold being equal to 108% of $V_{out,nom}$ and for $V_{out,nom}$ = 400 V, this will give 1.08 × 400 = 432 V which is lower than the lower OVP2 threshold of 442.6 V.

The values of R_{CS1} and R_{CS2} must be chosen high for not consuming too much power during standby.

During standby, there is no switching and the voltage seen by R_{CS1} in series with R_{CS2} is a constant voltage equal to:

$$V_{mains,rms} \cdot \sqrt{2}$$

The power consumed during standby $P_{CS,STBY}$ being given by:

$$P_{CS,STBY} = \frac{\left(V_{mains,rms} \cdot \sqrt{2}\right)^2}{R_{CS1} + R_{CS2}} \quad \text{(eq. 32)}$$

With:

R_{CS1} = 5.1 MΩ + 240 kΩ + 240 kΩ

R_{CS2} = 39 kΩ

We get:

For $V_{mains,rms}$ = 86 V this will give $P_{CS,STDBY}$ = 2.6 mW

For $V_{mains,rms}$ = 110 V this will give $P_{CS,STDBY}$ = 4.3 mW

For $V_{mains,rms}$ = 230 V this will give $P_{CS,STDBY}$ = 18.8 mW

For $V_{mains,rms}$ = 265 V this will give $P_{CS,STDBY}$ = 25.0 mW

CSZCD Resistors Bridge – Resistor value choice and PCB layout guideline

When the R_{CS} resistor bridge totals a resistance in the MΩ range, it is very sensitive to parasitic capacitances as low as few hundreds of fF. Parasitic capacitances can be found between R_{CS} resistors nodes and (GND or power MOSFET drain). These parasitic capacitances effect can lead to permanent false fault detection events: OCP, OVS or OVP2 triggering, making the controller unable to operate and regulate V_{out} properly.

One easy way to avoid the effect of parasitic capacitors is to reduce the value of the resistors, while keeping the dividing ratio K_{CS} around 138. Reducing the CS/ZCD bridge resistors value (reducing R_{CS1} + R_{CS2}) is at the expense of standby power consumption which will increase.

If R_{CS1} + R_{CS2} value is well under 1 MΩ, three 200-V SMD1206 resistors can be placed in series but **when the R_{CS1} + R_{CS2} value is above 1 MΩ** it has been found that the three SMD 200-V resistors in series lead to false fault tripping (e.g. OVP2 false triggering). In that case, it is advised to have one 500-V SMD high-value resistor on the drain side (e.g. 5.1 MΩ for The EVB) with two low value (e.g. 240 kΩ) 200-V SMD resistors in series like the values used in the previous calculations. This is to avoid inter-resistor capacitance to GND to have difficulties to be discharged before a t_{ON} cycle. Experience shows that it is not recommended to **follow the common sense reasoning of using 3 equal value resistors to balance the drain voltage.**

Bench experiments have proven SMD1206 & 0805 superiority, parasitic capacitance wise, over trough hole resistors for R_{CS1}, R_{CS2} and R_{CS0} resistors.

R_{CS0} must be placed as close as possible to CS/ZCD pin voltage and R_{CS1} and R_{CS2} as close as possible to R_{CS0}.

PCB traces connecting the R_{CSi} resistors must be kept as short as possible, the width of the trace being as small as possible (minimum parasitic capacitance)

It is wise to keep a safety distance of 1 cm between the high value resistors of the CSZCD brige and DRV, V_{in}, V_{drain} copper traces to avoid coupling.

Note than while decreasing the value of R_{CS1} and R_{CS2}, R_{CS0} must be increased in order to meet the 500-ns time constant made with R_{CS} resistor and C_{CS} total capacitance.

STEP 4: INPUT VOLTAGE SENSING – BROWN-OUT

In a boost converter, considering a zero inductor average voltage at steady state,averaged drain voltage is equal to the V_{in} voltage (rectified V_{line} voltage) .

The V_{CSint} voltage of Figure 4 is equal to $R_{sense} \cdot I_{ind}$ during the on-time and equal to V_{drain}/K_{CS} during off-time.

Thanks to the DRV driven switches, the input of the R_{sns}/C_{sns} low pass filter will be $v_{drain}(t)/K_{CS}$ and the output of the same filter $v(t)$ will be $v_{in}(t)/K_{CS}$ or abs$(v_{line}(t)/K_{CS})$

$$V_{SNS}(t) = \text{Abs}\left(\frac{V_{line}(t)}{K_{CS}}\right) \quad \text{(eq. 33)}$$

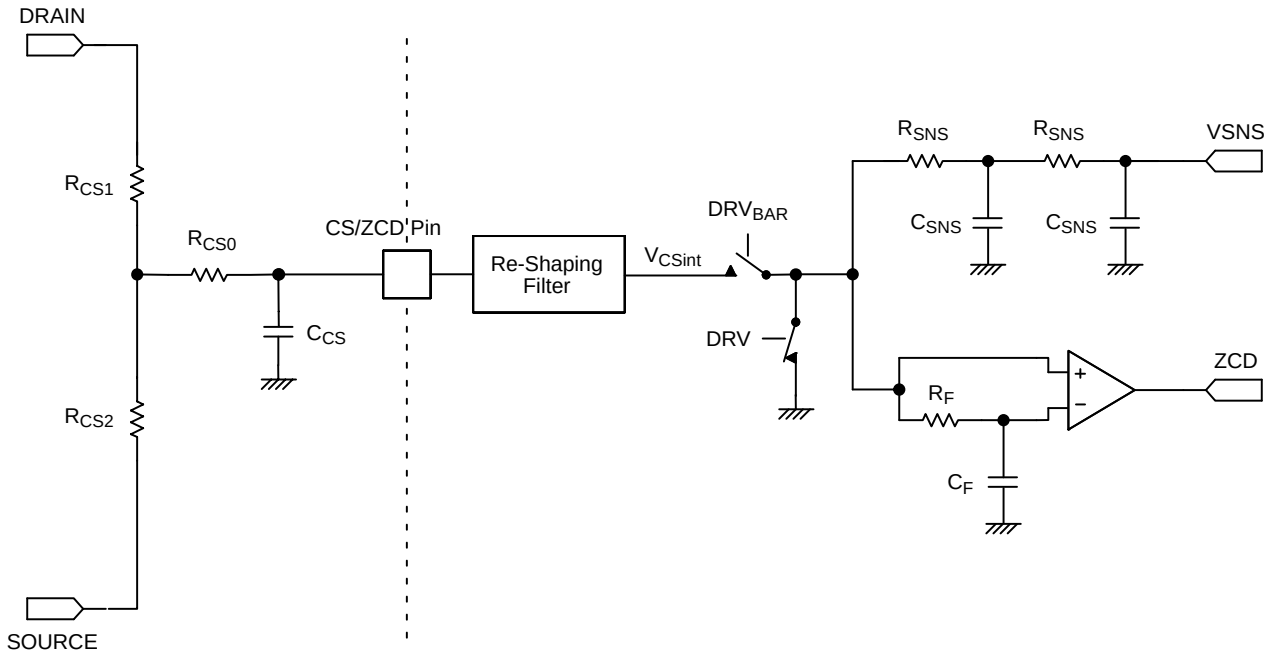

Figure 4. Brown-Out and Line Range Detection Block

The product codes [C**] and [D**] have the Brown-out feature enabled. There are two brown-out levels, high and low.

By default and before start-up, the brown-out is enabled. When V_{SNS} (V_{SNS} is a low-pass filtered scaled down V_{line}) sensed thru CS/ZCD pin goes higher than the internal reference voltage V_{BOH} = 819 mV the brown-out is reset and allows the controller to start switching. After brown-out is reset, and switching activity starts, V_{line} continues to be sensed thru CS/ZCD pin and when V_{SNS} falls under the brown-out internal reference voltage V_{BOL} = 737 mV for 50 ms, then brown-out is enabled. After brown-out is confimed, drive pulses are not immediately disabled, instead, a 30-μA current source is applied to the VCTRL pin to gradually reduce V_{ctrl}. As a result, the circuit only stops pulsing when the static OVP function is activated (that is when V_{ctrl} reaches the SKIP detection threshold). At that moment, the circuit stops switching. This method limits any risk of false tripping. The following formulas are showing

how internal brown-out reference voltages translate to line rms voltage thresholds.

$$\left(V_{line,rms}\right)_{BOH} = \frac{K_{CS} \cdot V_{BOH}}{\sqrt{2}} = \frac{143.1 \cdot 0.819}{\sqrt{2}} = 83\ V \quad \text{(eq. 34)}$$

$$\left(V_{line,rms}\right)_{BOL} = \frac{K_{CS} \cdot V_{BOL}}{\sqrt{2}} = \frac{143.1 \cdot 0.734}{\sqrt{2}} = 74\ V \quad \text{(eq. 35)}$$

Where:

V_{BOH} is the 819-mV upper brown-out internal threshold.

V_{BOL} is the 734-mV lower brown-out internal threshold.

High and Low Line Detection

An internal digital flag named LLINE is used to detect if the line voltage is low (LLINE = 1) or high (LLINE = 0). This flag is used to change the on-time in order to realize a two-level line feed-forward and reduce the spread of the small signal open-loop cut-off frequency. There is also an abrupt change in VCTRL when transitioning from high line to low line and vice versa. Like in the brown-out detection circuit, the internal V_{SNS} is compared to two levels defining an hysteresis between high line and low line states. When V_{SNS} goes above V_{HL} = 1.801 V, the controller enters the high line state and when V_{SNS} goes under V_{LL} = 1.392 V it toggles into the the low line state. Translation of high line to low line thresholds and vice versa into line rms voltage is given by the following equations.

Low line to high line threshold is:

$$\left(V_{line,rms}\right)_{HL} = \frac{K_{CS} \cdot V_{HL}}{\sqrt{2}} = \frac{143.1 \cdot 1.801}{\sqrt{2}} = 182\ V \quad \text{(eq. 36)}$$

High line to low line threshold is:

$$\left(V_{line,rms}\right)_{LL} = \frac{K_{CS} \cdot V_{LL}}{\sqrt{2}} = \frac{143.1 \cdot 1.392}{\sqrt{2}} = 141\ V \quad \text{(eq. 37)}$$

X2 Capacitors Discharge:

R_{X1} and R_{X2} are designed for safety considerations. In general, they must be selected so that the series combination of ($R_{X1} + R_{X2} = 2R_X$) form with the X2 EMI capacitors a time constant less than 3 s (?? Habituellement, la norme impose une constant de temps de 1 s). In our case, two 1-MΩ resistors ($R_{X1} = R_{X2} = R_X$ = 1 MΩ) are implemented so that with the selected X2 capacitors, it leads to a 1.8-s discharge time constant, which offers a comfortable margin.

STEP 5: CURRENT SENSE NETWORK

The current sense circuitry consists of a current sensing resistor R_{sense}.

=> Computing R_{sense}

The circuit detects an over-current situation if the voltage across the current sense resistor exceeds 0.5 V. Hence:

$$R_{sense} = \frac{0.5}{\left(I_{L,pk}\right)_{max}} \quad \text{(eq. 38)}$$

Combining this equation with Equation 8 leads to:

$$R_{sense} = \frac{\left(V_{line,rms}\right)_{LL}}{4\sqrt{2} \cdot \left(P_{in,avg}\right)_{max}} \quad \text{(eq. 39)}$$

In our practical case,

$$R_{sense} = \frac{90}{4\sqrt{2} \cdot 170} \cong 0.094\ \Omega \quad \text{(eq. 40)}$$

In order to have a bit of margin, a 80-mΩ resistor is selected.

R_{sense} losses can be computed using the equation giving the MOSFET conduction losses where R_{sense} replace $R_{DS(on)}$:

$$\left(P_{R_{cs}}\right)_{max} = \frac{4}{3} \cdot R_{sense} \cdot \left(\frac{\left(P_{in,avg}\right)_{max}}{\left(V_{line,rms}\right)_{LL}}\right)^2 \cdot \left(1 - \frac{8\sqrt{2} \cdot \left(V_{line,rms}\right)_{LL}}{3\pi \cdot V_{out,nom}}\right) \quad \text{(eq. 41)}$$

Hence, our 80-mΩ current sense resistor will dissipate about 278 mW at full load, low line.

=> Zero Current Circuitry

The ZCD circuitry is show in Figure 5. The basic idea is to get the ZCD information from V_{drain} voltage crossing the V_{in} voltage. V_{drain} and V_{in} voltages being external to the controller, the schematic of Figure 5 will bring these voltages internally but scaled-down by K_{CS}.

$$K_{CS} = \frac{R_{CS1} + R_{CS2}}{R_{CS2}} \quad \text{(eq. 42)}$$

In a boost converter, the averaged drain voltage which is one pin of the boost inductor is equal to the V_{in} voltage which is on the other pin of the boost inductor and this is because the average voltage drop across the inductor is zero volts if we neglect the series resistance of the inductor.

Scaled-down drain voltage is brought inside the controller by R_{CS1}, R_{CS2} bridge and the re-shaping filter so the internal node voltage V_{CSint} will be:

$$V_{CSint}(t) = \frac{1}{K_{CS}} \cdot V_{drain}(t) \quad \text{(eq. 43)}$$

Thanks to a low pass filter the two inputs of the ZCD comparator will be like comparing $V_{in}(t)$ and $V_{drain}(t)$:

$$V^-(t) = \frac{1}{K_{CS}} \cdot V_{in}(t)$$
$$V^+(t) = \frac{1}{K_{CS}} \cdot V_{drain}(t) \quad \text{(eq. 44)}$$

The ZCD digital signal resulting from the comparison $V_{in}(t)$ and $V_{drain}(t)$ is used for synchronizing the power MOSFET turn-on. The power MOSFET turn-on event is synchronized with the falling edge of ZCD signal.

The only thing to care about is that K_{CS} value is as close as possible to 138, to ensure a correct operation of the ZCD comparator.

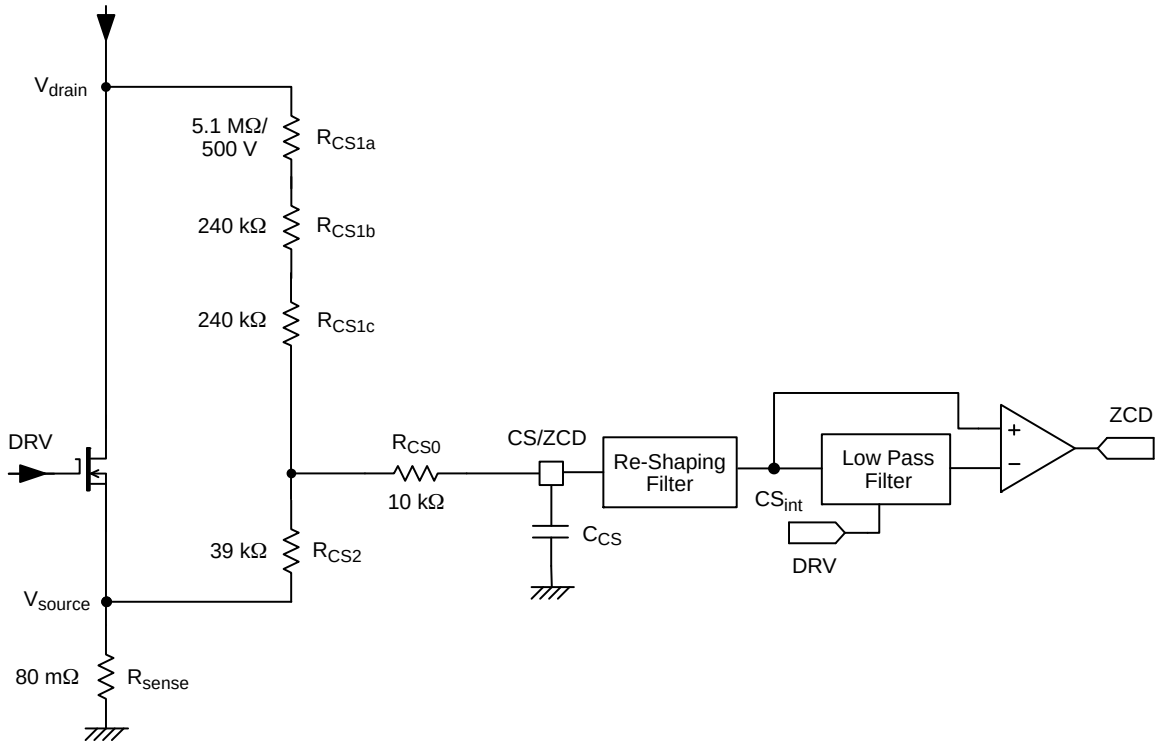

Figure 5. NCP1602 Zero Crossing Detection with Typical Component Values

The NCP1602 integrates leading edge blanking on the CS/ZCD pin that prevents the need for a filtering capacitor. No any capacitor is allowed in the CS/ZCD circuitry as this will result in distorting the CS/ZCD signal leading to wrong or no ZCD detection. Care must be taken when probing the CS/ZCD signal with a scope probe as the scope probe will add typically a 10-pF capacitance in parallel with the package parasitic capacitance C_{CS}. This additional capacitance will distort the CS/ZCD signal and result in degraded ZCD detection performance (we may lose demagnetization detection and start triggering a 200 μs watchdog timer, and also loose valley turn-on).

Using the Auxiliary Winding Voltage V_{aux} for the CSZCD Circuitry

It is possible to use the schematic shown in Figure 6 to generate the signal of CS/ZCD pin.

Thanks to the auxiliary winding voltage capacitor C_{aux}, resistor R_{aux} and diode D_{aux1}, it is possible to generate at the cathode of D_{aux1} diode a voltage equal to the power MOSFET drain voltage multiplied by the auxiliary (N_{aux}) to primary (N_{prim}) transformer turns ratio. The parameter K_{CS} previously described is now defined by:

$$K_{CS} = \frac{N_{prim}}{N_{aux}} \cdot \frac{R_{CS1} + R_{CS2}}{R_{CS2}} \qquad \text{(eq. 45)}$$

K_{CS} = 138 must always be the target value.

This new K_{CS} formula allows to use ten times a lower R_{CS1} value, given the fact that N_{prim}/N_{aux} = 10 for the transformer used on our EVB. With this approach, a lower voltage is carried and also low R_{CS1} values reduce the sensitivity to parasitic capacitors.

One benefit of this circuitry is that there is no current consumption during standby (No switching activity hence no V_{aux} voltage).

It has to be mentioned that product version with brown-out feature activated will not operate with this circuitry so product versions [C**] and [D**] must not be used with this V_{aux} circuitry.

Everything else will work exactly the same as already described when the power MOSFET drain voltage is used instead of auxiliary voltage V_{aux}. It is just that K_{CS} formula is slightly different.

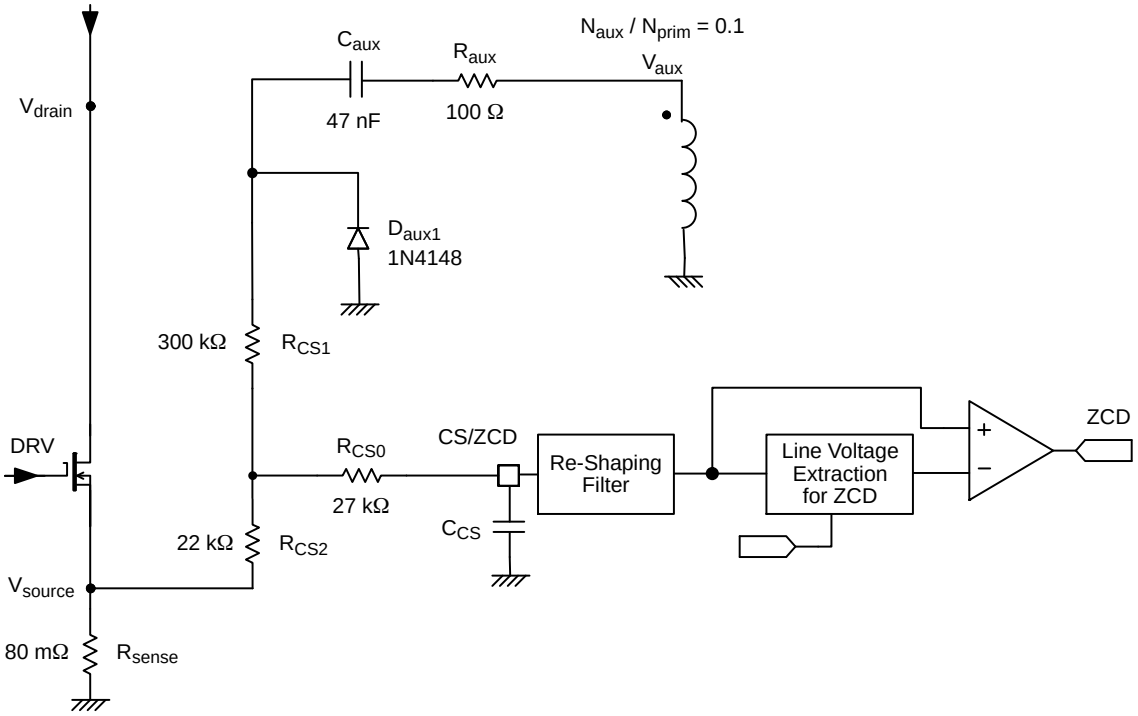

Figure 6. CS/ZCD Circuitry using Auxilliary Winding Voltage with Typical Components Values

Layout and Noise Immunity Considerations

The NCP1602 is not particularly sensitive to noise. However, usual layout rules for power supply design apply. Among them, let us remind the following ones:

- The loop area of the power train must be minimized.
- Star configuration for the power ground that provide the current return path.
- Star configuration for the circuit ground.
- The circuit ground and the power ground should be connected by one single path, no loop is allowed.
- This path should preferably connect the circuit ground to the power ground at a place that is very near the grounded terminal of the current sense resistor (R_{sense}).
- A 100 or 220-nF capacitor should be placed between the circuit V_{CC} and GND pins, with minimized connection length.
- The R_{CSx} resistors must be placed as close as possible to the CS/ZCD pin, and capacitance coupling with GND or any other signal must be avoided.
- It is recommended to place a filtering capacitor on the FB pin to protect the pin from possible surrounding noise. It must be small however not to distort the voltage sensed by the FB pin. See the corresponding sections for more details.

SUMMARY OF THE MAIN EQUATIONS

Table 1. DESIGN STEPS TABLE

Step	Components	Formula	Comments
Step 1: Key Specifications	• f_{line}: Line frequency. It is often specified in a range of 47−63 Hz for 50 Hz/60 Hz applications. • $(V_{line,rms})_{LL}$: Lowest Level of the line voltage, e.g., 90 V. • $(V_{line,rms})_{HL}$: Highest Level for the line voltage (e.g., 264 V in many countries). • $(V_{line,rms})_{BOH}$: Brown-Output Line Upper Threshold. The circuit prevents operation until the line rms voltage exceeds this level. • $V_{out,nom}$: Nominal Output Voltage. • $(\delta V_{out})_{pk\text{-}pk}$: Peak-to-Peak output voltage low-frequency ripple. • $t_{HOLD\text{-}UP}$: Hold-up Time that is the amount of time the output will remain valid during line drop-out. • $V_{out,min}$: Minimum output voltage allowing for operation of the downstream converter. • $P_{out,max}$: Maximum output power consumed by the PFC load, that is, 160 W in our application. • $(P_{in,avg})_{max}$: Maximum power absorbed from the mains in normal operation. Generally obtained at full load, low line, it depends on the efficiency that, as a rule of a thumb, can be set to 95%.		
Step 2: Power Components	Input Diodes Bridge Losses	$P_{bridge} = 2 \cdot V_f \cdot \frac{2\frac{\sqrt{2}}{\pi} \cdot \frac{P_{out}}{\eta}}{V_{line,rms}} \approx \frac{1.8 \cdot V_f}{V_{line,rms}} \cdot \frac{P_{out}}{\eta}$	V_f is the forward voltage of any diode of the bridge. It is generally in the range of 1 V or less.
	Inductor	$L \le \frac{\left(V_{line,rms}\right)_{LL}^2}{2 \cdot \left(P_{in,avg}\right)_{max}} \cdot T_{on,max}$ $\left(I_{L,pk}\right)_{max} = 2 \cdot \sqrt{2} \cdot \frac{\left(P_{in,avg}\right)_{max}}{\left(V_{line,rms}\right)_{LL}}$ $\left(I_{L,rms}\right)_{max} = \frac{\left(I_{L,pk}\right)_{max}}{\sqrt{6}}$	In our application $L \le \frac{:90^2}{2 \cdot 170} \cdot 12.5\ \mu = 295\ \mu H$ $\left(I_{L,pk}\right)_{max} = 2 \cdot \sqrt{2} \cdot \frac{170}{90} \cong 5.3\ A$ $\left(I_{L,rms}\right)_{max} = \frac{5.3}{\sqrt{6}} \cong 2.2\ A$
	MOSFET Conduction Losses	$(P_{on})_{max} = \frac{4}{3} \cdot R_{DS(on)} \cdot \left(\frac{P_{out,max}}{\eta \cdot \left(V_{line,rms}\right)_{LL}}\right)^2 \cdot$ $\cdot \left(1 - \frac{8\sqrt{2} \cdot \left(V_{line,rms}\right)_{LL}}{3\pi \cdot V_{out,nom}}\right)$	$R_{DS(on)}$ is the drain-source on-state resistance of the MOSFET
	Bulk Capacitor Constraints	$C_{bulk} \le \frac{P_{out,max}}{\left(\delta V_{out}\right)_{pk-pk} \cdot \omega \cdot V_{out,nom}}$ $C_{bulk} \ge \frac{2 \cdot P_{out,max} \cdot t_{HOLD-UP}}{V_{out,nom}^2 - V_{out,min}^2}$ $\left(I_{c,rms}\right)_{max} \cong$ $\cong \sqrt{\left[\sqrt{\frac{32\sqrt{2}}{9\pi}} \cdot \frac{\left(P_{in,avg}\right)_{max}}{\sqrt{\left(V_{line,rms}\right)_{LL} \cdot V_{out,nom}}}\right]^2 - \left(\frac{P_{out,max}}{V_{out,nom}}\right)^2}$	These 3 equations quantify the constraints resulting from the low-frequency ripple ($(\delta V_{out})_{pk\text{-}pk}$ that must be kept below 8%), the hold-up time requirement and the rms current to be sustained.

Table 1. DESIGN STEPS TABLE (continued)

Step	Components	Formula	Comments
Step 3: Bulk Voltage Monitoring and Regulation Loop	Resistor Divider	$R_{fb2} = \frac{2.5}{I_{FB}}$ $R_{fb1} = R_{fb2} \cdot \left(\frac{V_{out,nom}}{V_{REF}} - 1 \right)$ $C_{fb} \leq \frac{1}{150 \cdot \left(R_{fb1} \parallel R_{fb2} \right) \cdot f_{line}}$	I_{FB} is the bias current that is targeted within the resistor divider. Values in the range of 50 μA to 100 μA generally give a good trade-off between losses and noise immunity.
	Compensation	$G_0 = \frac{\left(V_{line,rms} \right)_{LL}^{2} \cdot R_{load,min}}{640000 \cdot L \cdot V_{out,nom}}$ $C_2 = \frac{G_0 \cdot \tan\left(\frac{\pi}{2} - \phi_m \right)}{2 \cdot \pi^2 \cdot f_c^{\,2} \cdot R_{load,min} \cdot C_{bulk} \cdot R_0}$ $C_1 = \frac{G_0}{2 \cdot \pi \cdot f_c \cdot R_0} - C_2$ $R_1 = \frac{R_{load,min} \cdot C_{bulk}}{2 \cdot C_1}$	C_{FB} is the filtering capacitor that can be placed between the FB pin and ground to increase the noise immunity of this pin. (see Figure 3)
	OVP and UV OVP 2	107% of $V_{out,nom}$ for OVP $V_{out,UVPx} = K_{FB} \cdot V_{UVPx}$ $V_{out,OVP2x} = K_{CS} \cdot V_{OVP2x}$	OVP and UV are sensed by the feedback network (K_{FB}) as OVP2 is sensed by the CS/ZCD resistor network (K_{CS}).
Step 4: Input Voltage Sensing	Input Voltage Sensing	$K_{CS} = \frac{R_{CS1} + R_{CS2}}{R_{CS2}}$ $\left(V_{line,rms} \right)_{BOH} = \frac{K_{CS} \cdot V_{BOH}}{\sqrt{2}}$ $\left(V_{line,rms} \right)_{BOL} = \frac{K_{CS} \cdot V_{BOL}}{\sqrt{2}}$ $\left(V_{line,rms} \right)_{HL} = \frac{K_{CS} \cdot V_{HL}}{\sqrt{2}}$ $\left(V_{line,rms} \right)_{LL} = \frac{K_{CS} \cdot V_{LL}}{\sqrt{2}}$	Input voltage is sensed through the CS/ZCD pin $(V_{line,rms})_{BOH}$ line rms level above which the circuit starts operating the circuit stops switching when line rms level falls under $(V_{line,rms})_{BOL}$. When line rms voltage goes above $(V_{line,rms})_{HL}$ we enter High Line state and when line rms voltage below $(V_{line,rms})_{LL}$ we enter Low Line state

Table 1. DESIGN STEPS TABLE (continued)

Step	Components	Formula	Comments
Step 5: Current Sense Network	Input Voltage Sensing	$R_{CS} = \frac{\left(V_{line,rms}\right)_{LL}}{4\sqrt{2} \cdot \left(P_{in,avg}\right)_{max}}$ $\left(P_{R_{cs}}\right)_{max} = \frac{4}{3} \cdot R_{CS} \cdot \left(\frac{\left(P_{in,avg}\right)_{max}}{\left(V_{line,rms}\right)_{LL}}\right)^2 \cdot$ $\cdot \left(1 - \frac{8\sqrt{2} \cdot \left(V_{line,rms}\right)_{LL}}{3\pi \cdot V_{out,nom}}\right)$	$(V_{line,rms})_{LL}$ is the line rms voltage lowest level in normal condition (e.g., 90 V). $V_{out,nom}$ is the output nominal level (e.g., 390 V). $(P_{in,avg})_{max}$ is the maximum input power of your application.
	Current Controlled Frequency Fold-Back	$R_{FF} = \frac{25\sqrt{2} \cdot \left(V_{line,rms}\right)_{BOH}}{112 \cdot L \cdot \left(I_{line}\right)_{th}}$ $C_{FF} \leq \frac{1}{150 \cdot I_{line} \cdot R_{FF}}$	$(I_{line})_{th}$ is the line current level below which the NCP1612 starts reducing the frequency.

SCHEMATICS

(Detailed Schematic for our 160-W Evaluation Board, Universal Mains Application)

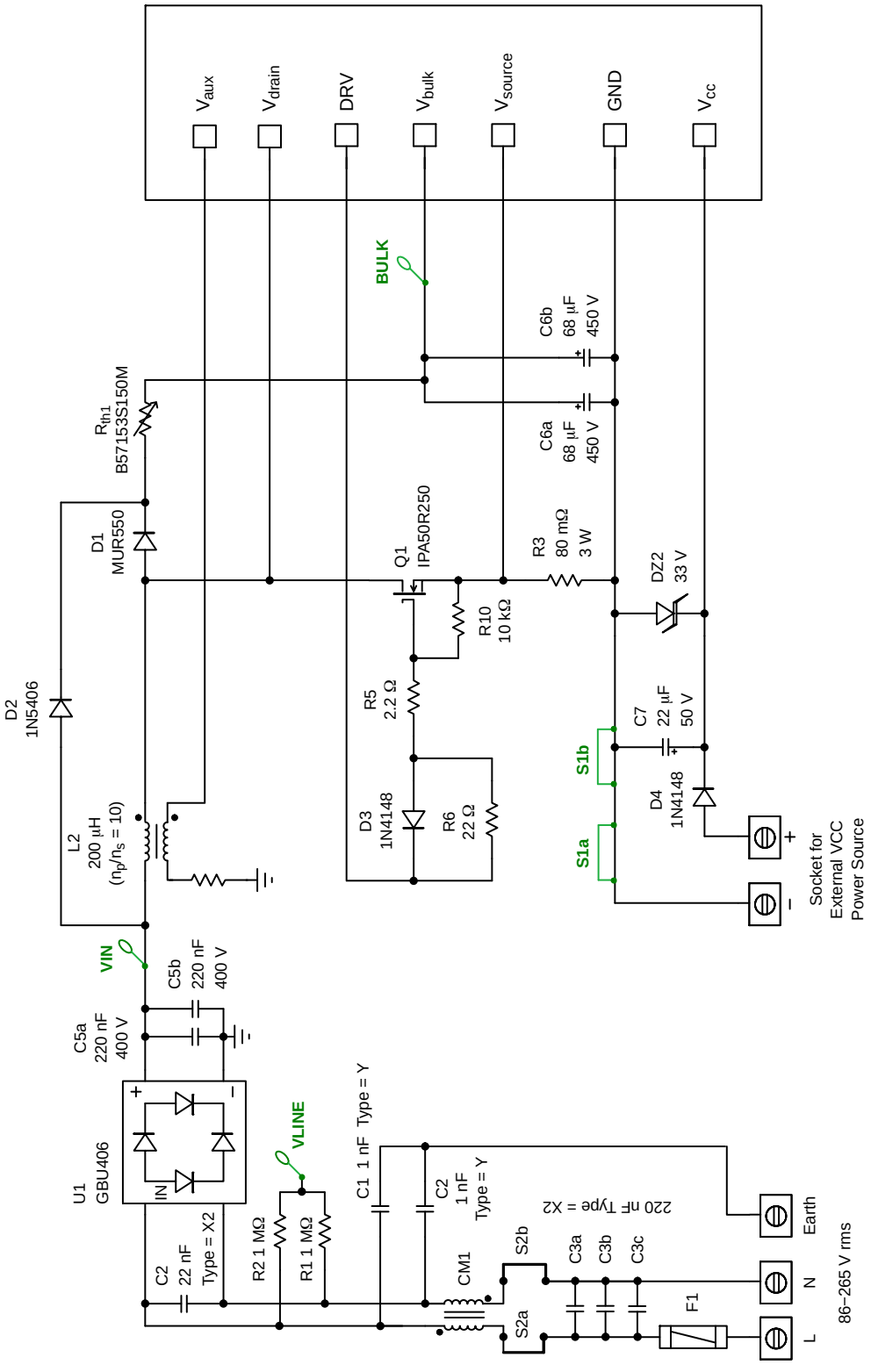

Figure 7. Application Schematic − Power Section

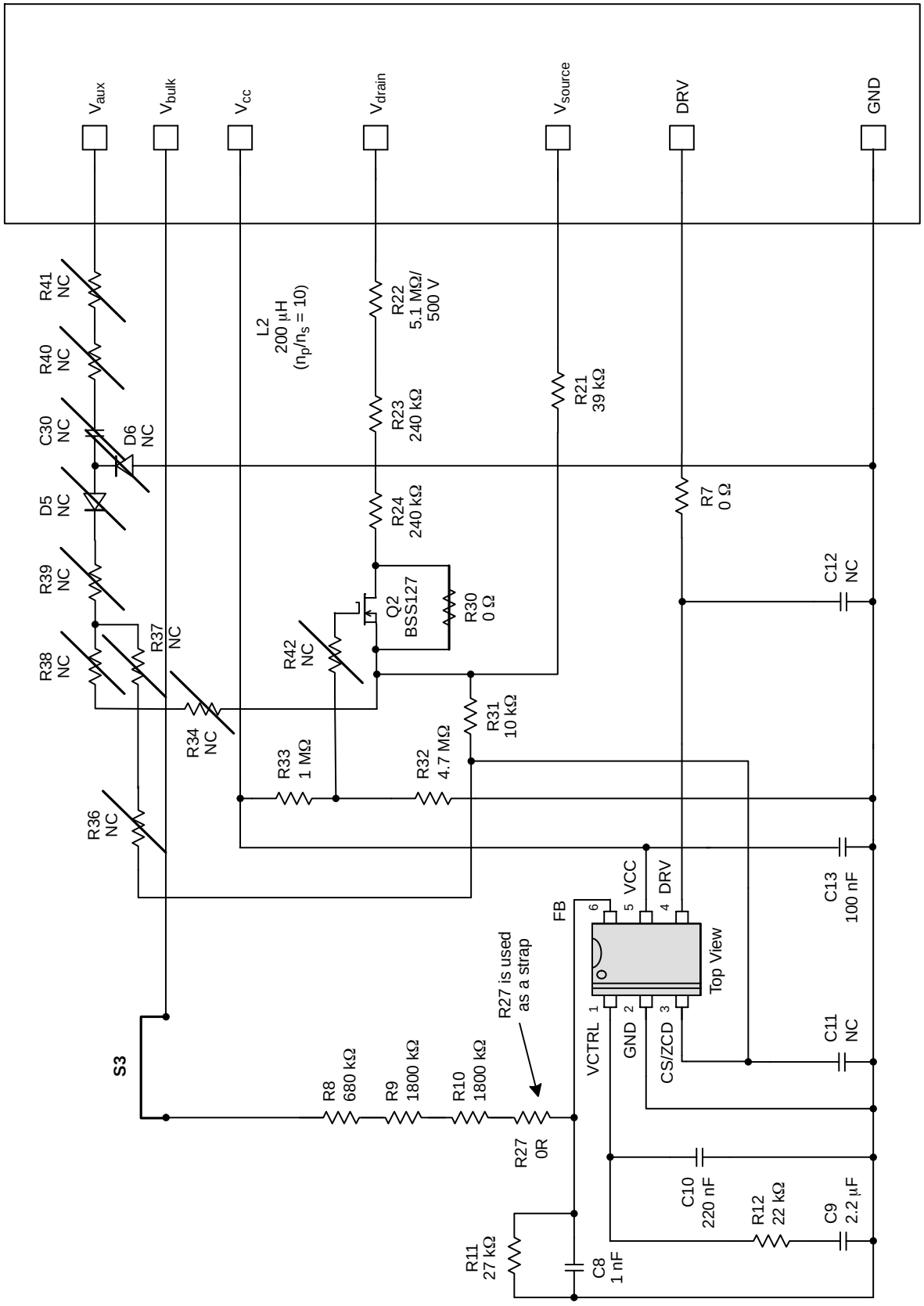

Figure 8. Application Schematic for ZCD Sensing using Power MOSFET Drain Voltage − Control Section

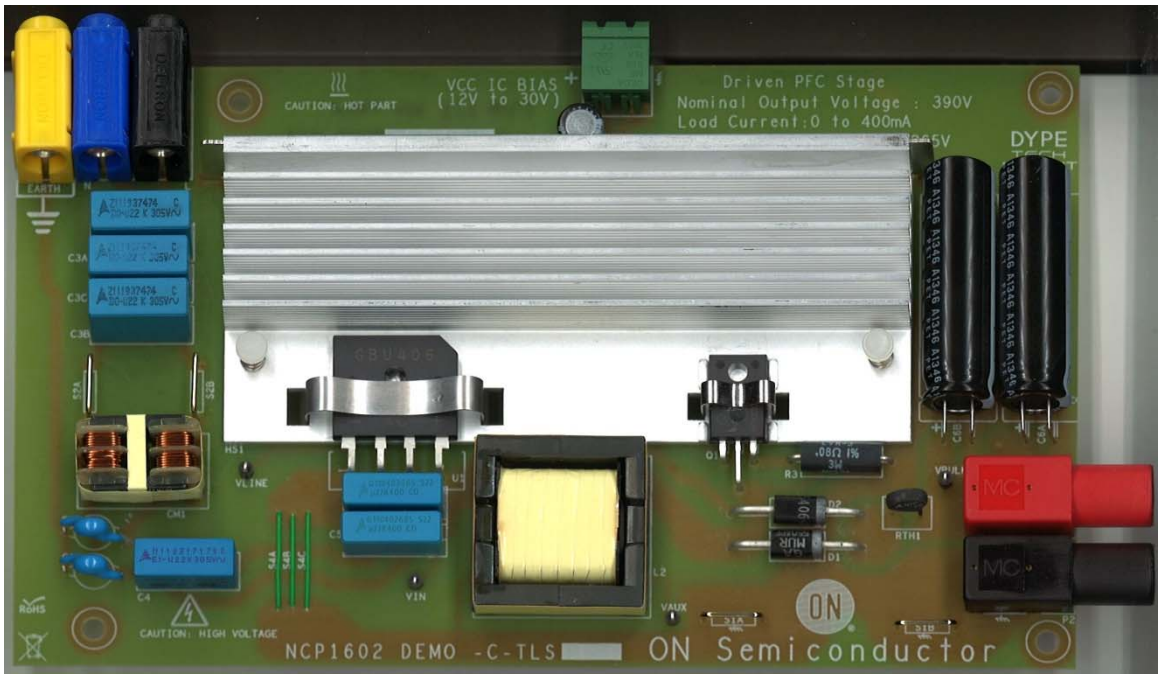

Figure 9. NCP1602 Low Profile Evaluation Board Top View Showing Power Circuitry

Figure 10. NCP1602 Low Profile Evaluation Board Bottom View Showing the Control Circuitry

CONCLUSIONS

This paper summarizes the key steps when dimensioning a NCP1602−driven PFC stage. The proposed approach being systematic, it can be easily applied to other applications.

REFERENCES

More details on the circuit operation can be found in its data sheet [4].

[1] Joel Turchi, “Safety tests on a NCP1612-driven PFC stage”, Application note AND9064/D, http://www.onsemi.com/pub_link/Collateral/AND9064−D.PDF.

[2] Joel Turchi, “Compensation of a PFC stage driven by the NCP1654”, Application note AND8321/D, http://www.onsemi.com/pub_link/Collateral/AND8321−D.PDF.

[3] Joel Turchi, “Compensating a PFC stage”, Tutorial TND382/D available at: http://www.onsemi.com/pub_link/Collateral/TND382−D.PDF.

[4] NCP1602/D Data Sheet, http://www.onsemi.com/pub_link/Collateral/NCP1602−D.PDF.

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