AND8397/D

A 90 Watt High Efficiency, Notebook Adapter Power Supply with Inherent Power Factor Correction

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APPLICATION NOTE

Introduction

This application note describes a relatively novel and simple way to produce an off−line, power factor corrected, 15 V output (and higher) power supply for notebook adapters and similar applications using an isolated, single−stage conversion topology. The power topology is essentially a buck−boost derived flyback converter operating in continuous conduction mode (CCM) and utilizing ON Semiconductor's NCP1652 controller which was designed specifically for this application. The power supply described in this application note is a 19 V, 5 A supply with universal AC input and is intended as a notebook adapter. Efficiencies approaching 90% were achieved with a power factor exceeding 0.95 for most typical loads. The supply also includes overcurrent protection, overvoltage protection, brownout detection, and an input EMI filter. The NCP1652 converter circuitry is sufficiently versatile that the basic design can be modified for LED ballast or other similar applications that require a constant voltage, constant current (CVCC) output characteristic with typical output voltages of 12 V and higher in the 25 to 150 W power range.

Background

Applications that require an isolated, regulated output voltage along with input power factor correction typically involve a two stage conversion process as depicted in Figure 1. This scheme is composed of an input boost power factor corrector stage which converts and pre−regulates the input line into a 400 Vdc bus. This bus then provides the voltage for a conventional dc−to−dc converter which can be of any appropriate topology. For lower power applications of 150 W and less, this is usually a flyback converter.

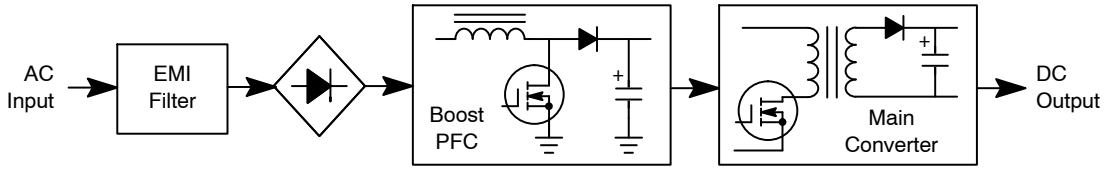


Figure 1. Conventional 2−Stage Conversion

With a few minor performance compromises, a simpler technique can be used in which the power factor and main converter sections are combined into one conversion stage by using the NCP1652 controller as shown in Figure 2.

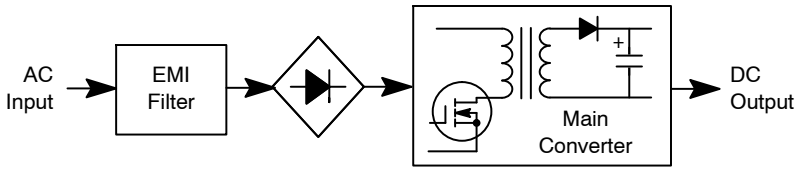
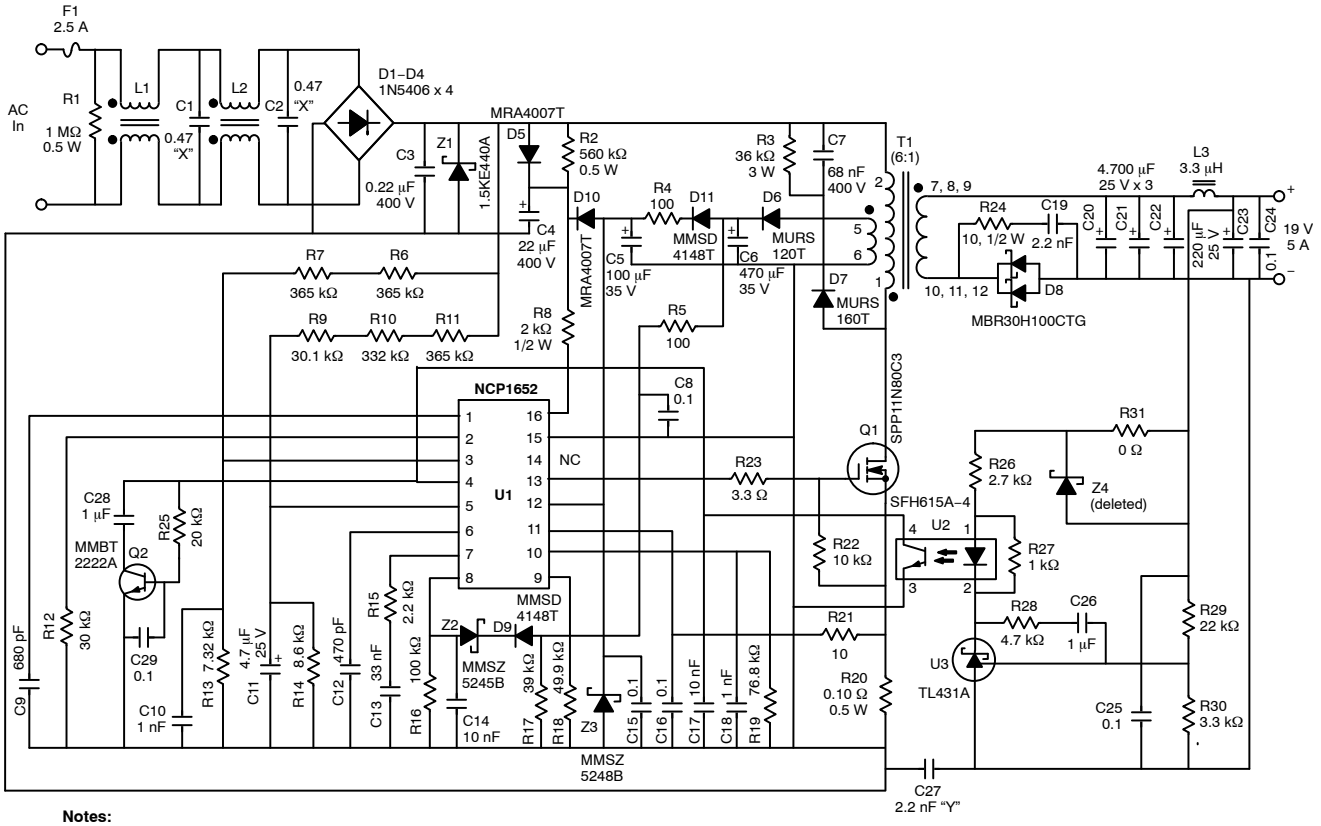


Figure 2. Single Stage Conversion with NCP1652

The difference here is that the flyback conversion stage not only handles the voltage regulation and input to output isolation functions, but provides power factor correction as well. The circuit essentially functions as a conventional PFC converter with the output being derived from a secondary winding on what would be the boost choke in the “normal” type of non−isolated PFC circuit. The dc input to the converter is a 120 Hz haversine instead of a pure dc voltage because the normal input “bulk” capacitor following the bridge rectifier is reduced to a value of less than a microfarad. The full schematic of the single stage converter is shown in Figure 3.



Notes:

1. Crossed schematic lines are not connected.
2. Heavy lines indicate power traces/planes.
3. Z2/D9 is for optional OVP.
4. L1 is Coilcraft BU10−1012R2B or equivalent.
5. L2 is Coilcraft P3221−AL or equivalent.
6. L3 is Coilcraft RFB0807−3R3L or equivalent.
7. Q1 and D8 will require small heatsinks.

NCP1652 90 Watt PFC Adapter Supply
19 Vout, 90−265 VAC Input (Rev 6)

Figure 3. Single Stage Converter Schematic

Single Stage Converter Characteristics

The single stage, isolated PFC converter can be easily configured from the conventional buck−boost derived flyback topology. The operational mode can be in discontinuous conduction mode (DCM), critical conduction mode (CRM), or continuous mode (CCM). The most common operational mode for lower power circuits is CRM because of ease of implementation of synchronous output rectification for 12 V_{out} and below. CCM, however, can offer some significant advantages for applications that require fixed frequency operation with output voltages of 15 V or higher where the use of synchronous rectification yields marginal efficiency improvements. In CCM the peak MOSFET current can be significantly less than in CRM resulting in lower switching losses, particularly in power levels above 75 W. CCM also reduces the high frequency output capacitor ripple current, and the overall conversion efficiency is generally higher. The NCP1652 controller is designed particularly for CCM operation and also provides a second gate drive output for the implementation of an active clamp snubber for higher power applications where voltage spikes caused by the flyback transformer’s leakage inductance energy can become a significant issue. The 19 V, 5 A adapter circuit of Figure 3 achieved an average efficiency approaching 90% for typical operation loads. The flyback transformer T1 was designed to effectively operate in “deep” CCM with a relatively low magnetizing current component (see Figure 8 for the transformer design details). This resulted in significantly reduced switching losses in MOSFET Q1 over a similar CRM based design.

The single stage PFC conversion process, regardless of the operational mode, has a few compromises over the traditional 2−stage conversion scheme of Figure 1. They are as follows:

1. As with any power factor corrector circuit, the gain bandwidth of the control loop is very low, typically in the 10 to 30 Hz range. This is necessary, otherwise the control loop would attempt to regulate off the 120 Hz line variations of the input and this would result in a very poor power factor. As a consequence of the low bandwidth, transient response to load step changes will be poor although dc regulation will be excellent. For most adapter applications where point−of−load regulation (POL) is utilized anyway, the slow transient response is inconsequential. Figure 7 shows the output voltage profile at supply turn−on with no load and with full load indicating a controlled voltage rise with no overshoot that is sometimes typical with slow control loops.
2. Because the loop cannot regulate away the 120 Hz line ripple, it will appear as a ripple component on the output. For this circuit, the peak−to−peak output ripple was in the order of 1 V (5 %) for full load with three 4700 μF output capacitors (see Figure 4). Additional output capacity will reduce this further. Again, for most analog or POL applications, this ripple magnitude should not be a problem.
3. Due to the lack of a large input bulk capacitor (C3), which would preclude high power factor, the converter has no significant inherent hold−up time other than that provided by the stored energy in T1 and the output capacitors.
4. The power factor for the single stage converter tends to degrade with increasing line and decreasing load due to factors related to the D/(1−D) transfer function and CCM operation, however, for most typical line and load conditions the PF will be above 0.95.

Despite these tradeoffs, the single stage, isolated PFC converter is an efficient and very cost effective solution to most notebook adapter and similar applications. For LED ballast applications, an additional current feedback loop with output current sense resistors can be implemented to provide a constant voltage, constant current (CVCC) characteristic. The ON Semiconductor NCP4300A dual opamp plus zener reference is well suited for such applications.

Circuit Technical Information

NCP1652 components selection: The logic level circuit components immediately associated with the NCP1652 shown in the Figure 3 schematic should work well with just about any design implementation. Changes for different output voltages will be required for the voltage sense divider for the TL431 (R29, R30) and the value of R20 will determine the peak limit of the MOSFET current and the subsequential maximum output current. R12 sets the ramp compensation for CCM operation and can be adjusted depending on the primary inductance and level of the CCM transformer magnetizing ramp. The switching frequency is set to approximately 70 kHz with C9. The component values shown should be adequate for most applications. R5, R16, R17, D9, Z2 and C14 form a simple and optional OVP circuit that monitors the V_{CC} derived from T1's auxiliary winding. Since this voltage will track the output voltage, it provides a simple primary side means of OVP sensing. R2, D5 and C4 form a dc startup circuit for the 1652 which uses a peak detector to sample the input haversine. This circuit, along with TVS Z1, also doubles as a transient suppression circuit in the event of short duration, high amplitude line transients that input capacitor C3 would be unable to suppress.

At light and zero loads the controller enters skip mode operation where the converter operates in short bursts. This type of operation keeps the no load "standby" power below the Energy Star requirement of 500 mW. The circuit composed of Q2, R25, C28 and C29 extends the control loop bandwidth during this mode so as to stabilize the skip mode operation. This is necessary because the large output capacitance of the supply would cause the skip frequency at no load to be too low to adequately refresh the V_{CC} capacitor C6 and maintain it above U1's undervoltage lock out level. When the feedback voltage on pin 4 of U1 drops below about 0.65 V, Q2 turns off and disconnects bandwidth limiting capacitor C28 from pin 4. The bandwidth is then controlled by C17 which provides adequate loop bandwidth which results in a higher frequency of skip mode operation.

Input EMI filter design: The EMI filter consists of two stages of off the shelf common mode inductors (L1 and L2) which are manufactured by Coilcraft. The common mode inductors have a high leakage inductance so a signal inductor can be used for both common mode and differential mode filtering. The differential LC low pass filter is formed with the leakage inductance and the X capacitors from line−to−line. The first stage of filtering is with L1 and C1, and the second stage is with L2 and C2. L1 has a leakage inductance of 15 μH and L2 has a leakage inductance of 22 μH.

$$f = \frac{1}{2\pi\sqrt{L3C18}} = \frac{1}{2\pi\sqrt{15\ \mu H \cdot 0.47\ \mu F}} = 59.97\ kHz$$

$$f = \frac{1}{2\pi\sqrt{L2C17}} = \frac{1}{2\pi\sqrt{22\ \mu H \cdot 0.47\ \mu F}} = 49.52\ kHz$$

When testing in accordance with the IEC 61000−4−6 limits (0.15 MHz to 80 MHz) there should be at least −24 dB of attenuation of the 70 kHz switching frequency with these EMI filter component values.

On the ac input side of the filter is a fuse, F1 for safety. The fuse is rated for 2.5 A of continuous current, where the average input current for 90 W output is:

$$I_{avg} = \frac{P_{out}\sqrt{2}}{\eta V_{inLL}} = \frac{90\ W\sqrt{2}}{0.88 \cdot 90\ Vac} = 1.61\ A$$

Where η is the estimated efficiency (0.88)

The input line voltage is full wave rectified and there is a small bulk film capacitor (C3) across the output of the bridge rectifiers (D1, D2, D3, and D4). The capacitor is there to decouple the high frequency switching and provide a low impedance source for the flyback converter. A typical range for the capacitor is 0.27 μF to 1.0 μF. For this application a 1.0 μF capacitor was selected.

T1 Flyback Transformer Design: The transformer design for a single stage PFC converter is a tricky and iterative process, especially when operation is in continuous conduction mode. There are several ways to mathematically approach this, however, treating the transformer as an energy storage choke initially is probably the most straight forward way. Hitting the correct design on the first try is largely a matter of experience with realizing what core volumes and structures will support the desired power level and accommodate the necessary coil turns. A PQ3230 ferrite core was chosen for this design based on previous experience and the following facts:

1. The PQ core has a fairly large cross sectional area parameter (Ae) for its overall volume. This will minimize primary turns which contribute to unwanted leakage inductance. The shape of the core also has a good shielding effect on radiated emissions, particularly if the required core gap is entirely in the center pole.
2. The core window area has a good length to width aspect ratio which helps minimize turn layers and thus reduce leakage inductance and magnetic flux proximity effects.
3. For minimal leakage inductance, this core will accommodate a “sandwiched” secondary winding configuration where the secondary is in between two primary windings which are connected in series.

Since the peak primary current in the inductor will determine the output power, the peak magnitude of the current can be obtained from the following relationship:

$$I_{pk} = 2\,P_{out}/n \times f \times V_{in(min)} \times t_{on(max)}$$

Where n is the estimated efficiency, f is the switching frequency, $V_{in(min)}$ is the minimum average input voltage at lowest line voltage, and ton max is the maximum on time. This results in a value of:

$$I_{pk} = (2 \times 95\ W)/0.88 \times 70000 \times 83\ V \times 10\ \mu s) = 3.7\ A(pk)$$

Note that the average line voltage was used and not the rms value (90 Vac) for low line. This results from the fact that the input is a 120 Hz haversine and the energy storage will be a function of the average voltage and not rms.

Now, for wire sizing purposes we need to know the rms value of this peak current. If we assume an average duty cycle of D = 0.5 at 120 Vac input and assume an almost rectangular CCM waveform (the magnetizing component will actually be about 30% of the peak, but this should give a worst case estimate), the rms value of the switching frequency component for a pure dc input would be:

$$I_{rms} = I_{pk} \times \sqrt{D} = 3.7 \times 0.707 = 2.6\ A$$

Now we must divide this by 0.707 again to account for the fact that the input to the converter is a 120 Hz haversine envelope and not pure dc. This results in an rms primary current of about 1.8 A. Looking at wire tables we can effectively choose #24 magnet wire for the primary since it will handle this current and should have minimal skin effect loss at 70 kHz.

The minimum primary inductance required is given by the following:

$$L_{min} = Vdcpk(min) \times t_{on(max)}/Ipk = (120\ Vdc \times 10\ \mu s)/3.7\ A = 324\ \mu H$$

Where Vdc pk min is the low line value of the peak input voltage (85 Vac x 1.414). Now we make an assumption: In order to be in CCM for most of the typical loading of the supply, let’s double this inductance value to 650 μH. The number of primary turns required for this core can now be calculated:

$$NP = \frac{L \times Ipk \times 10^8}{Ae \times B_{max}} = \frac{650\ \mu H \times 4\ A \times 10^8}{1.6\ cm^2 \times 2800\ g} = 58\ turns$$

Where the peak current was rounded off to 4 A and the maximum flux density (B_{max}) was chosen to be 2.8 kilogauss to give a saturation safety margin for overcurrent conditions.

Noting that the PQ3230 bobbin winding width for the PQ3230 core is about 0.73 inches, we can comfortably get about 30 turns of number 24 wire (dia. = 0.022”) on one layer of the bobbin and a total of 60 turns for the entire series primary, so 60 turns total is a good number to go with.

Next will be to decide the primary to secondary turns ratio. This will determine the reflected flyback voltage on the MOSFET Q1 and also the peak reverse voltage seen by the Schottky output rectifier D8. Let’s try 6:1 where the secondary will have 10 turns. With this selection we can comfortably get 3 strands of # 24 trifilar wound over 1 layer to handle the secondary current which will be about 10 A rms worst case. The reflected primary flyback voltage and maximum PRV output diode voltage will occur at high line. Let’s assume an input voltage of 270 Vac which translates to peak voltage of 378 Vdc. The reflected flyback voltage will be the peak secondary voltage of 19 V_{out} plus the Schottky forward drop times the turns ratio:

$$V_{flyback} = (19\ V + 1\ V) = 120\ V$$

Adding this to the peak primary voltage of 378 V gives 378 + 120 = 498 V plus any leakage inductance spike which will probably be in the order of 100 V. The selected 800 V MOSFET should be adequate for this. The primary of T1 is bypassed with the voltage clamping snubber network of D7, C7 and R3 to clamp residual spikes caused by T1’s leakage inductance.

The output Schottky PRV voltage will be the peak input voltage divided by the turns ratio plus the output voltage and output diode drop:

$$\text{Diode PRV} = (378/6) + 20\ \text{V} = 83\ \text{Vpk}$$

So, the 100 V rated Schottky should handle this. Notice that a small R/C snubber composed of R24 and C19 is across D9 to attenuate any parasitic voltage spikes. The final transformer design is detailed in Figure 8.

Test Results

Efficiency and power factor measurements: Power factor, THD, and efficiency measurements were taken at loads of 25%, 50%, 75% and 100% at both US and Euro mains voltages. The efficiencies were averaged per Energy Star criteria. The results are shown in the table below.

	Load	100%	75%	50%	25%	
Vin = 120 Vac	THD =	6.6	4.5	7.2	11.4	
	PF =	0.995	0.993	0.986	0.948	
	Eff =	88.0	88.9	89.8	89.1	Eff avg = 89%
Vin = 230 Vac	THD =	7.1	10.3	13.8	14.6	
	PF =	0.975	0.951	0.901	0.713	
	Eff =	89.9	89.4	90.4	87.1	Eff avg = 89.2%

Note that for either AC line value, the efficiency easily exceeded the 87% minimum Energy Star requirement for adapters. At no load the input power consumption was 310 mW at 120 Vac and 430 mW at 230 Vac. The light load efficiency was as follows:

Output Load	0.5 W	1.0 W	1.7 W
120 Vac in	57%	69%	73%
230 Vac in	47%	59%	69%

Output Ripple

The 120 Hz output ripple with a 5 amp load on the power supply is shown in Figure 4 for 115 Vac input. The ripple amplitude is strictly a function of the output capacity and load on the power supply since the regulation loop bandwidth is necessarily less than the ripple frequency to assure high power factor (see also Figure 7).

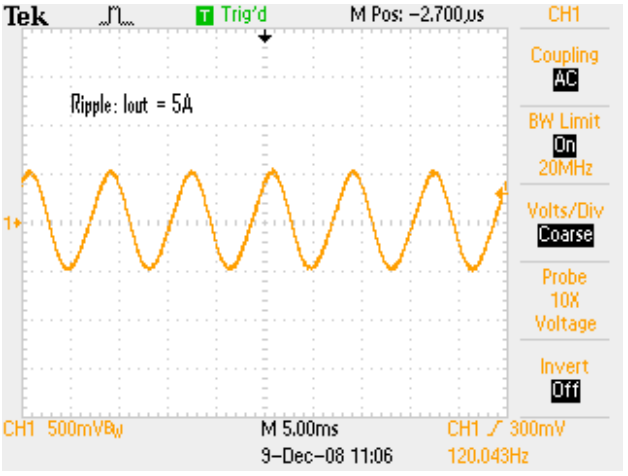
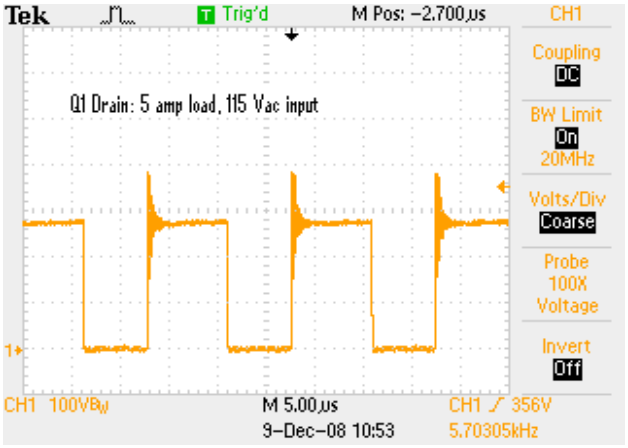


Figure 4. Output Ripple

Flyback Waveforms

The waveforms of Figure 5 shows the drain voltage profile on MOSFET Q1 with full output load (5 A) for 115 Vac and 230 Vac input. The leading edge voltage spike is caused by the leakage inductance of transformer T1 and is largely suppressed by the snubber network of D7, C7 and R3.



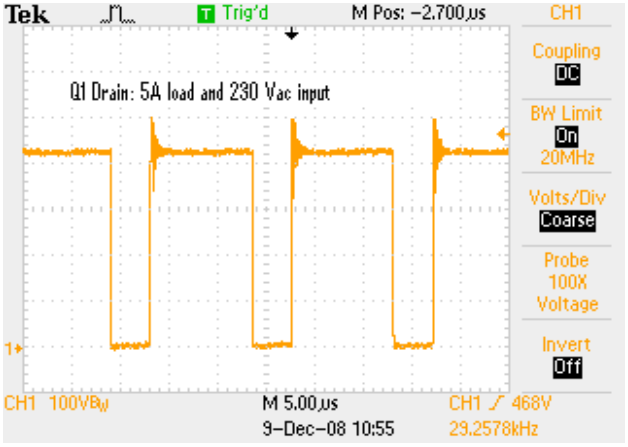
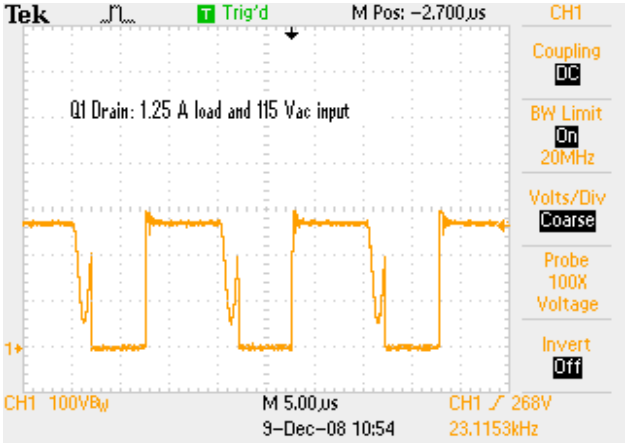


Figure 5. Q1 Drain Waveforms at Full Load

The waveforms of Figure 6 display Q1's drain waveform at 25% output load (1.25 A). Note that operation is clearly in DCM at this load for both line input levels. Note that when the flyback energy is depleted, the drain voltage will ring prior to Q1's next turn−on due to the resonant circuit formed by the transformer's primary inductance and the MOSFET's parasitic capacitance. This is a characteristic of DCM operation.



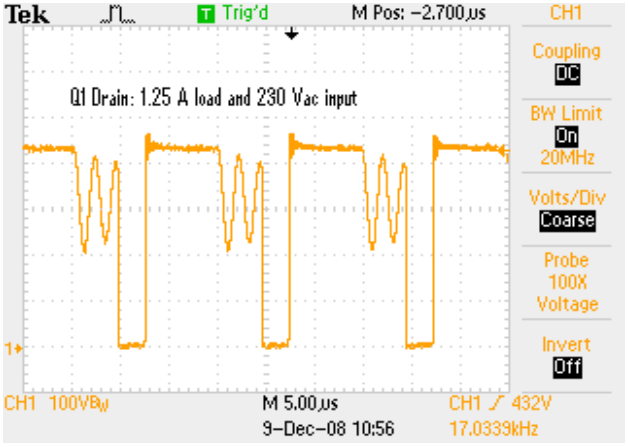


Figure 6. Q1 Drain Waveforms at 25% Load

The drain waveforms in the prototype were very “clean” of excessive leakage inductance voltage spikes and subsequent ringing which is imperative for high efficiency operation and low EMI generation. Use of proper PC board layout techniques with minimal power loop traces, liberal ground planes, and clad “pours” where possible to lower trace inductance will assure proper switching waveform profiles and lowest EMI. Very low flyback transformer leakage inductance is also extremely important as previously mentioned. In higher power applications and in cases were mechanical constraints limit optimum core structure and/or winding techniques, the use of an active clamp to suppress the primary voltage spikes may be necessary.

The output turn on profiles of Figure 7 clearly indicate that no output overshoot exists for either load condition, particularly at no−load where it is not uncommon to exhibit overshoot with narrow bandwidth control loops. At full load the 120 Hz throughput ripple is clearly visible.

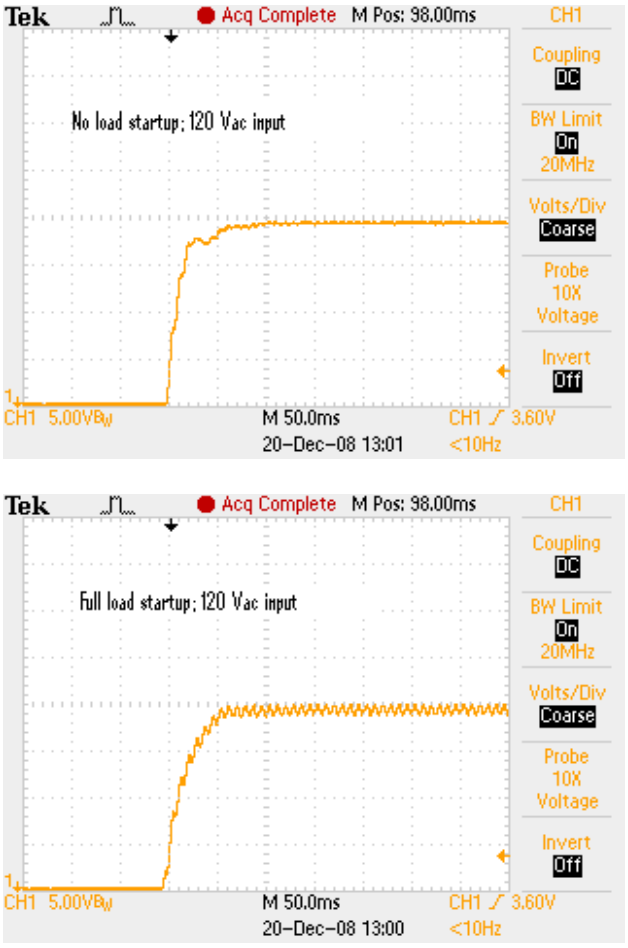


Figure 7. Turn−on Profiles

MAGNETICS DESIGN DATA SHEET

Project: NCP1652, 90W, 19V Adapter

Part Description: CCM Flyback transformer, 70 kHz, 19 Vout (Rev 2)

Schematic ID: T1

Core Type: PQ3230, 3C94 (Ferroxcube) or P material (Mag Inc.)

Core Gap: Gap core for 600 to 650 uH across pins 1 to 2.

Inductance: 625 uH nominal measured across primary (pins 1 to 2)

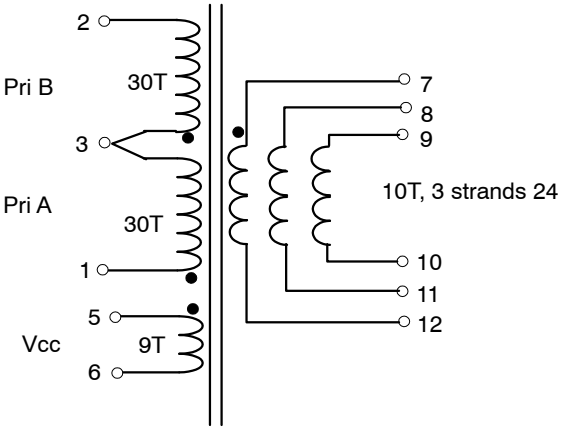
Bobbin Type: 12 pin pc mount (Mag Inc PC−B3230−12 or equivalent)

Windings (in order):

Winding # / type	Turns / Material / Gauge / Insulation Data
Primary A: (1 – 3)	30 turns of #24HN over one layer (no margins). Self−leads to pins. Insulate for 3 kV to next winding.
19V Secondary (7, 8, 9 – 10, 11, 12)	10 turns of 3 strands of #24HN flat wound (trifilar) over one layer with tape cuffed ends for safety (no margins) Terminate with 1 wire per pin as shown in drawing below. Insulate with tape for 3 kV to next winding.
Primary B: (3 – 2)	Same as primary A. Insulate for 1.5 kV to Vcc/Aux.
Vcc/Aux (5 – 6)	9 turns of #24HN spiral wound and centered with 8 mm end margins. Insulate with tape and terminate self−leads to pins.

Hipot: 3 kV from primary/Vcc to 19V secondary windings.

Schematic



Lead Breakout / Pinout

(bottom view)

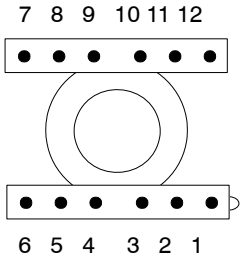


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Figure 8. Flyback Transformer Design

Some Final Comments

For single stage, isolated PFC converters where the output voltage is 12 V and less, the efficiency can be enhanced by with the use of synchronous output rectifiers instead of convention PN or Schottky diodes. Synchronous output rectifiers are not, however, wholly compatible with continuous conduction mode (CCM) operation. This is because CCM or DCM operation will almost always transition into the other depending on the load situation. At light load CCM will transition to DCM, and with DCM operation, the startup and overcurrent conditions usually reverts to CCM. As a result of these two different modes of operation, the required gate drive signal to the synchronous MOSFET must be based on different sensing criteria for each mode which causes additional circuit complexity. The "problem mode" is CCM because there has to be a delayed timing sequence to the sync MOSFET to prevent simultaneous conduction overlap with the main primary side MOSFET. Even though the necessary timing sequence can be achieved, one critical issue still remains. When the sync MOSFET is turned off just prior to the main primary MOSFET coming on, the intrinsic body diode of the sync MOSFET must carry the still flowing continuous flyback current. This parasitic body diode has very poor recovery characteristics and when the main MOSFET turns on, the body diode is force commutated off and significant reverse current will flow in the body diode during the recovery process. This current along with the associated circuit reactive parasitics generates large voltage spikes and ringing on the sync MOSFET and main MOSFET during this transition. This usually necessitates the addition of larger snubbers and/or TVS clamping circuits to avoid MOSFET failure. The added circuit cost and dissipative issues are generally not worth it. So, if synchronous rectification is desired, the control technique to use is critical conduction mode (CRM) where all of the critical switching transitions can take place simultaneously when current in both the primary side and synchronous MOSFETs are zero. In this case no timing sequencing is required and a simple secondary current detection scheme is all that is necessary for effective synchronous rectifier control. Unlike DCM or CCM implementations, CRM does not have any load dependent mode transition, and currents are always zero when switching transitions takes place.

References

– Datasheet NCP1652

– Application Note AND8124: 90 W, Universal Input, Single Stage, PFC Converter

– Application Note AND8147: An Innovative Approach to Achieving Single Stage PFC and Step–Down Conversion for Distributive Systems

– Application Note AND8209: 90 W, Single Stage, Notebook Adaptor

– Application Note AND8394: A 48 V, 2 A High Efficiency, Single Stage, Isolated Power Factor Corrected Power Supply for LED Drivers and Telecom Power

– Reference Design TND317: 90 W Notebook AC–DC Adapter GreenPoint® Reference Design

All the above documentation is available for download from ON Semiconductor's website (www.onsemi.com).

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