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应用指南 AN-3006 光电隔离相位控制电路解决方案

引言

光电耦合器根据交流线路、电源变换以及多相电源系统的控制来简化逻辑隔离。通过确保敏感逻辑中无交流线路噪声和瞬变,光电耦合器能有助于解决问题。飞兆半导体的 6 引脚 DIP 光电耦合器系列具有高浪涌电压能力(7500V 峰值交流电压,60Hz,1 秒持续时间),设计人员凭借其能实现目标。本文介绍一个功率三端双向可控硅 (TRIAC) 相位控制电路,并将其与传统过零电路作比较。示例电路将低电平控制电路与交流线路相隔离。该电路可用来控制通用电机速度或灯具的亮度。通用电机具有高启动扭矩和宽速度范围特性 — 常用于混料器、搅拌器、地板磨光器、电动手工和木工工具等。

过零和随机相位 TRIAC 驱动器

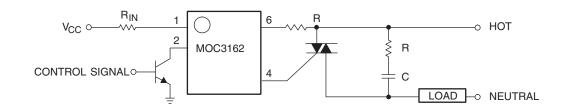
过零 TRIAC 驱动器光电耦合器为: MOC316X 和 MOC308X 系列。随机相位光电耦合器为: MOC301X、MOC302X 和 MOC305X 系列。所有系列都具有同类铝砷化镓红外发光二极管,但光耦合至不同的单片硅检波器芯片。过零系列设计用于控制电路和功率负载应用之间的接口。使用过零开关的优势是浪涌电流更低,从而电磁干扰 (EMI) 更少。这样就能减少很多应用中的可靠性问题,如固态继电器、工业控制、电机、电磁阀和消费类家用电器。高速过零开关提供 500 V/μs 至 2000 V/μs 的最小 dv/dt,保护器件不受交流电源线路瞬变的误触发影响。

图 1 所示电路是可实现通 - 断电源控制的基本电路。随着连续正向电流流过 LED,过零光电耦合器的检波器仅在施加的交流电压通过零点附近时,才切换到导通状态。相位控制应用(如控制电机速度或灯具亮度)要求沿交流电压波进行触发。这便需要使用随机相位 TRIAC 驱动器光电耦合器。

使用 MOC3023 以相位控制功率 TRIAC

设计目标

图 2 中的应用电路是采用相位控制功率 TRIAC 的一个示例。随机相位 TRIAC 驱动器为飞兆半导体的 MOC3023。该器件的 LED 触发电流 I_{FT} 为 5 mA,且关态输出端接电压 V_{DRM} 为 400 V。本例中使用的功率 TRIAC 具有 15 A 通态 (RMS) 电流 (T_{C} = 80C). 负载为 1/3 HP 单相感性电机,以 1750 rpm 的最高速度驱动风扇。该电路能够以更高的额定值应用于不同的功率 TRIAC 和负载中。设计目标为采用相位控制功率 TRIAC 驱动 115 VAC 线路供源的电机或调光器。采用 5 至 15 VD 控制电压,并利用光隔离逻辑系统产生的一系列脉冲宽度即可达成设计目标。



DESIGN RULE: V_{peak}/I_{peak} = 180 /1 amp = 180 ohms (Assume the line voltage is 115 volts RMS)

图 1. 使用 MOC3061 进行过零切换

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系统原理框图

全波过零传感器连接光隔离可变脉冲宽度振荡器。振荡器控制光隔离功率 TRIAC 导通时间,从而为负载提供相位控制。

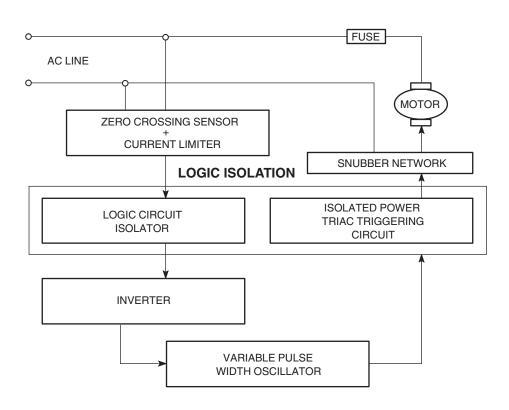


图 2. 系统原理框图

电路说明

全波交流至逻辑耦合

电路始于交流线路输入电压。它通过 1N4001 二极管桥式整流,并连接至 H11L1 逻辑输出光电耦合器的砷化镓 LED。正向电流(范围为 10 至 50 mA)流过光电耦合器 LED,产生红外辐射,触发高速施密特触发器输出级,使其导通。在由齐纳二极管定义的恒定输入电压下,该操作每半个交流周期发生一次,发生位置在线路过零附近。

限流器

R1 是一个限流电阻,用于齐纳二极管和光电耦合器输入 LED 的限流。 R2 提供较小的偏置电流,确保齐纳二极管工作在其特性曲线转折点上方的线性部分。通过为漏电流提供路径,它方便了 LED 的通 - 断切换。

可变脉冲宽度振荡器的光隔离触发

脉冲宽度为 720μs 的直流信号在 H11L1 的输出检波器处产生。 MPSA40 NPN 晶体管的目的是产生反向信号,该信号进入 LM555 单片时序电路的触发引脚 2。有关输入触发脉冲宽度与线路电压的关系,请参见图 4。

可变脉冲宽度振荡器

在每一个输入触发信号的下降沿,LM555 单片时序电路均产生正向脉冲,其占空比由C1、VR1 和 R5 控制。脉冲持续时间在时间常数 t=1.1* (VR1+R5)*C1 内测量。电容 C1 两端的电压与 LM555 输入触发信号的关系参见图 5。

隔离 TRIAC 触发

来自振荡器的输出信号 (V_{td}) 输入 MOC3023 TRIAC 驱动器 LED。当有足够的 LED 电流 (I_{FT}) 流经 LED 时,TRIAC 驱动器锁存在高电平,在功率 TRIAC 中产生栅极电流,将其触发为导通状态。

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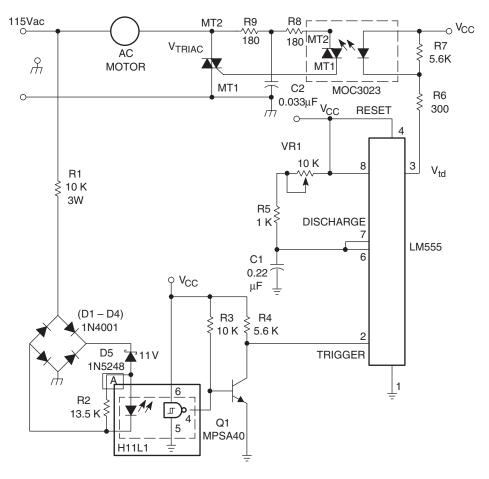


图 3. 原理示意图 使用 MOC3023 以相位控制功率 TRIAC

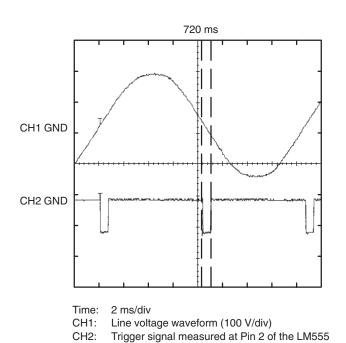


图 4. 过零交流至逻辑耦合

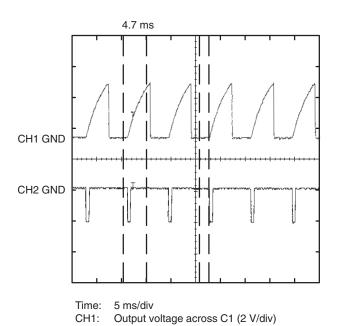


图 5. 电容 C1 在输入触发脉冲的下降沿开始充电,时间常数 为 1.1*R5*C1

CH2:

Input trigger pulse to LM555 (5 V/div)

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一旦功率 TRIAC 锁存,即使此时已施加了 I_{FT} , TRIAC 驱动器也将被迫进入断态。功率 TRIAC MT2 到栅极的电压下降至低于光电耦合器阈值电压的较低值,并且无法保持光电耦合器导通状态。参见图 8 中功率 TRIAC 两端电压 (V_{TRIAC}) 与功率 TRIAC 栅极触发信号 (V_{td}) 的关系。

相位控制的最小负载功率

施加在负载上的平均功率通过 TRIAC 驱动器的输入波形持续时间加以调制。相位延迟时间越长,导通角度和分配到负载上的功率就越小。 R5、 VR1 和 C1 确定最小负载功率。这样便确保了功率 TRIAC 的锁存与光电耦合器的关断。它可防止光电耦合器的换向 dv/dt 故障。图 3 所示电路的最小导通角度为 12 度。功率 TRIAC 两端的电压与 TRIAC 驱动器输入信号的关系参见图 9。

缓冲器网络

若施加的电压上升速率超过功率 TRIAC 的 dv/dt 或TRIAC 驱动器的 dv/dt,则功率 TRIAC 可能会被误导通。为防止这种误触发现象,使用单个缓冲器限制功率TRIAC 和光电耦合器的最大 dv/dt。缓冲器网络可通过假设感性负载的功率因数定义,随后通过测量实际 dv/dt 加以调整,并对缓冲器作必要的调节。图 3 中所用的缓冲器网络可获得最差情况下的 dv/dt,其中耦合器为:

dv/dt = Vto / (R9 * C2) = 180 / (180 * 0.033)

 $= 30.3 \text{ V/}\mu\text{s}$

V_{to} = 瞬时峰值线路电压

负载电感的存在 (比如负载是一个电机) 使 dv/dt 的值 大幅下降。有关设计缓冲器网络的详细信息,请参见飞 兆半导体应用指南 AN3008。

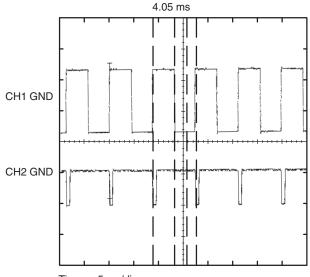
R8 限制流过 TRIAC 驱动器的峰值电容放电电流。其最小值可由下式计算得出:

R8 = V_{pk} / I_{max} = 180 / 1.2 A = 150 Ω (1/2 W) V_{pk} - 栅极触发所需的电压 I_{max} - 光电耦合器的浪涌电流额定值

作者选用 180 Ω限流电阻。

结论

本应用指南展示了 TRIAC 驱动器和功率 TRIAC 在交流逻辑隔离相位控制应用中的使用。使用相对较少的元器件即可轻松完成电路设计。

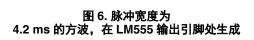


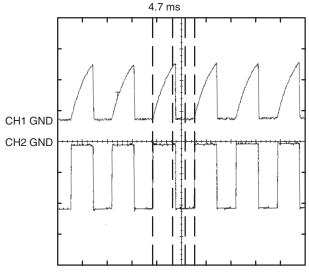
Time: 5 ms/div

CH1: Output signal measured at Pin 3 of the

MC1455 (2 V/div)

CH2: Input trigger pulse to MC1455 (5 V/div)





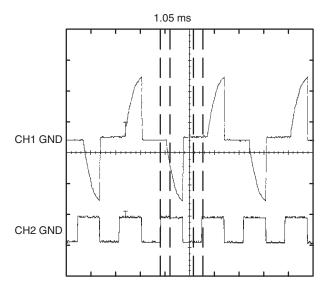
Time: 5 ms/div

CH1: C1 starts to discharge when voltage reaches 2/3 of the V_{CC} (2 V/div)
CH2: Power triac gate trigger signal (V_{td})

with pulse duration of 4.7 ms (2 V/div)

图 7. 电容电压与功率 TRIAC 栅极触发信号的关系

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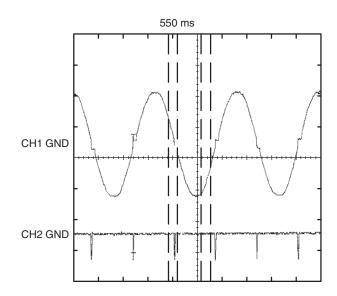


Time: 5 ms/div

CH1: Voltage across the power triac terminals (V_{TRIAC}) (100 V/div)
CH2: Power triac gate trigger signal,

V_{td} (5 V/div)

图 8. 功率 TRIAC



Time: 5 ms/div

CH1: Voltage across the power triac terminals (VTRIAC) (100 V/div)
CH2: Power triac gate trigger, Vtd (5 V/div)

图 9. 最小负载功率

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