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AN-4163 — Shielded Gate PowerTrench® MOSFET Datasheet Explanation

Introduction

A MOSFET datasheet contains important technical information for power system designers to choose proper MOSFETs for specific applications. This application note explains the electrical parameters and graphs specified in datasheets PowerTrench® MOSFETs. The shielded gate PowerTrench is Fairchild's advanced trench MOSFET design technology that supports MOSFETs rated up to 300 V. In this application note, the 100 V N-channel FDMS86101A datasheet is used for explanation.

1. Drain-to-Source Breakdown Voltage, BV_{DSS}

The breakdown voltage between the drain and the source terminal, BV_{DSS}, is measured at 250 µA drain current, I_D, with the gate shorted to the source, which turns off the MOSFET, as shown in Figure 1. Table 1 provides the minimum value of BV_{DSS} at 25° C junction temperature, T_J. The level of the BV_{DSS} is proportional to the increase of T_J positively. For example, the breakdown voltage temperature coefficient of FDMS86101A, $\frac{\Delta BV_{DSS}}{\Delta T_J}$ is 71 mV/°C typically. If T_J of FDMS86101A reaches 100° C, the BV_{DSS} increases by 5.325 V (75°C x 71 mV/°C). For more reliable operation, special caution should be taken to not exceed the BV_{DSS}; especially at an inductive load condition.

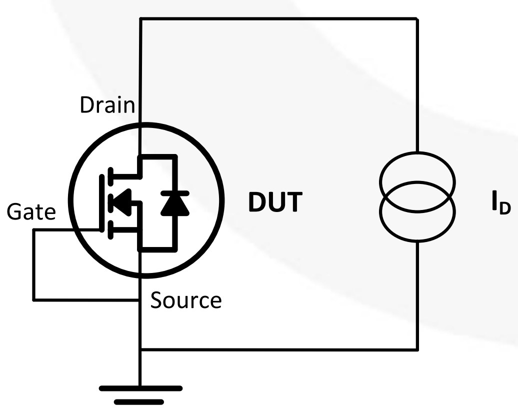

Figure 1. Drain-to-Source Breakdown Voltage Test Circuit

Table 1. Drain-to-Source Breakdown Voltage Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Unit
BV_{DSS}	Drain-to-Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V	100		V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		71	mV/°C

2. Gate-to-Source Voltage, V_{GS}

The sustainable voltage between the gate and the source terminal is limited to the maximum voltage, V_{GS}. It has the positive and negative 20 V, shown in Table 2, and any gate drive voltage must be less than the maximum V_{GS}. Designers should check the datasheet value for reliable operation since the V_{GS} varies by MOSFET technology.

Table 2. Gate to Source Voltage Parameters

Symbol	Parameter	Ratings	Unit
V_{GS}	Gate to Source Voltage	±20	V

3. Gate-to-Source Threshold Voltage, $V_{GS(th)}$

The gate-to-source threshold voltage, $V_{GS(th)}$, is defined as a minimum gate electrode bias to conduct the 250 µA drain current, I_D. It has the negative temperature coefficient, $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ so it is decreased as the junction temperature, T_J rises. For example, when T_J of FDMS86101A becomes 100°C, $V_{GS(th)}$ is reduced by 0.675 V (75°C x -9 mV/°C). Minimum, typical, and maximum values are specified in Table 3.

Table 3. Gate-to-Source Threshold Voltage Parameters

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D=250 µA	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate-to-Source Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		-9		mV/°C

4. Static Drain-to-Source On Resistance, $R_{DS(on)}$

The static drain-to-source on-resistance, $R_{DS(on)}$, is described at various gate voltages, V_{GS} which are greater than the gate-to-source threshold voltage, $V_{GS(th)}$, and different drain current levels in Table 4 because the $R_{DS(on)}$ value changes at a different amplitude of the V_{GS} and the drain current, I_D, at a junction temperature, T_J. There are two graphs pertaining to the static on-resistance.

Table 4. Static Drain-to-Source On Resistance Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Static Drain-to-Source On Resistance	V_{GS} = 10 V, I_D = 13 A		6.3	8.0	mΩ
		V_{GS} = 6 V, I_D = 9.5 A		8.0	13.5	
		V_{GS} = 10 V, I_D = 13 A, T_J=125°C		10.3	13.1	

The normalized drain-to-source on resistance is a function of I_D at a given V_{GS}, as shown in Figure 2. V_{GS} plays an important role in changing the on resistance value. When the V_{GS} is decreased from 10 V_{GS} to 5 V_{GS} at 60 A of I_D, the $R_{DS(on)}$ increases three times, which can be translated to 18.9 mΩ (3 times 6.3 mΩ) and the maximum I_D is saturated at around 60 A with 5 V_{GS} due to the increased $R_{DS(on)}$.

Figure 3 shows the normalized drain-to-source on resistance according to T_J. The $R_{DS(on)}$ has a positive temperature coefficient; so at the 125°C junction temperature, the static drain-to-source on resistance of FDMS86101A is increased by 1.63 times compared to the 25°C value. Therefore, in the case of parallel operation, the drain current can be well balanced among MOSFETs because increasing on resistance caused by increasing junction temperature prevents the drain current from flowing through only one or a few channels of MOSFETs and then parallel connected MOSFETs share the total drain current.

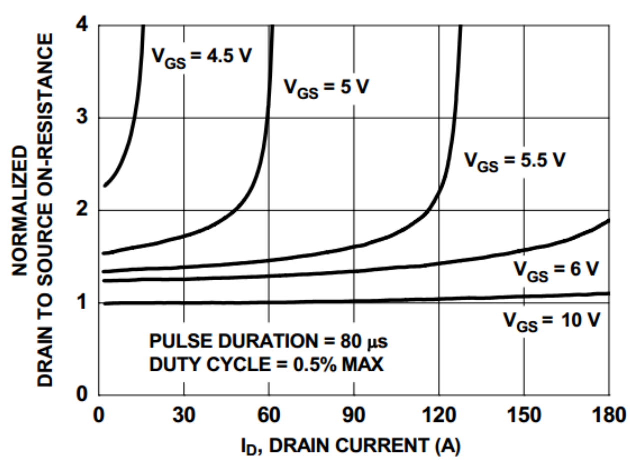

Figure 2. Normalized On Resistance vs. Drain Current and Gate Voltage

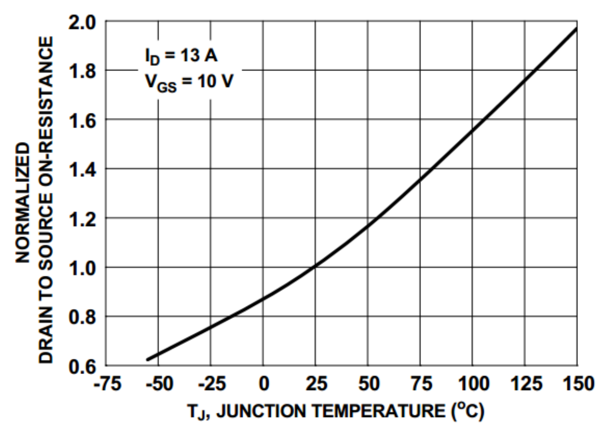

Figure 3. Normalized On Resistance vs. T_J

By using two graphs showing normalized drain-to-source on resistance values, the $R_{DS(on)}$ graph of Figure 4 as the function of the V_{GS} at both given T_J and I_D provides typical $R_{DS(on)}$ values. For example, if I_D is 13 A and V_{GS} is 5 V in 25°C junction temperature, the typical $R_{DS(on)}$ is 10 mΩ.

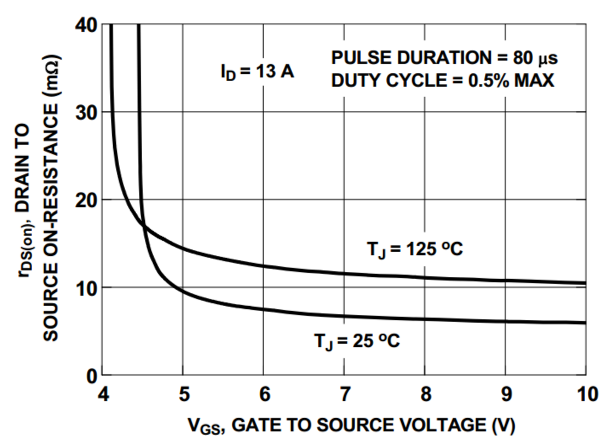

Figure 4. On Resistance vs. Gate-to-Source Voltage

5. Operating and Storage Junction Temperature Range, T_J

The operating and storage junction temperature, T_J indicates the recommended temperature range in which a MOSFET operates reliably under specified electrical values. Most of standard MOSFETs have -55°C to +150°C temperature range like Table 5.

Table 5. Operating and Storage Junction Temperature Parameters

Symbol	Parameter	Ratings	Unit
T_J	Operating and Storage Junction Temperature Range	-55 to +150	°C

6. Power Dissipation, P_D

The power dissipation, P_D, is the maximum allowable power limit of a device. The two P_D parameters are dependent on specific temperature conditions: case temperature, T_C, and ambient temperature, T_A. These parameters are calculated with Equations (1) and (2), respectively:

$$P_D(T_C) = \frac{T_J - T_C}{R_{\Theta JC}} \tag{1}$$

$$P_D(T_A) = \frac{T_J - T_A}{R_{\Theta JA}} \tag{2}$$

Thermal resistance is the ability to transfer heat from device to outside. Typically, two thermal resistances are provided in the datasheet, as shown in Table 6: junction-to-case thermal resistance, $R_{\Theta JC}$, and junction-to-ambient thermal resistance, $R_{\Theta JA}$. $R_{\Theta JA}$ is the sum of the junction-to-case resistance, $R_{\Theta JC}$, and the case-to-ambient thermal resistance, $R_{\Theta CA}$, where the case thermal reference is defined as the solder mounting surface of the device package. $R_{\Theta JC}$ is guaranteed by design, while $R_{\Theta JA}$ is determined by board conditions such as a PCB material, a mounted pad area, and layer number. Figure 5 shows the PCB information of the large 1-inch^2 and minimum pad sizes when the junction-to-ambient thermal resistance is measured.

Table 6. Thermal Resistance Parameters

Symbol	Parameter	Ratings	Unit
$R_{\Theta JC}$	Thermal Resistance, Junction-to-Case	1.2	°C/W
$R_{\Theta JA}$	Thermal Resistance, Junction-to-Ambient (Figure 5a)	50	°C/W
	Thermal Resistance, Junction-to-Ambient (Figure 5b)	125	°C/W

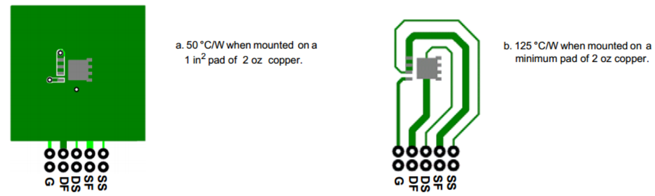

Figure 5. Mounted PCB Information for Thermal Resistance

With these thermal resistance values, the maximum P_D a MOSFET can sustain is calculated. For example, the maximum P_D of FDMS86101A mounted on the 1 inch^2 PCB pad can be calculated with $R_{\Theta JA}$ at 25°C ambient temperature from Table 6.

$$P_D(T_A) = \frac{T_J - T_A}{R_{\Theta JA}} = \frac{150℃ - 25℃}{50℃/W} = 2.5W$$

Table 7 describes the maximum allowable P_D based on each condition.

Table 7. Power Dissipation Parameters

Symbol	Parameter	Ratings	Unit
P_D	Power Dissipation, T_C=25°C	104	W
	Power Dissipation, T_A=25°C (Figure 5a)	2.5	W

7. Continuous Drain Current, I_D

Two continuous drain currents are specified in the datasheet based on the case temperature, T_C, and the ambient temperature, T_A. They can be calculated with Equations (3) and (4), respectively.

$$I_D(T_C) = \sqrt{\frac{T_J - T_C}{R_{DS(ON),TJ(MAX)} \cdot R_{\Theta JC}}} \tag{3}$$

$$I_D(T_A) = \sqrt{\frac{T_J - T_A}{R_{DS(ON),TJ(MAX)} \cdot R_{\Theta JA}}} \tag{4}$$

The I_D of FDMS86101A at T_C=25°C can be computed with $R\Theta_{JC}$ and $R_{DS(on)}$ at the maximum T_J of 150°C. As the $R_{DS(on)}$ is increased by the rise of T_J, the $R_{DS(on)}$ at the maximum T_J is calculated by multiplying the normalized factor at the 150°C junction temperature from Figure 3. Therefore, the $R_{DS(on)}$ becomes 15.6 mΩ (8 mΩ x 1.95).

$$I_D(T_C) = \sqrt{\frac{T_J - T_C}{r_{DS(ON),TJ(MAX)} \cdot R_{\Theta JC}}} = \sqrt{\frac{150℃ - 25℃}{8m\Omega \cdot 1.95 \cdot 1.2℃/W}} = 81.7A$$

It results in 81.7 A at the 25°C case temperature.

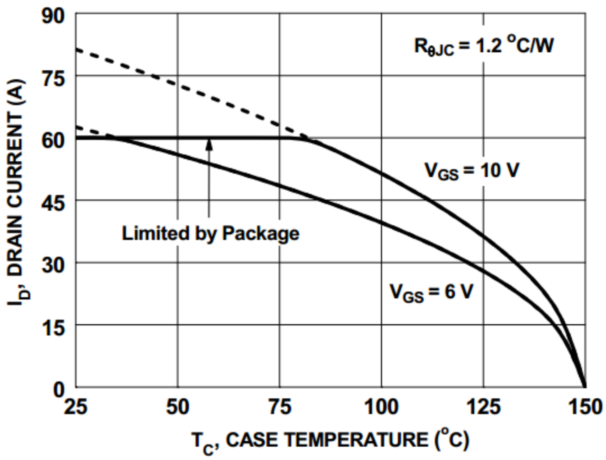

Figure 6. Maximum Continuous Drain Current vs. Case Temperature

Another constraint is caused by the current capability of a package. The I_D of FDMS86101A at the 25°C case temperature is limited by 60 A in Figure 6 due to its package current capability. Table 8 describes the maximum continuous drain current based on each condition.

Table 8. Continuous Drain Current Parameters

Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current, T_C=25°C	60	A
	Continuous Drain Current, T_A=25°C (Figure 5 - a)	13	A

8. Forward Transconductance, g_{FS}

The forward transconductance, g_{FS}, is the gain of the MOSFET expressed in Equation (5). It is the rate of change of the drain current, ΔI_D, per a change of the gate-to-source voltage variance, ΔV_{GS}, at a constant drain voltage, V_{DS}. A large transconductance is desirable to obtain a high current capability with low gate voltage:

$$g_{FS} = \left[\frac{\Delta I_{DS}}{\Delta V_{GS}}\right]_{VDS} \quad (5)$$

The typical g_{FS} value at the specific condition is listed in Table 9.

Table 9. Forward Transconductance Parameter

Symbol	Parameter	Conditions	Typ.	Unit
g_{FS}	Forward Transconductance	V_{GS} = 10 V, I_D = 13 A	53	S

9. Forward Bias Safe Operating Area, FBSOA

The forward bias safe operating area, FBSOA, is defined by lines of the maximum allowable drain current, I_D, under a specific drain-to-source voltage, V_{DS}, when a MOSFET is turned on by a single pulse or a continuous voltage at the T_A=25°C and minimum PCB pad. The set of the curves shows a DC line and five single pulse operating lines: 10 s, 1 s, 100 ms, 10 ms, and 1 ms in Figure 7.

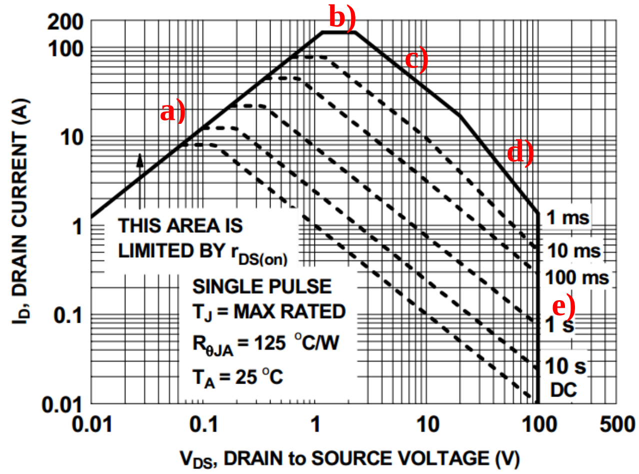

Figure 7. Forward Bias Safe Operating Area

There are five limitations from the a) to the e) line:

a. Limited by the static drain-to-source on resistance, $R_{DS(on)}$. For example, when the V_{DS} is 0.01 V, the I_D of FDMS86101A is limited to 1.25 A due to Ohm's law. (Typical the $R_{DS(on)}$ of FDMS86101A at 10 V_{GS} is 8 mΩ, from Table 4.)

$$I_D = \frac{V_{DS}}{r_{DS(on)}} = \frac{0.01V}{8m\Omega} = 1.25A$$

b. Limited by the maximum power dissipation, P_D is explained in Section 6.

c. Limited by the maximum drain current, I_D is explained in Section 7.

d. Limited by the thermal run away in the linear region, Figure 8 shows the I_D as the function of the V_{DS} at a given V_{GS}. The on-state operation of a MOSFET is divided into the ohmic region and the linear region, defined by $V_{DS} = V_{GS} - V_{GS(th)}$ as the boundary line. In the ohmic region, located to the left of the boundary line ($V_{DS} < V_{GS} - V_{GS(th)}$); the I_D is defined by Ohm's law and increases linearly with the incremental drain voltage. In the linear region, to the right of the boundary line ($V_{DS} > V_{GS} - V_{GS(th)}$); the I_D differs by the V_{GS}, not by V_{DS}. For example, when the V_{DS} is 4 V and V_{GS} is 4.5 V, the FDMS86101A operates in the linear region and its I_D stays at around 17 A. To increase I_D, a higher V_{GS} should be applied to the gate.

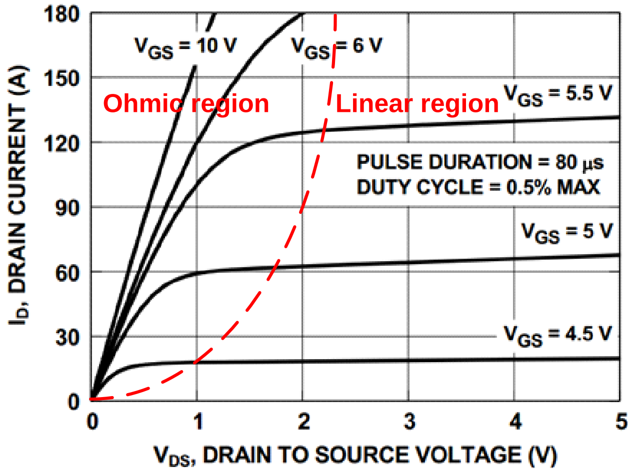

Figure 8. On-Region Characteristics

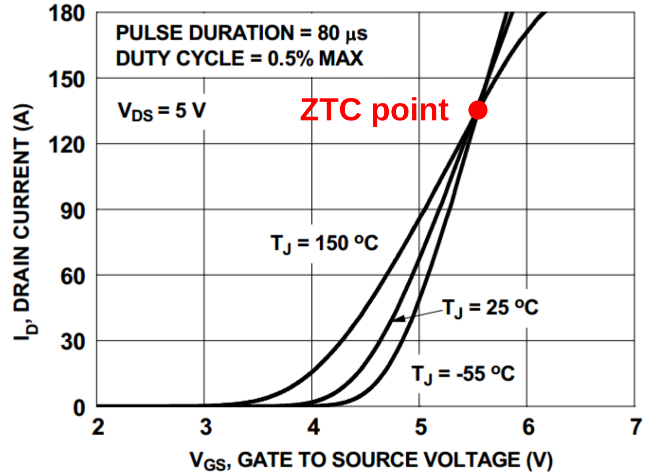

Figure 9. Transfer Characteristics

Figure 9 expresses the I_D as the function of the V_{GS} at given T_J and 5 V of V_{DS}. There is the crossover point among the transconductance curves at each junction temperature, which is called the Zero Temperature Coefficient, ZTC. If V_{GS} is above the ZTC point, a MOSFET has a negative temperature coefficient. It means if some cells within a MOSFET are getting hotter than others, hotter cells have a higher $R_{DS(on)}$ and their channels conduct less current, resulting in stabilizing the heat across unit cells. However, interestingly, a MOSFET has the positive temperature coefficient when operating with V_{GS} below the ZTC point. The gate threshold voltage, $V_{GS(th)}$, is reduced with the increase of junction temperature, T_J, and much more drain current flows. In the case of operation in the linear region with V_{GS} less than the ZTC point, a local hot spot within the MOSFET can occur and create non-uniform heat on the die due to the positive temperature coefficient. As a result, a thermal run away can occur in the worst case. So the d) line of FBSOA is defined based on real measurements.

e. Limited by the drain-to-source breakdown voltage explained in Section 1.

10. Transient Thermal Impedance, $Z_{\Theta JA}$

The steady-state thermal resistance values are not enough to find a peak junction temperature in terms of pulse driven applications. Figure 10 provides the normalized effective transient thermal resistance, r(t), as a function of the rectangular pulse duration at a given duty cycle. As the duty cycle and the pulse duration increase, the transient thermal impedance gets close to 1. This means the transient thermal resistance approaches steady-state resistance. It calculate the transient thermal impedance, $Z_{\Theta JA}(t)$, which is used to estimate the junction temperature, T_J, resulting from a transient power dissipation by using Equations (6) and (7):

$$Z_{\Theta JA}(t) = R_{\Theta JA} \times r(t) \quad (6)$$

$$T_J = P_D \times Z_{\Theta JA}(t) + T_A \quad (7)$$

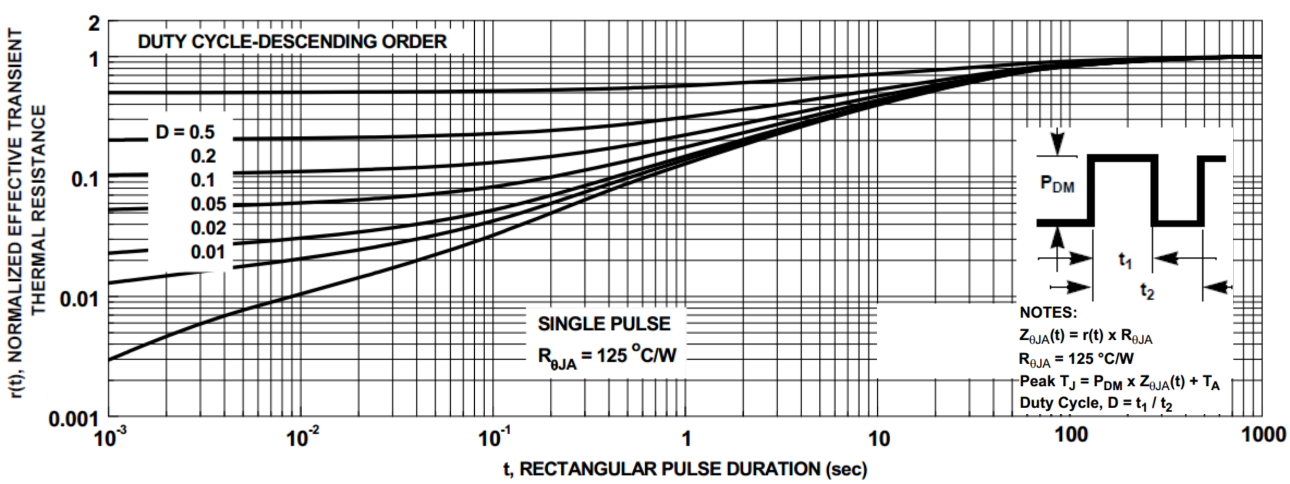

Figure 10. Junction-to-Ambient Transient Thermal Response Curve

For example, when FDMS86101A is conducting during 1 ms out of the 2 ms period which is the 0.5 duty cycle, the r(t) from Figure 10 is 0.5. The junction-to-ambient thermal resistance, $R_{\Theta JA}$ on the minimum pad of 2 oz copper is 125 °C/W from Table 6. Then the $Z_{\Theta JA}(t)$ of FDMS86101A mounted on the minimum pad of 2 oz copper is 62.5° C/W by using Equation (6).

$$Z_{\Theta JA}(t) = R_{\Theta JA} \times r(t) = 125°C/W \times 0.5 = 65°C/W$$

So the junction temperature of FDMS86101A at T_A=25°C can be computed using Equation (7).

$$T_J = P_D \times Z_{\Theta JA}(t) + T_A = 1W \times 62.5°C/W + 25°C = 87.5°C$$

Figure 11 provides the single-pulse maximum power dissipation as a function of the single pulse width at T_A=25°C and on the minimum pad of 2 oz copper PCB. The single-pulse maximum power dissipation can be calculated by using $Z_{\Theta JA}(t)$. For instance, $Z_{\Theta JA}(t)$ during the 10 ms single pulse is 1.25°C/W (125°C/W x 0.01) at T_A=25°C if the FDMS86101A is mounted on the minimum pad of 2 oz copper PCB. The single-pulse maximum power dissipation during 10 ms at T_A=25°C is 100 W.

$$P_D = \frac{T_J - T_A}{Z_{\Theta JA}(t)} = \frac{150°C - 25°C}{1.25°C/W} = 100W$$

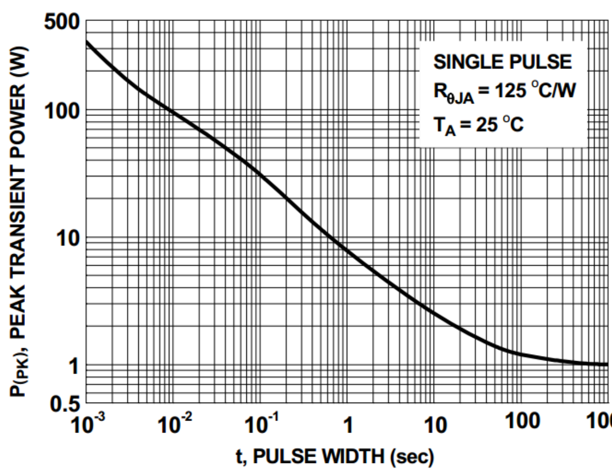

Figure 11. Single-Pulse Maximum Power Dissipation

11. Single-Pulse Avalanche Energy, E_{AS}

When the drain-to-source voltage, V_{DS}, exceeds the specified drain-to-source breakdown voltage, BV_{DSS}, at the turn-off state; the MOSFET breaks down and conducts the avalanche current, I_{AS}, and goes into avalanche mode. The I_{AS} through the body of the MOSFET causes the high power dissipation that can be translated to the avalanche energy, E_{AS}, and it can destroy the device. Figure 12 is the unclamped inductive switching (UIS) test circuit to show how much I_{AS} a MOSFET withstands during avalanche time, t_{AV}. The Device Under Test (DUT) is connected with an inductor in series, which induces the voltage of the counter-electromotive force. When the MOSFET is turned on for t_p time, the drain current reaches the point of I_{AS} and the energy is charged in the inductor. Right after the t_p, the MOSFET is quickly turned off and the inductor generates the voltage of the counter-electromotive force to increase the voltage of the drain terminal referenced to the ground (V_{DS}), which is clamped to BV_{DSS}.

The charged inductor energy starts being discharged through the device for the avalanche time, t_{AV}. Figure 13 shows the waveform of I_{AS} and V_{DS} in avalanche mode testing.

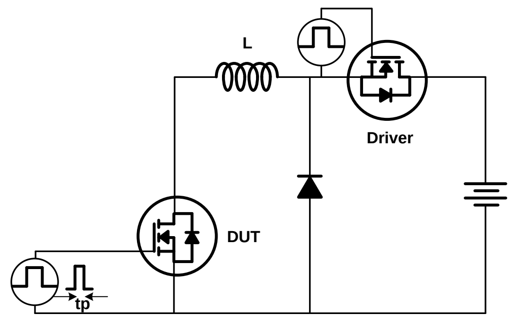

Figure 12. Unclamped Inductive Switching Test Circuit

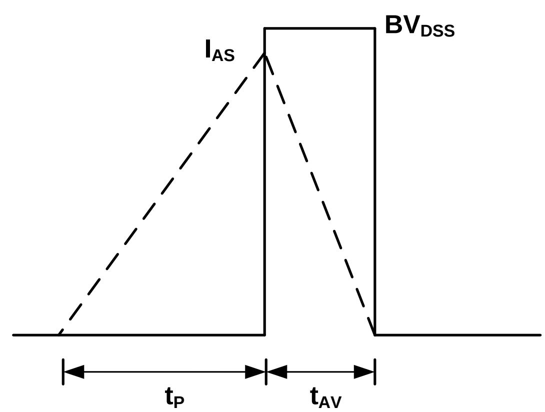

Figure 13. Unclamped Inductive Switching Waveforms

Figure 14 shows the relationship between t_{AV} and I_{AS} a MOSFET withstands at a given the junction temperature, T_J. There are a), b), c), and d) areas to determine whether or not the device is safe in the Unclamped Inductive Switching (UIS) mode.

a) Under the boundary of various T_J, the MOSFET is within the UIS capability.

b) Area between two boundaries of 125°C and 100°C of the T_J. If the starting point of the T_J is below 125°C before entering avalanche mode, the MOSFET is within the UIS capability.

c) Area between two boundaries of 100°C and 25°C of the T_J. If the starting point of the T_J is below 100°C before entering avalanche mode, the MOSFET is within the UIS capability.

d) The MOSFET is out of the UIS capability.

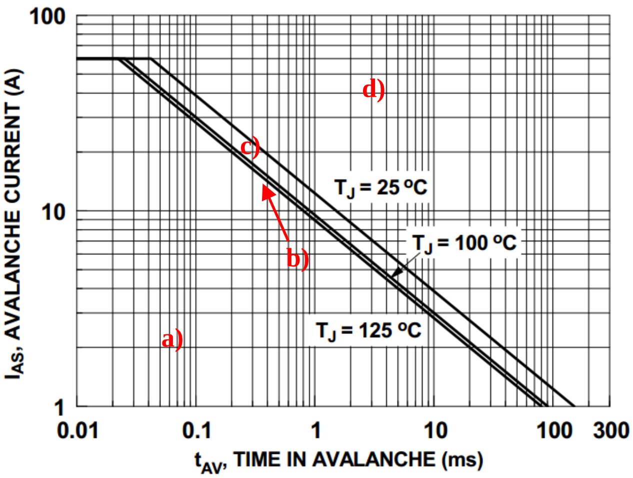

Figure 14. Unclamped Inductive Switching Capability

The single-pulse avalanche energy dissipated during the avalanche mode is calculated with the Equation (8). The FDMS86101 datasheet provides the maximum single-pulse avalanche energy at the specific condition, like the 3 mH inductor and the 25°C junction temperature in Table 10.

$$E_{AS} = \frac{1}{2} \times L \times I_{AS}^2 \quad (8)$$

Table 10. Single-Pulse Avalanche Energy Parameters

Symbol	Parameter	Ratings	Unit
E_{AS}	Single Pulse Avalanche Energy	486	mJ

Starting T_J = 25°C, L = 3 mH, I_{AS} = 18 A, V_{DD} = 100 V, and V_{GS} = 10 V.

For more information on the UIS, consult the following application notes on the Fairchild web site:

- *AN-9034: Power MOSFET Avalanche Guideline*
- *AN-7514: Single Pulse Unclamped Inductive Switching*

12. Capacitances

The switching performance of a MOSFET is normally determined by the time required to make the voltage change across capacitances. The datasheet provides three different capacitances, as shown in Table 11, which are measured at half of the drain-to-source voltage rating, V_{GS}, and 1 MHz frequency. The input capacitance, C_{iss}, is defined as the sum of the gate to drain capacitance, C_{GD}, and the gate-to-source capacitance, C_{GS}. The output capacitance, C_{oss} is the sum of the gate-to-drain capacitance, C_{GD}, and the drain-to-source capacitance, C_{DS}. The reverse transfer capacitance, C_{rss}, is the gate-to-drain capacitance, C_{GD}. Both typical and maximum values are specified in Table 11.

Table 11. Capacitances Parameters

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS}=0 V, f = 1 MHz	3095	4120	pF
C_{oss}	Output Capacitance		460	615	pF
C_{rss}	Reverse Transfer Capacitance		15	25	pF

Capacitances are dependent on an applied voltage and frequency. Figure 15 shows each capacitance as the function of the drain to source voltage at 1 MHz frequency.

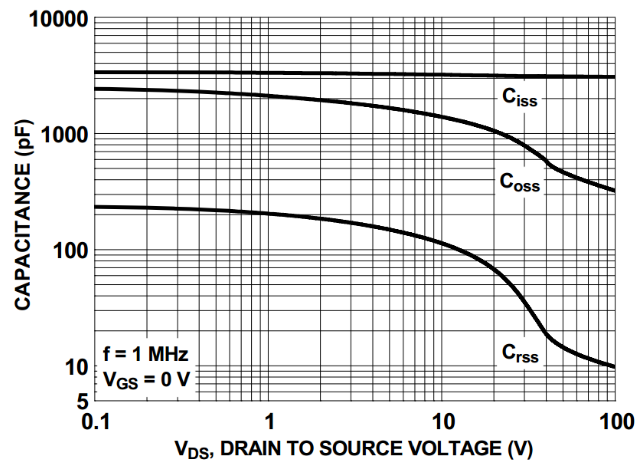

Figure 15. Capacitance vs. Drain-to-Source Voltage

13. Gate Charge, Q_g

Figure 16 shows waveforms when the DUT MOSFET in Figure 17 is turned on. When the MOSFET is turned on at T0, it starts to charge input capacitance, C_{iss}. From T0 to T1, there is no change in both the drain-to-source voltage, V_{DS}, and the drain current, I_D. Once the gate-to-source voltage, V_{GS}, reaches the gate-to-source threshold voltage, $V_{GS(th)}$, at T1, the MOSFET starts to conduct the I_D. From T1 to T2, the V_{GS} continues to increase to the plateau voltage, V_P, as the I_D rises to the specific load current controlled by the driver. The V_P varies by the load current. The V_{DS} is still clamped to the input voltage, V_{DD}. From T2 to T3, the V_{DS} begins falling and the drain-to-gate voltage, V_{DG}, takes on negative values, which increases gate-to-drain capacitance, C_{gd}, hugely. Due to the dramatic increase of C_{gd}, the V_{GS} is held at V_p. From T3 to T4, the MOSFET is fully enhancing the channel to obtain its rated $R_{DS(on)}$ at the applied V_{GS}. Figure 17 shows the gate charge test circuit.

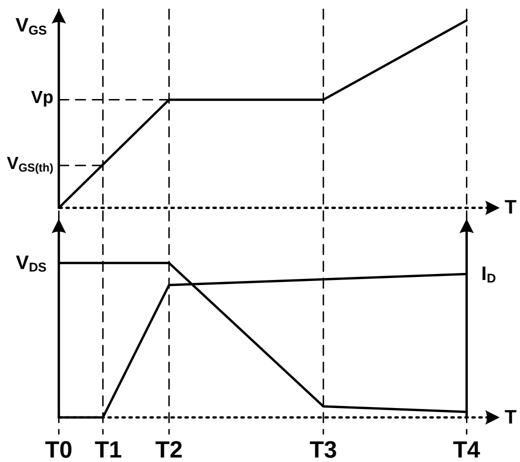

Figure 16. Gate Charge Waveforms

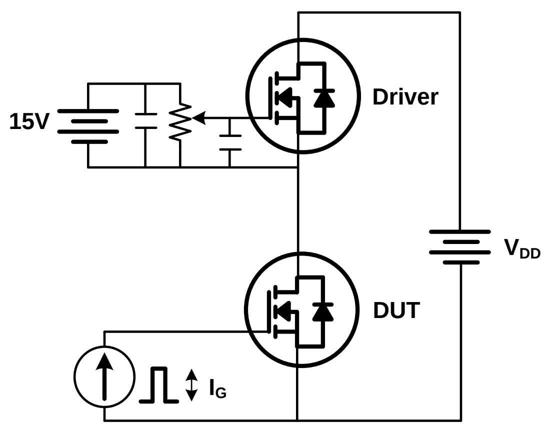

Figure 17. Gate Charge Test Circuit

By using the constant gate current, I_G, by the driver, the gate charge time is measured and the gate charge is calculated with Equation (9):

$$Q_g = T \times I_G \tag{9}$$

The gate-to-source charge, Q_{gs}, is the multiplication of I_G and the time from T_0 to T_2 and the gate-to-drain charge, Q_{gd}, is the multiplication of the I_G and the time from T_2 to T_3. The total gate charge, Q_g, is defined as the multiplication of the I_G and the time for the V_{GS} to reach a specific voltage, such as 5 V_{GS} or 10 V_{GS}. The typical and maximum values are specified in Table 12

Figure 18 shows that the gate charge characteristic depends on the V_{DS}. The higher V_{DS} is, the larger Q_{gd} is at a fixed I_D.

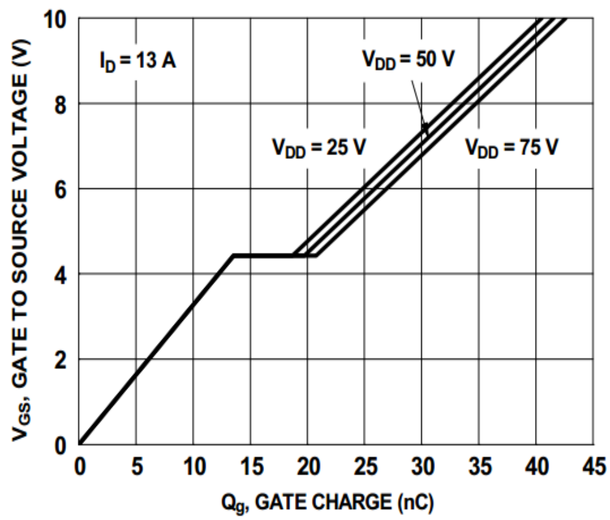

Figure 18. Gate Charge Characteristics

Table 12. Gate Charge Parameters

Symbol	Parameter	Conditions		Typ.	Max.	Unit
Q_g	Total Gate Charge	V_{GS}=0 V to 10 V	V_{DS} = 50 V, I_D=13 A	42	58	nC
Q_g	Total Gate Charge	V_{GS}=0 V to 5 V		22	31	nC
Q_{gs}	Gate-to-Source Charge	V_{DS} = 50 V, I_D=13 A		13.5		nC
Q_{gd}	Gate-to-Drain “Miller” Charge			6.2		nC

14. Switching Time

Like Table 13, switching time parameters are specified in the datasheet.

Table 13. Switching Time Parameters

Symbol	Parameter	Conditions	Typ.	Max.	Unit
$t_{d(on)}$	Turn-On Delay	V_{DS} = 50 V, I_D = 13 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	19.0	35.0	ns
t_r	Rise Time		5.4	11.0	ns
$t_{d(off)}$	Turn-Off Delay		27.0	44.0	ns
t_f	Fall Time		4.0	10.0	ns

The turn-on delay, $t_{d(on)}$, is defined as the time to charge the input capacitance, C_{iss}, before the I_D flows. The rise time, t_r, is the time to discharge output capacitance, C_{oss}, after the MOSFET conducts the I_D set by the resistor load, R_D. In the same way, the turn-off delay, $t_{d(off)}$, is the time to discharge C_{iss} after the MOSFET is turned off. The fall time, t_f, is the time to charge the output capacitance, C_{oss}, through the load resistor. Figure 19 and Figure 20 show the switching time test circuit and simple waveforms, respectively.

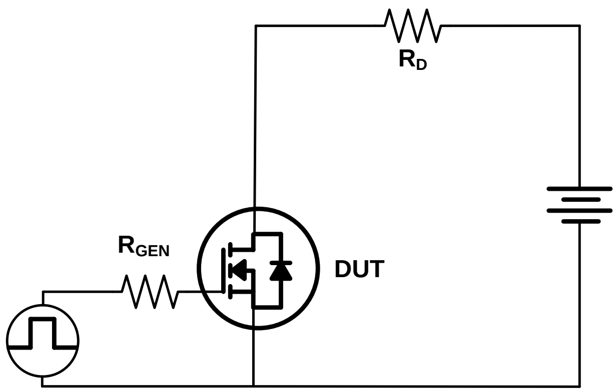

Figure 19. Switching Time Test Circuit

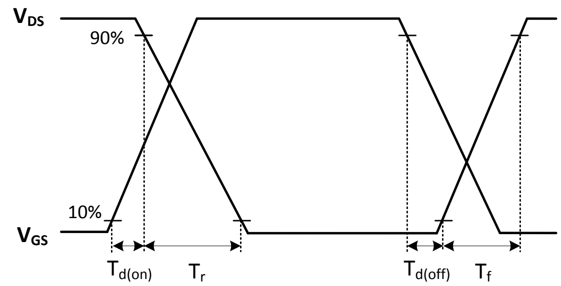

Figure 20. Switching Waveforms

15. Drain-to-Source Diode Characteristics

Like Table 14, the datasheet gives drain to source diode characteristics such as the source to drain diode forward voltage V_{SD}, the reverse recovery time t_{rr}, and the reverse recovery charge Q_{rr}.

Table 14. Drain-to-Source Diode Characteristics Parameter

Symbol	Parameter	Conditions	Typ.	Max.	Unit
V_{SD}	Source-to-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A	0.74	1.20	V
		V_{GS} = 0 V, I_S = 13 A	0.81	1.30	
t_{rr}	Reverse-Recovery Time	I_F = 13 A, di/dt = 100 A/µs	64	102	ns
Q_{rr}	Reverse-Recovery Charge		102	164	nC

The forward voltage of the intrinsic source-to-drain diode or the body diode is measured at the specific reverse drain current, I_S. Figure 21 shows the I_S as the function of body diode forward voltage, V_{SD}, at given junction temperatures, T_J. As the T_J increases, the V_{DS} is reduced at the fixed I_S due to its negative temperature coefficient.

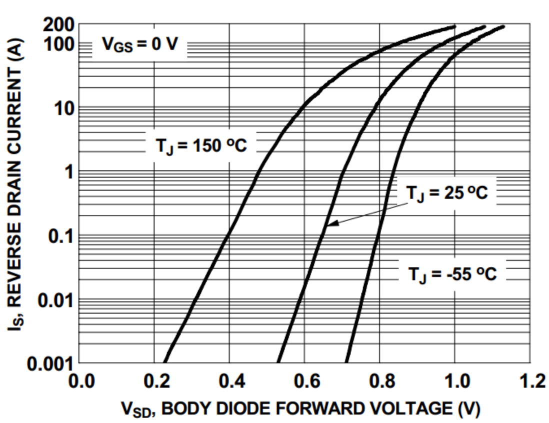

Figure 21. Source-to-Drain Diode Forward Voltage vs. Source Current

When the body diode is reversely biased right after its forward conduction, it cannot regain the reverse blocking capability until minority charge carriers stored in the body diode are recombined. It results in the reverse-recovery current flow, I_{rr}, through the body diode. The amount of time it takes body diode to recover is the reverse-recovery time, t_{rr}. The reverse-recovery charge, Q_{rr}, is the integral of I_{rr} over the t_{rr}. Figure 22 and Figure 23 show the reverse-recovery test circuit and waveforms. Two consecutive gate signals are applied to the driver MOSFET. With the first turn-on gate signal, the inductor, L, charges the energy through the driver MOSFET. Once the driver MOSFET is turned off, the inductor current starts flowing through the body diode of the DUT MOSFET. As the following second gate signal to the driver MOSFET is applied, the forward current of the body diode starts decreasing and is commutated to the driver MOSFET. The I_S decreases at a current slope, di/dt, and crosses zero to the I_{rr}. The decreasing slop, di/dt, of the recovery current is of importance because it determines t_{rr} and I_{rr}. Typical and maximum values of Q_{rr} and t_{rr} are listed in Table 14.

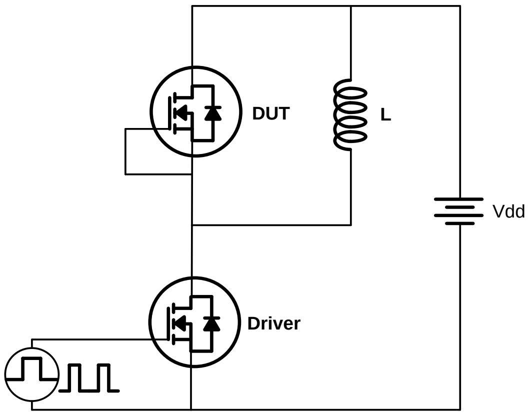

Figure 22. Reverse-Recovery Test Circuit

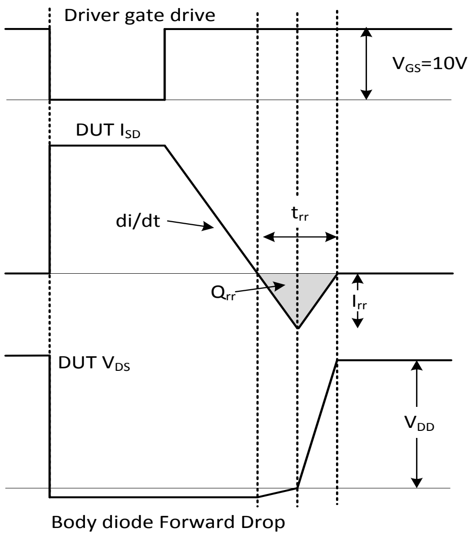

Figure 23. Reverse-Recovery Test Waveforms

16. Gate Resistance, R_G

The datasheet describes the gate resistance, which is the intrinsic resistance of the internal gate terminal. The minimum, typical, and maximum values are listed in Table 15.

Table 15. Resistance Parameter

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_g	Gate Resistance	0.1	1.6	3.3	Ω

17. Leakage Currents

The datasheet provides the maximum current for the leakage current from the drain-to-the source at the zero gate voltage and the 80% of the drain-to-source breakdown voltage, BV_{DSS}. The maximum gate-to-source leakage current is shown at the maximum V_{GS}. The maximum value is listed in Table 16.

Table 16. Leakage Current Parameters

Symbol	Parameter	Conditions	Max.	Unit
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	800	nA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	±100	nA

Authors

Ilsoo Yang and SungJin Kuen

Related Resources

- *FDMS86101A – 100 V N-Channel PowerTrench® MOSFET*
- *AN-9034 − Power MOSFET Avalanche Guideline*
- *AN-7514 − Single Pulse Unclamped Inductive Switching*

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