One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

ADV7280A/ADV7281A/ADV7282A Functionality and Features

SCOPE

This user guide provides a detailed description of the functionality and features of the ADV7280A, ADV7280A-M, ADV7281A-M, ADV7282A, and ADV7282A-M video decoders.

All features, functionality, and specifications are shared by the ADV7280A, ADV7280A-M, ADV7281A-M, ADV7282A, and ADV7282A-M, unless otherwise noted. They are referred to as the ADV7280A, ADV7281A, and ADV7282A devices in this user guide.

The ADV7280A, ADV7280A-M, ADV7281A-M, ADV7282A, and ADV7282A-M automatically detect and convert standard composite analog baseband video signals compatible with worldwide National Television System Committee (NTSC), phase alternating line (PAL), and sequential color with memory (SECAM) standards. These video recorders accept composite video signals (CVBS) as well as S-Video (Y/C) and YPbPr video signals, supporting a wide range of consumer and automotive video sources. The ADV7281A-M, ADV7282A, and ADV7282A-M models can also accept pseudo differential and true differential CVBS inputs.

The ADV7280A, ADV7281A-M, and ADV7282A models convert the analog video inputs into a YCrCb 4:2:2 component video data stream that is compatible with the 8-bit ITU-R BT.656 interface standard.

The ADV7280A-M, ADV7281A-M, and ADV7282A-M models convert the analog video inputs into an 8-bit YCrCb 4:2:2 video stream, and output over an MIPI CSI-2 (referred to as MIPI Tx) interface. This MIPI Tx output interface connects to a wide range of video processors and field programable gate arrays (FPGAs).

The automatic gain control (AGC) and clamp restore circuitry allow an input video signal peak-to-peak range of 1.0 V at the analog video input pin of the ADV7280A, ADV7281A, and ADV7282A devices. Alternatively, these can be bypassed for manual settings.

AC coupling of the input video signals provides short to battery (STB) protection. On the ADV7281A, ADV7282A, and ADV7281A devices, STB diagnostics can be carried out on two input video signals.

The ADV7280A, ADV7281A, and ADV7282A devices are programmed via a 2-wire, serial, bidirectional port (I^2C compatible). The ADV7280A, ADV7281A, and ADV7282A devices support a number of functions including 8-bit to 6-bit downdither mode and adaptive contrast enhancement (ACE).

The advanced interlaced to progressive (I^2P) function allows the ADV7280A, ADV7281A, ADV7282A, and ADV7282A-M devices to convert an interlaced video input into a progressive video output. This function is performed without the need for external memory. Edge adaptive technology minimizes video defects on low angle lines.

The ADV7280A, ADV7281A, and ADV7282A devices are fabricated in a 1.8 V complementary metal-oxide semiconductor (CMOS) process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation. The ADV7280A, ADV7281A, and ADV7282A devices are available in a variety of temperature ranges making them suitable for a range of industrial and automotive applications.

See Table 2 for a descriptive list of these video decoder models.

A full description of the ADV7280A, ADV7281A, and ADV7282A is available in the ADV7280A, ADV7281A, and ADV7282A data sheets and should be consulted in conjunction with this hardware reference manual.

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REVISION HISTORY

9/2017—Revision 0: Initial Version

GENERAL DESCRIPTION

OVERVIEW OF ANALOG FRONT END

The ADV7280A, ADV7281A, and ADV7282A devices AFE consist of a single high speed, 10-bit analog-to-digital converter (ADC) that digitizes the analog video signal before applying it to the standard definition processor (SDP).

The front end also includes a 4-channel input mux that enables multiple composite video signals applied to the ADV7280A, ADV7281A, and ADV7282A devices. Clamp restore circuitry is positioned in front of the ADC to ensure the video signal remains within the range of the converter. Place an external resistor and capacitor circuit before each analog input channel to ensure the input signal is kept within the range of the ADC (see the Input Networks section). Fine clamping of the video signal is performed downstream by digital fine clamping within the ADV7280A, ADV7281A, and ADV7282A devices.

Table 1 shows the three ADC clocking rates that are determined by the video input format to be processed—that is, INSEL[4:0]. These clock rates ensure 4× oversampling per channel for the CVBS, Y/C, and YPbPr modes.

Table 1. ADC Clock Rates

Input Format	ADC Clock Rate (MHz)[1]	Oversampling Rate per Channel
CVBS	57.27	4×
Y/C (S-Video)	114	4×
YPbPr	172	4×

[1] Based on a 28.63636 MHz crystal between the XTALP and XTALN pins.

OVERVIEW OF SDP

The ADV7280A, ADV7281A, and ADV7282A devices are capable of decoding a large selection of baseband video signals in composite, S-Video, and component formats. The ADV7281A-M, ADV7282A and ADV7282A-M are also capable of receiving pseudo differential and fully differential CVBS inputs. The video standards supported by the video processor include PAL B/ PAL D/ PAL I/PAL G/PAL H, PAL 60, PAL M, PAL N, PAL Nc, NTSC M/ NTSC J, NTSC 4.43, and SECAM B/SECAM D/SECAM G/ SECAM K/SECAM L. The ADV7280A, ADV7281A, and ADV7282A devices can automatically detect the video standard and process it accordingly.

The ADV7280A, ADV7281A, and ADV7282A devices have a five-line, adaptive, 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality without requiring user intervention.

Video user controls, such as brightness, contrast, saturation, and hue, are also available with these video decoders.

The ADV7280A, ADV7281A, and ADV7282A devices implement a patented Adaptive Digital Line Length Tracking (ADLLT™) algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the devices to track and decode poor quality video sources, such as VCRs and noisy sources, from tuner outputs and camcorders. The ADV7280A, ADV7281A, and ADV7282A devices contain a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

ACE offers improved visual detail using an algorithm to automatically vary contrast levels enhance picture detail. This algorithm increases the brightness of dark regions of an image without saturating bright areas of the image.

Downdithering converts the output of the ADV7280A, ADV7281A, and ADV7282A devices from 8-bit outputs to 6-bit outputs.

The I²P block on the ADV7280A, ADV7280A-M, ADV7282A, and ADV7282A-M converts the interlaced video input into a progressive video output. This conversion is done without a need for external memory.

The ADV7280A, ADV7281A, and ADV7282A devices can process a variety of vertical blanking interval (VBI) data services, such as closed captioning (CCAP), widescreen signaling (WSS), and copy generation management systems (CGMS). VBI data is transmitted as ancillary data packets.

The ADV7280A, ADV7281A, and ADV7282A devices are fully Rovi compliant (formerly Microvision and now rebranded as TiVo upon acquisition of the same); detection circuitry identify and report Type I, Type II, and Type III protection levels. The decoder is also fully robust to all Rovi signal inputs.

INPUT NETWORKS

An input network (external resistor and capacitor circuit) is required on the $A_{IN}x$ input pins of the ADV7280A, ADV7281A, and ADV7282A devices. The components of the input network depend on the video format selected for the analog input.

The available input networks include a single-ended input network and a differential input network. Refer to the ADV7280A, ADV7281A, and ADV7282A data sheets for more information.

STB DIAGNOSTICS

STB diagnostic pins are only available on the ADV7281A-M, ADV7282A, and ADV7282A-M models. See the ADV7281A and ADV7282A data sheets for more information.

VIDEO DECODER MODELS

Table 2 lists the Analog devices, Inc., video decoders described in this reference manual. Select columns are described in full in the sections that follow.

Table 2. Description of Models of ADV7280A, ADV7281A, and ADV7282A Devices

Model Number	Video Input Pins	Differential AFE	Output Format	Diagnostic Pins	GPO Pins	Sync Output Pins	ACE	I²P	Package
ADV7280A	4	No	ITU-R BT.656	None	None	Yes	Yes	Yes	32-lead LFCSP, 5 mm × 5 mm
ADV7280A-M	8	No	MIPI Tx	None	3	No	Yes	Yes	32-lead LFCSP, 5 mm × 5 mm
ADV7281A-M	6	Yes	MIPI Tx	2	3	No	Yes	No	32-lead LFCSP, 5 mm × 5 mm
ADV7282A	4	Yes	ITU-R BT.656	2	None	No	Yes	Yes	32-lead LFCSP, 5 mm × 5 mm
ADV7282A-M	6	Yes	MIPI Tx	2	3	No	Yes	Yes	32-lead LFCSP, 5 mm × 5 mm

VIDEO INPUT PINS COLUMN

The video input pins column indicates how many analog video inputs pins are available on each model of the ADV7280A, ADV7281A, and ADV7282A devices. The following section outlines the number of pins required for each type of video input:

- One analog video input pin is required for single-ended CVBS inputs.
- Two analog video input pins are required for pseudo differential and fully differential CVBS inputs.
- Two analog video input pins are required for S-Video (Y/C) inputs.
- Three analog video input pins are required for component (YPbPr) inputs.

DIFFERENTIAL AFE COLUMN

The differential AFE column indicates if the ADV7280A, ADV7281A, and ADV7282A devices have a differential analog front end (AFE). A differential AFE is needed to process pseudo differential and fully differential CVBS inputs.

OUTPUT FORMAT COLUMN

The output format column indicates the digital video output format output from each ADV7280A, ADV7281A, and ADV7282A model.

- ITU-R BT.656 means that the ADV7280A, ADV7281A, or ADV7282A model outputs 8-bit YUV video data bus.
- MIPI Tx indicates that the ADV7280A-M, ADV7281A-M, and ADV7282A-M models output 8-bit YUV video data over a MIPI Tx bus. This MIPI Tx bus consists of one differential data channel (composed of the D0P and D0N signals) and one differential clock channel (composed of the CLKP and CLKN signals).

DIAGNOSTIC PINS COLUMN

The diagnostic pins column indicates if the ADV7280A, ADV7281A, and ADV7282A devices have diagnostic pins and how many diagnostic pins they have. Diagnostic pins monitor analog video input lines for STB events.

GPO PINS COLUMN

The GPIO pins column indicates if the ADV7280A, ADV7281A, and ADV7282A devices have general-purpose output (GPO) pins and how many GPO pins they have. GPO pins are outputs from the ADV7280A, ADV7281A, and ADV7282A devices that can control external devices.

SYNC OUTPUT PINS COLUMN

The SYNC output pins column indicates if the video decoder has synchronization output pins and how many synchronization output pins they have. Examples of synchronization output pins include horizontal synchronization (HS), vertical synchronization (VS), and subcarrier frequency lock (SFL).

ACE COLUMN

The ACE column indicates if the ADV7280A, ADV7281A, and ADV7282A devices have the ability to perform the ACE function.

The ACE function allows dark areas of the video brighten without saturating bright areas. This is useful for automotive applications.

I²P COLUMN

The I²P column indicates if the ADV7280A, ADV7281A, and ADV7282A devices have a built in I²P, or a deinterlacer. The I²P core converts the interlaced video formats of NTSC (480i) or PAL (576i) into progressive standards (480p or 576p).

PACKAGE COLUMN

The package column indicates the package in which the video decoder is available. See the ADV7280A, ADV7281A, and ADV7282A data sheets for the corresponding functional block diagrams.

INTERRUPTS AND STB FUNCTIONALITY

This section describes the interrupt operation of the ADV7280A, ADV7281A, and ADV7282A using the STB feature.

The ADV7281A and ADV7282A data sheets include an overview of the STB capabilities available in the ADV7281A-M, ADV7282A, and ADV7282A-M models. Use this section in conjunction with the ADV7281A and ADV7282A data sheets when using the STB feature.

PROGRAMMING DIAGNOSTIC INTERRUPT

This section describes how to program software interrupt bits to toggle when STB events are detected on the diagnostic pins. A hardware interrupt indicated by the INTRQ pin also triggers when a software interrupt activates. Details on how to control the INTRQ pin hardware interrupt are given in the Programming the Hardware Interrupt section.

Before programming the software diagnostic interrupts, the diagnostic circuitry must first be activated and the diagnostic slice level must be programmed; see the ADV7281A and ADV7282A data sheets for more information.

Unmask the diagnostic interrupts (that is, activate) using the DIAG_TRI1_L1_MSK and DIAG_TRI2_L1_MSK bits.

When a STB event is detected, the interrupt status bits DIAG_TRI1_L1 and DIAG_TRI2_L1 toggles from 0 to 1.

The DIAG_TRI1_L1 and DIAG_TRI2_L1 interrupts remains at 1 until they are cleared.

DIAG_TRI1_L1 and DIAG_TRI2_L1 interrupts are cleared by writing 1 to the DIAG_TRI1_L1_CLR and DIAG_TRI2_L1_CLR bits.

Unmasking Diagnostic Interrupts

The DIAG_TRI1_L1_MSK and DIAG_TRI2_L1_MSK bits unmask (that is, activate) the diagnostic interrupts.

DIAG_TRI1_L1_MSK, Address 0x55, Bit1, Interrupt/VDP Sub Map

Unmask Diagnostic Interrupt 1.This unmasks (that is, activates) the STB interrupt for Diagnostic Pin 1 (DIAG 1).

Table 3. DIAG_TRI1_L1_MSK Function

Setting	Description
0 (default)	Masks DIAG_TRI1_L1 interrupt
1	Unmasks DIAG_TRI1_L1 interrupt

DIAG_TRI2_L1_MSK, Address 0x55, Bit 3, Interrupt/VDP Sub Map

Unmask Diagnostic Interrupt 2.This unmasks (that is, activates) the STB interrupt for Diagnostic Pin 2 (DIAG 2).

Table 4. DIAG_TRI2_L1_MSK Function

Setting	Description
0 (default)	Masks DIAG_TRI2_L1 interrupt
1	Unmasks DIAG_TRI2_L1 interrupt

Diagnostic Interrupt Status

The DIAG_TRI1_L1 and DIAG_TRI2_L1 bits give the status of the diagnostic interrupt (that is, if a STB event occurs or not).

DIAG_TRI1_L1, Address 0x53, Bit 1, Interrupt/VDP Sub Map

Diagnostic Interrupt 1 status. This read only register shows the status of the interrupt for Diagnostic Pin 1, that is, if a STB event has occurred on the DIAG1 pin. An STB event is deemed to have occurred when the voltage on the DIAG1 pin exceeds the diagnostic slice level; see the ADV7281A and ADV7282A data sheets for more information. When triggered, the DIAG_TRI1_L1 bit remains high until cleared (see the Clearing Diagnostic Interrupts section).

Table 5. DIAG_TRI1_L1 Function

Setting	Description
0	Voltage higher than DIAG1_SLICE_LEVEL not detected on DIAG1 pin
1	Voltage higher than DIAG1_SLICE_LEVEL detected on DIAG1 pin

DIAG_TRI2_L1, Address 0x53, Bit 3, Interrupt/VDP Sub Map

Diagnostic Interrupt 2 status. This read only register, shows the status of the interrupt for Diagnostic Pin 2, that is, if a STB event has occurred on the DIAG2 pin. An STB event is deemed to have occurred when the voltage on the DIAG2 pin exceeds the diagnostic slice level; see the ADV7281A and ADV7282A data sheets for more information. When triggered, the DIAG_TRI2_L1 bit remains high until cleared (see the Clearing Diagnostic Interrupts section).

Table 6. DIAG_TRI2_L1 Function

Setting	Description
0	Voltage higher than DIAG2_SLICE_LEVEL not detected on the DIAG2 pin
1	Voltage higher than DIAG2_SLICE_LEVEL detected on the DIAG2 pin

Clearing Diagnostic Interrupts

The DIAG_TRI1_L1_CLR and DIAG_TRI2_L1_CLR bits clear the diagnostic interrupts.

DIAG_TRI1_L1_CLR, Address 0x54, Bit 1, Interrupt/VDP Sub Map

Clear Diagnostic Interrupt 1. This bit clears the interrupt for Diagnostic Pin 1 (DIAG1).

The DIAG_TRI1_L1_CLR is a self clearing, write only bit.

Table 7. DIAG_TRI1_L1_CLR Function

DIAG_TRI1_L1_CLR	Description
0 (default)	Do not clear DIAG_TRI1_L1
1	Clear DIAG_TRI1_L1

DIAG_TRI2_L1_CLR, Address 0x54, Bit 3, Interrupt/VDP Sub Map

Clear Diagnostic Interrupt 2. This bit clears the interrupt for Diagnostic Pin 2 (DIAG2).

The DIAG_TRI2_L1_CLR is a self clearing, write only bit.

Table 8. DIAG_TRI2_L1_CLR Function

Setting	Description
0 (default)	Do not clear DIAG_TRI2_L1
1	Clear DIAG_TRI2_L1

PROGRAMMING THE $\overline{\text{INTRQ}}$ HARDWARE INTERRUPT

When a software interrupt is unmasked and triggered, a hardware interrupt indicated by the $\overline{\text{INTRQ}}$ pin also automatically triggers.

An example of how to program a software interrupt is given in the Programming Diagnostic Interrupt section. Other software interrupts can be programmed in a similar manner. See Table 94 for other software interrupts available on the ADV7280A, ADV7281A-M, and ADV7282A devices.

The INTRQ_OP_SEL[1:0] bits program the $\overline{\text{INTRQ}}$ hardware interrupt to drive out in a variety of ways (for example, drive the $\overline{\text{INTRQ}}$ pin high, drive the $\overline{\text{INTRQ}}$ pin low, or make the $\overline{\text{INTRQ}}$ pin open drain).

The INTRQ_DUR_SEL[1:0] bits set the duration of the $\overline{\text{INTRQ}}$ interrupt output.

INTRQ_OP_SEL[1:0], Address 0x40 Bits[1:0], Interrupt/VDP Sub Map

The INTRQ_OP_SEL[1:0] bits program the $\overline{\text{INTRQ}}$ hardware interrupt to drive out in a variety of ways when active.

In open-drain mode, the $\overline{\text{INTRQ}}$ pin is at the D_{VDDIO} voltage when not active and drives low when active. The $\overline{\text{INTRQ}}$ pin requires a pull-up resistor to D_{VDDIO} for the $\overline{\text{INTRQ}}$ interrupt to work.

In drive low when active mode, the $\overline{\text{INTRQ}}$ pin is at D_{VDDIO} voltage when not active and drives low when active. The $\overline{\text{INTRQ}}$ pin does not require a pull-up resistor to D_{VDDIO}.

In drive high when active mode, the $\overline{\text{INTRQ}}$ pin is at ground (GND) when not active and drives high to D_{VDDIO} when active. The $\overline{\text{INTRQ}}$ pin does not require a pull-up resistor to D_{VDDIO}.

Table 9. INTRQ_OP_SEL[1:0] Function

Setting	Description
00 (default)	Open drain
01	Drive low when active
10	Drive high when active
11	Reserved

INTRQ_DUR_SEL[1:0], Address 0x40, Bits[7:6], Interrupt/VDP Sub Map

The INTRQ_DUR_SEL[1:0] bits set the duration of the $\overline{\text{INTRQ}}$ interrupt output.

The duration of the $\overline{\text{INTRQ}}$ interrupt output is given in terms of crystal clock periods. A28.63636 MHz crystal corresponds to a clock period of approximately 35 ns.

The $\overline{\text{INTRQ}}$ interrupt output can also be set to be active until cleared. In this mode of operation, the $\overline{\text{INTRQ}}$ pin is active until every active software interrupt clears.

Table 10. INTRQ_DUR_SEL[1:0] Function

Setting	Description
00 (default)	3 crystal periods (approximately 0.105 µs)
01	15 crystal periods (approximately 0.525 µs)
10	63 crystal periods (approximately 2.205 µs)
11	Active until cleared

ANALOG FRONT END

INPUT CONFIGURATION

The following two steps are key for configuring the ADV7280A, ADV7281A, and ADV7282A devices to correctly decode the input video:

1. Use the INSEL[4:0] bits to configure the routing and format decoding (CVBS, Y/C, or YPrPb).
2. If the input requirements are not met using the INSEL[4:0] options, the analog input muxing section must be configured manually to correctly route the video from the analog input pins to the ADC. Configure the SDP block, which decodes the digital data, to process the CVBS, Y/C, or YPrPb format. This is performed by the INSEL[4:0] setting.

For a full description of the INSEL[4:0] input formats, see the ADV7280A, ADV7281A, and ADV7282A data sheets.

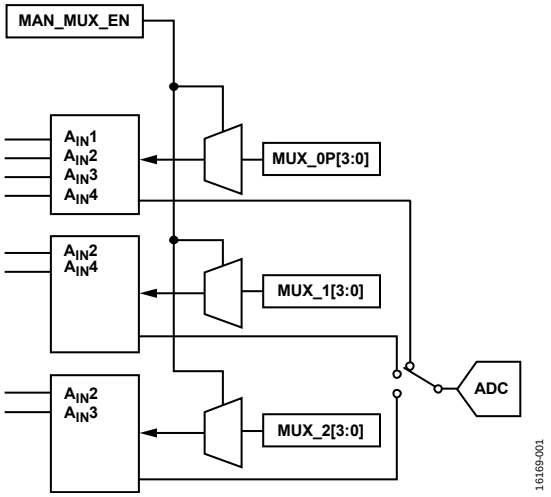

Figure 1. Manual Muxing Scheme for ADV7280A

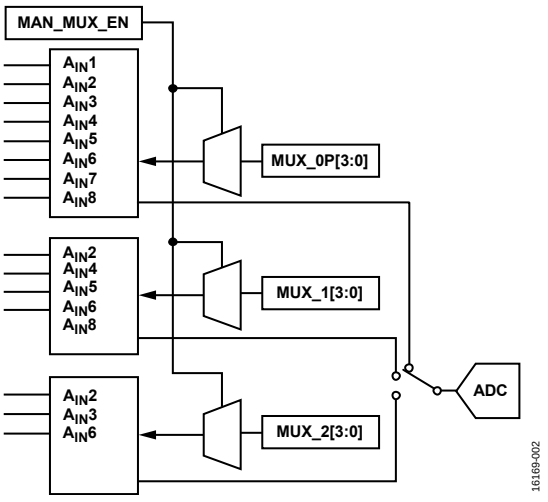

Figure 2. Manual Muxing Scheme for ADV7280A-M

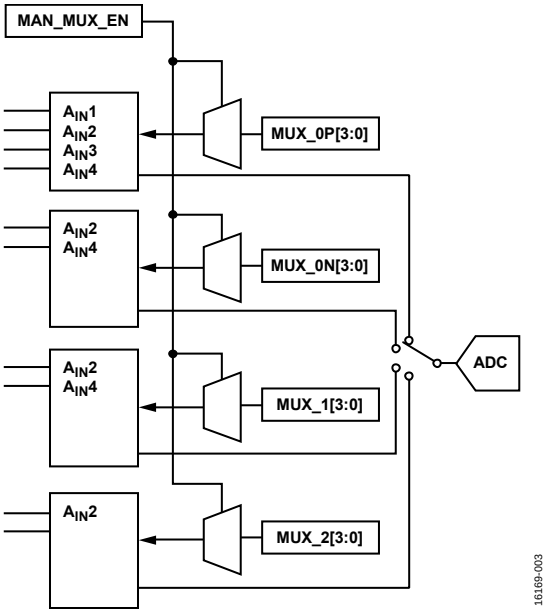

Figure 3. Manual Muxing Scheme for ADV7282A

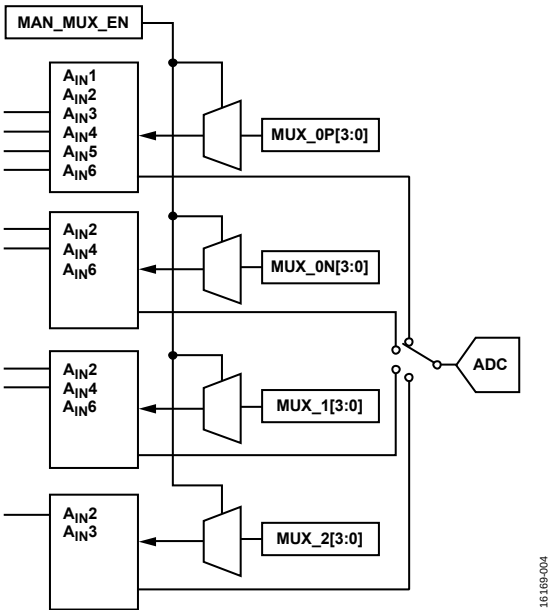

Figure 4. Manual Muxing Scheme for ADV7281A-M and ADV7282A-M

MANUAL MUXING MODE

In manual muxing mode, the user selects any analog input pin that is to be processed by the ADC of the ADV7280A, ADV7281A, and ADV7282A devices. MAN_MUX_EN (User Map, Register 0xC4, Bit 7) must be set to 1 to enable the following muxing blocks:

- MUX_0P[3:0], ADC mux configuration, Address 0xC3, Bits[3:0]
- MUX_0N[3:0], ADC mux configuration, Address 0x60, Bits[3:0] (applies only to the ADV7281A-M, ADV7282A, and ADV7282A-M models)
- MUX_1[3:0], ADC mux configuration, Address 0xC3, Bits[7:4]
- MUX_2[3:0], ADC mux configuration, Address 0xC4, Bits[3:0]

The four mux sections are controlled by the signal buses, MUX_0P[3:0], MUX_0N[3:0], MUX_2[3:0], and MUX_3[2:0].

Table 11 and Table 12 explains the control words used.

The input signal that contains the timing information (HS and VS) must be processed by MUX_0P[3:0]. For example, in a Y/C input configuration, connect MUX_0P[3:0] to the Y channel and MUX_1[3:0] to the C channel.

MUX_0N[3:0] only processes the negative input for fully differential or pseudo differential CVBS inputs.

When one or more muxes do not process video, such as the CVBS input, the idle mux and associated channel clamps and buffers must be powered down (see the description of Register 0x3A in the user sub map in Table 92).

MUX_0N[3:0] cannot be powered down independently. MUX_0N can only be powered down when MUX_0P[3:0], MUX_1[3:0], and MUX_2[3:0] are all powered down.

Manual Muxing of the ADV7280A and ADV7280A-M

Table 11 shows the settings for manual muxing of the ADV7280A. To setup manual muxing for the ADV7280A, complete the following steps:

- MAN_MUX_EN must be set to 1 (user sub map, Register 0xC4, Bit 7).
- CVBS can only be processed by MUX_0P[3:0].
- Y/C can only be processed by MUX_0P[3:0] and MUX_1[3:0]. MUX_0P[3:0] processes the luma (Y) and MUX_1[3:0] processes the chroma (C).
- Component (YPbPr) signals can only be processed by MUX_0P[3:0] (Y), MUX_1[3:0] (Pb), and MUX_2[3:0] (Pr).

Table 12 shows the settings for manual muxing of the ADV7280A-M. To setup manual muxing for ADV7280A-M, complete the following steps:

- MAN_MUX_EN must be set to 1 (User Map, Register 0xC4, Bit 7).
- CVBS can only be processed by MUX_0P[3:0].
- Y/C can only be processed by MUX_0P[3:0] and MUX_1[3:0]. MUX_0P[3:0] processes the luma (Y) and MUX_1[3:0] processes the chroma (C).
- Component (YPbPr) signals can only be processed by MUX_0P[3:0] (Y), MUX_1[3:0] (Pb), and MUX_2[3:0] (Pr).

Table 11. Manual Mux Settings for ADC of ADV7280A

MUX_0P[3:0]	ADC Connection	MUX_1[3:0]	ADC Connected To	MUX_2[3:0]	ADC Connection
0000	No connect	0000	No connect	0000	No connect
0001	$A_{IN}1$	0001	No connect	0001	No connect
0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$
0011	$A_{IN}3$	0011	No connect	0011	$A_{IN}3$
0100	$A_{IN}4$	0100	$A_{IN}4$	0100	No connect
0101 to 1111	No connect	0101 to 1111	No connect	0101 to 1111	No connect

Table 12. Manual Mux Settings for ADC of ADV7280A-M

MUX_0P[3:0]	ADC Connection	MUX_1[3:0]	ADC Connected To	MUX_2[3:0]	ADC Connection
0000	No connect	0000	No connect	0000	No connect
0001	$A_{IN}1$	0001	No connect	0001	No connect
0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$
0011	$A_{IN}3$	0011	No connect	0011	$A_{IN}3$
0100	$A_{IN}4$	0100	$A_{IN}4$	0100	No connect
0101	$A_{IN}5$	0101	$A_{IN}5$	0101	No connect
0110	$A_{IN}6$	0110	$A_{IN}6$	0110	$A_{IN}6$
0111	$A_{IN}7$	0111	No connect	0111	No connect
1000	$A_{IN}8$	1000	$A_{IN}8$	1000	No connect
1001 to 1111	No connect	1001 to 1111	No connect	1001 to 1111	No connect

Manual Muxing of the ADV7282A

Table 14 shows the settings for manual muxing of the ADV7282A. To setup manual muxing for ADV7282A, complete the following steps:

- MAN_MUX_EN must be set to 1 (user sub map, Register 0xC4, Bit 7)
- CVBS can only be processed by MUX_0P[3:0].
- Differential CVBS can only be processed by MUX_0P[3:0] (positive channel) and MUX_0N[3:0] (negative channel).
- Y/C can only be processed by MUX_0P[3:0] and MUX_1[3:0]. MUX_0P[3:0] processes the luma (Y) and MUX_1[3:0] processes the chroma (C).
- Component (YPbPr) signals can only be processed by MUX_0P[3:0] (Y), MUX_1[3:0] (Pb), and MUX_2[3:0] (Pr). For example, Y can be fed in on $A_{IN}1$ or $A_{IN}3$ for MUX_0P[3:0]. Pb can be fed in on $A_{IN}4$ for MUX_1[3:0]. Pr can be fed in on $A_{IN}2$ for MUX_2[3:0]. Table 13 gives an example of how to program the ADV7282A to accept YPrPb inputs.

Table 13. Register Writes to Program the ADV7282A to Accept YPbPr Input

Register Map	Register Address	Register Write	Description
User Sub Map	0x00	0x0C	Program INSEL[4:0] for YPbPr input.
	0xC3	0x87	Program manual muxing. Y is fed in on $A_{IN}3$ for MUX_0P[3:0]. Pb is fed in on $A_{IN}4$ for MUX_1[3:0].
	0xC4	0x82	Enable manual muxing. Pr is fed in on $A_{IN}2$ for MUX_2[3:0].

Table 14. Manual Mux Settings for ADC of ADV7282A

MUX_0P[3:0]	ADC Connection	MUX_0N[3:0]	ADC Connection	MUX_1[3:0]	ADC Connection	MUX_2[3:0]	ADC Connection
0000	No connect	0000	No connect	0000	No connect	0000	No connect
0001	$A_{IN}1$	0001	No connect	0001	No connect	0001	No connect
0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$
0011	No connect	0011	No connect	0011	No connect	0011	No connect
0100	No connect	0100	No connect	0100	No connect	0100	No connect
0101	No connect	0101	No connect	0101	No connect	0101	No connect
0110	No connect	0110	No connect	0110	No connect	0110	No connect
0111	$A_{IN}3$	0111	No connect	0111	No connect	0111	No connect
1000	$A_{IN}4$	1000	$A_{IN}4$	1000	$A_{IN}4$	1000	No connect
1001 to 1111	No connect	1001 to 1111	No connect	1001 to 1111	No connect	1001 to 1111	No connect

Manual Muxing of the ADV7281A-M and ADV7282A-M

Table 15 shows the settings for manual muxing of the ADV7281A-M and ADV7282A-M. To set up manual muxing for ADV7281A-M or ADV7282A-M, complete the following steps:

- MAN_MUX_EN must be set to 1 (user sub map, Register 0xC4, Bit 7)
- CVBS can only be processed by MUX_0P[3:0].
- Differential CVBS can only be processed by MUX_0P[3:0] (positive channel) and MUX_0N[3:0] (negative channel).
- Y/C can only be processed by MUX_0P[3:0] and MUX_1[3:0]. MUX_0P[3:0] processes the luma (Y) and MUX_1 processes the chroma (C).
- Component (YPbPr) signals can only be processed by MUX_0P[3:0] (Y), MUX_1[3:0] (Pb), and MUX_2[3:0] (Pr).

Table 15. Manual Mux Settings for ADC of ADV7281A-M and ADV7282A-M

MUX_0P[3:0]	ADC Connection	MUX_0N[3:0]	ADC Connection	MUX_1[3:0]	ADC Connection	MUX_2[3:0]	ADC Connection
0000	No connect	0000	No connect	0000	No connect	0000	No connect
0001	$A_{IN}1$	0001	No connect	0001	No connect	0001	No connect
0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$
0011	$A_{IN}3$	0011	No connect	0011	No connect	0011	$A_{IN}3$
0100	$A_{IN}4$	0100	$A_{IN}4$	0100	$A_{IN}4$	0100	No connect
0101	No connect	0101	No connect	0101	No connect	0101	No connect
0110	No connect	0110	No connect	0110	No connect	0110	No connect
0111	$A_{IN}5$	0111	No connect	0111	No connect	0111	No connect
1000	$A_{IN}6$	1000	$A_{IN}6$	1000	$A_{IN}6$	1000	No connect
1001 to 1111	No connect	1001 to 1111	No connect	1001 to 1111	No connect	1001 to 1111	No connect

ANTIALIASING FILTERS

The ADV7280A, ADV7281A, and ADV7282A devices have optional on-chip antialiasing (AA) filters on each of the four channels that are multiplexed to the ADC (see Figure 5).

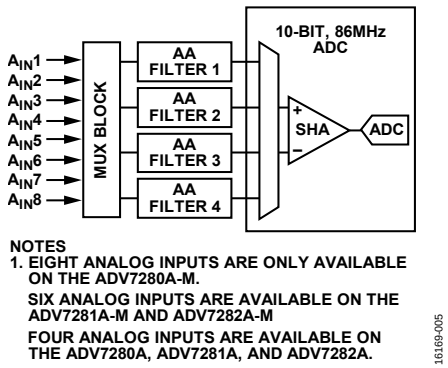

Figure 5. Antialias Filter Configuration

The filters are designed for SD video up to 10 MHz bandwidth. Figure 6 and Figure 7 show the filter magnitude and phase characteristics.

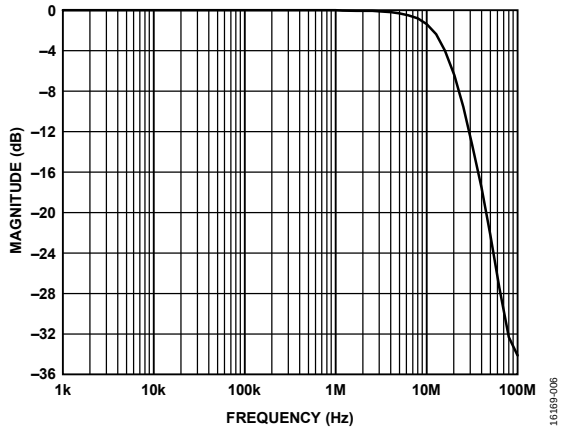

Figure 6. Antialiasing Filter Magnitude Response

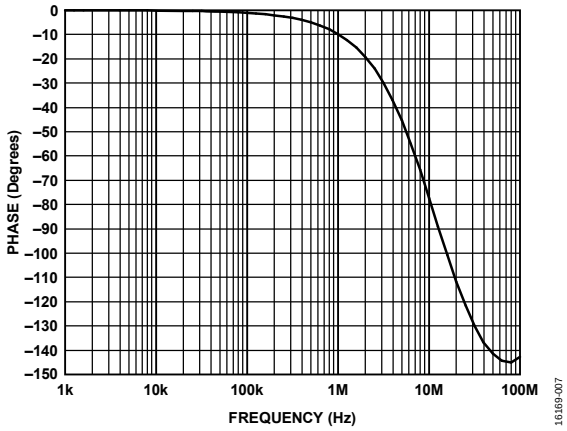

Figure 7. Antialiasing Filter Phase Response

The antialiasing filters are enabled by default and the selection of INSEL[4:0] determines which filters are powered up at any given time. For example, if CVBS mode is selected, the filter circuits for the remaining input channels are powered down to conserve power. However, the antialiasing filters can be disabled or bypassed using the AA_FILT_MAN_OVR control.

ANTIALIASING FILTER CONFIGURATION

AA_FILT_MAN_OVR, Address 0xF3, Bit 4, User Sub Map

This feature allows the user to override the antialiasing filters on/off settings, which are automatically selected by INSEL[4:0].

AA_FILT_EN3 to AA_FILT_EN0, Address 0xF3, Bits[3:0], User Sub Map

These bits allow the user to enable or disable the antialiasing filters on each of the three input channels multiplexed to the ADC. When disabled, the analog signal bypasses the AA filters and is routed directly to the ADC.

AA_FILT_EN[0], Address 0xF3, Bit 0

When AA_FILT_EN[0] is set to 0, AA Filter 1 is disabled.

When AA_FILT_EN[0] is set to 1, AA Filter 1 is enabled.

AA_FILT_EN[1], Address 0xF3, Bit 1

When AA_FILT_EN[1] is set to 0, AA Filter 2 is disabled.

When AA_FILT_EN[1] is set to 1, AA Filter 2 is enabled.

AA_FILT_EN[2], Address 0xF3, Bit 2

When AA_FILT_EN[2] is set to 0, AA Filter 3 is disabled.

When AA_FILT_EN[2] is set to 1, AA Filter 3 is enabled.

AA_FILT_EN[3], Address 0xF3, Bit 2

When AA_FILT_EN[3] is set to 0, AA Filter 4 is disabled.

When AA_FILT_EN[3] is set to 1, AA Filter 4 is enabled.

GLOBAL CONTROL REGISTERS

The register control bits listed in this section affect the entire chip.

POWER SAVING MODE AND RESET CONTROL

Power Down

PWRDWN, Address 0x0F, Bit 5, User Sub Map

The ADV7280A, ADV7281A, and ADV7282A devices can be placed into a chip wide, power-down mode by setting the PWRDWN bit or by using the $\overline{\text{PWRDWN}}$ pin. The power-down mode stops the clock from entering the digital section of the chip, thereby freezing its operation. No I²C bits are lost during power-down mode. The PWRDWN bit also affects the analog blocks and switches them into low current modes. The I²C interface is unaffected and remains operational in power-down mode.

When PWRDWN is set to 0, the chip is operational. When PWRDWN is set to 1 (default), the ADV7280A, ADV7281A, and ADV7282A devices are in a chip wide, power-down mode.

Chip Reset

Reset, Address 0x0F, Bit 7, User Sub Map

Setting this bit, which is equivalent to controlling the $\overline{\text{RESET}}$ pin on the ADV7280A, ADV7281A, and ADV7282A devices, issues a full chip reset. All I²C registers are reset to their default/power-up values. Some register bits do not have a reset value specified; they keep their last written value. Those bits are marked as having a reset value of X in the register tables (see Table 92 and Table 94). After the reset sequence, the devices immediately start to acquire the incoming video signal.

After setting the reset bit (or initiating a reset via the $\overline{\text{RESET}}$ pin), the part returns to the default for its primary mode of operation. All I²C bits are loaded with their default values, making this bit self clearing. Executing a software reset takes approximately 2 ms. However, it is recommended to wait 5 ms before any further I²C writes are performed.

The I²C master controller receives a no acknowledge condition on the ninth clock cycle when a chip reset is implemented.

When the reset bit is set to 0 (default), operation is normal.

When the reset bit is set to 1, the reset sequence starts.

GLOBAL PIN CONTROL

Drive Strength Selection (I²C)

DR_STR_S[1:0], Address 0xF4, Bits[1:0], User Sub Map

The DR_STR_S[1:0] bits allow the user to select the strength of the I²C signal output drivers. These bits affect the drive strength for the SDATA and SCLK pins.

Table 16. DR_STR_S Function

Setting	Description
00	Low drive strength (1×)[1]
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

[1] The low drive strength setting is not recommended for the optimal performance of the ADV7280A, ADV7281A, and ADV7282A devices.

GENERAL-PURPOSE OUTPUT (GPO) CONTROLS

The ADV7280A-M, ADV7281A-M, and ADV7282A-M have three GPOs.

These outputs allow the user to control other devices in a system via the I²C port of the device. See Table 17 for the GPO truth table.

GPO_ENABLE, Address 0x59, Bit 4, User Sub Map

When GPO_ENABLE is set to 0 (default), all GPO pins are tristated.

When GPO_ENABLE is set to 1, all GPO pins are in a driven state. The polarity output from each GPO is controlled by GPO[3:0].

GPO[2] to GPO[0], Address 0x59, Bits[2:0], User Sub Map

Individual control of the four GPO ports is achieved using GPO[2:0].

GPO_ENABLE must be set to 1 for the GPO pins to become active.

GPO[0]

When GPO[0] is set to 0 (default), Logic 0 is output from the GPO0 pin.

When GPO[0] is set to 1, Logic 1 is output from the GPO0 pin.

GPO[1]

When GPO[1] is set to 0 (default), Logic 0 is output from the GPO1 pin.

When GPO[1] is set to 1, Logic 1 is output from the GPO1 pin.

GPO[2]

When GPO[2] is set to 0 (default), Logic 0 is output from the GPO2 pin.

When GPO[2] is set to 1, Logic 1 is output from the GPO2 pin.

Table 17. GPO Registers Truth Table

GPO_ENABLE	GPO[2:0]	GPO2	GPO1	GPO0
0	XXX[1]	Z[2]	Z[2]	Z[2]
1	000	0	0	0
1	001	0	0	1
1	010	0	1	0
1	011	0	1	1
1	100	1	0	0
1	101	1	0	1
1	110	1	1	0
1	111	1	1	1

[1] X means don't care.
[2] Z means high-Z.

GLOBAL STATUS REGISTER

Four registers provide summary information about the video decoder. The IDENT register allows the user to identify the revision code of the ADV7280A, ADV7281A, and ADV7282A devices. The other three registers (Address 0x10, Address 0x12, and Address 0x13) contain status bits from the ADV7280A, ADV7281A, and ADV7282A devices.

Depending on the setting of the FSCLE bit, the status registers are based solely on horizontal timing information or on the horizontal timing and lock status of the color subcarrier. See the FSCLE, Address 0x51 section.

IDENTIFICATION

IDENT[7:0], Address 0x11[7:0], User Sub Map

This is the register identification of the ADV7280A, ADV7281A, and ADV7282A devices revision (see Table 18).

Table 18. IDENT[7:0] Code

Address	Description
0x42	Production silicon

STATUS 1

Status 1, Address 0x10, Bits[7:0], User Sub Map

This read only register provides information about the internal status of the ADV7280A, ADV7281A, and ADV7282A devices.

See the CIL[2:0], Address 0x51, Bits[2:0], User Sub Map section and the COL[2:0], Address 0x51, Bits[5:3], User Sub Map section for details on timing.

Table 19. Status 1 Function

Bit	Bit Name	Description
7	COL_KILL	Color kill active
6:4	AD_RESULT[2:0]	Result of autodetection
3	FOLLOW_PW	AGC follows peak white algorithm
2	FSC_LOCK	f_{SC} locked (now)
1	LOST_LOCK	Lost lock (since last read)
0	IN_LOCK	In lock (now)

STATUS 2

Status 2, Address 0x12, Bits[7:0], User Sub Map

Table 20. Status 2 Function

Bit	Bit Name	Description
7	Reserved	Reserved
6	Reserved	Reserved
5	FSC_NSTD	Subcarrier frequency (f_{SC}) is nonstandard
4	LL_NSTD	Line length is nonstandard
3	MV_AGC_DET	Detected Rovi AGC pulses
2	MV_PS_DET	Detected Rovi pseudo sync pulses
1	MVCS_T3	Rovi color striping protection; conforms to Type 3 if high, Type 2 if low
0	MVCS_DET	Detected Rovi (previously Macrovision) color striping

STATUS 3

Status 3, Address 0x13, Bits[7:0], User Sub Map

Table 21. Status 3 Function

Bit	Bit Name	Description
7	PAL_SW_LOCK	Reliable sequence of swinging bursts detected
6	Interlaced	Interlaced video detected (field sequence found)
5	STD_FLD_LEN	Field length is correct for currently selected video standard
4	FREE_RUN_ACT	Flags if ADV7280A, ADV7281A, and ADV7282A devices enters free run mode (see the Free Run Operation section)
3	Reserved	Reserved
2	SD_OP_50Hz	Flags whether 50 Hz or 60 Hz is present at output
1	Reserved	Reserved
0	INST_HLOCK	Horizontal lock achieved

AUTODETECTION RESULT

AD_RESULT[2:0], Address 0x10, Bits [6:4], User Sub Map

The AD_RESULT[2:0] bits report back on the findings from the ADV7280A, ADV7281A, and ADV7282A devices autodetection block. See the General Setup section for more information on enabling the autodetection block and the Autodetection of SD Modes section for more information on how to configure it.

Table 22. AD_RESULT[2:0] Function

Setting	Description
000	NTSC M/NTSC J
001	NTSC 4.43
010	PAL M
011	PAL 60
100	PAL B/PAL G/PAL H/PAL I/PAL D
101	SECAM
110	PAL Combination N
111	SECAM 525

VIDEO PROCESSOR

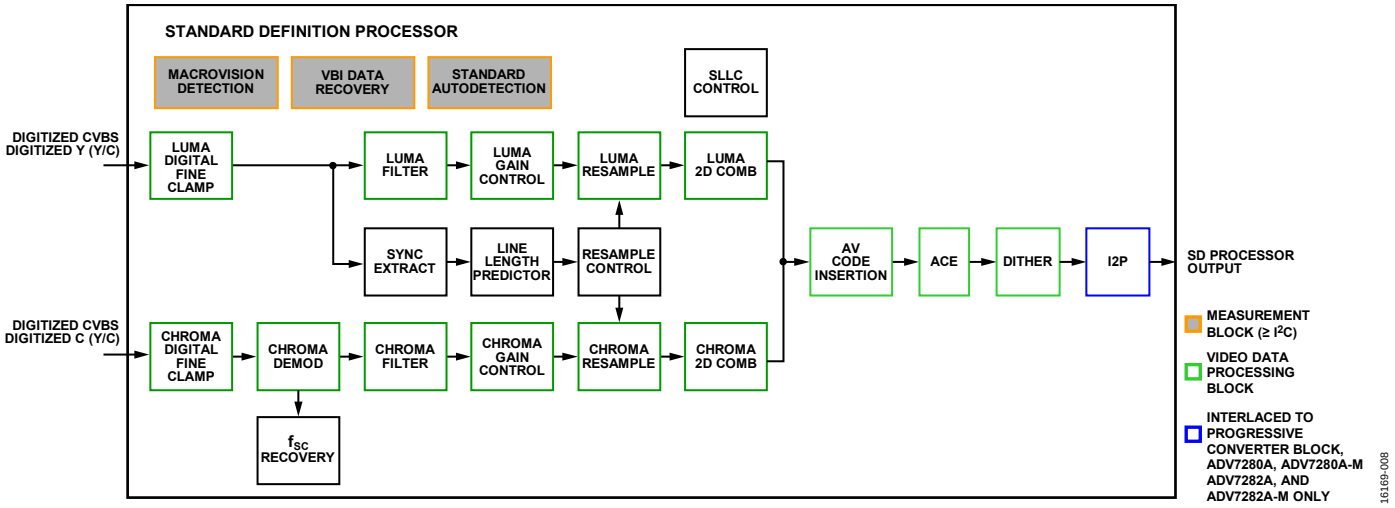

Figure 8. Block Diagram of Video Processor

Figure 8 shows a block diagram of the video processor within the ADV7280A, ADV7281A, and ADV7282A devices. The devices can handle SD video in CVBS, Y/C, and YPrPb formats. It can be divided into a luminance and chrominance path. If the input video is of a composite type (CVBS), both processing paths are fed with the CVBS input. The output from the video processor is fed into a MIPI Tx block in the ADV7280A-M, ADV7281A-M, and ADV7282A-M models. In the ADV7280A and ADV7282A models, the output of the video processor is output from the devices in an ITU-R BT.656 video stream.

SD LUMA PATH

The analog video signal received is processed by the following blocks:

- Luma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Luma filter. This block contains a luma decimation filter (YAA) with a fixed response and some shaping filters (YSH) that have selectable responses.
- Luma gain control. The AGC can operate on a variety of different modes, including gain based on the depth of the horizontal sync pulse, peak white mode, and fixed manual gain.
- Luma resample. To correct for line length errors as well as dynamic line length changes, the data is digitally resampled.
- Luma 2D comb. The 2D comb filter provides Y/C separation.
- Active video (AV) code insertion. At this point, the decoded luma (Y) signal is merged with the retrieved chroma values. AV codes can be inserted (as per ITU-R BT.656).

SD CHROMA PATH

The input signal is processed by the following blocks:

- Chroma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Chroma demodulation. This block employs a color subcarrier signal (f_{SC}) recovery unit to regenerate the color subcarrier for any modulated chroma scheme. The demodulation block then performs an AM demodulation for PAL and NTSC, and an FM demodulation for SECAM.
- Chroma filter. This block contains a chroma decimation filter (CAA) with a fixed response and some shaping filters (CSH) that have selectable responses.
- Chroma gain control. AGC can operate on several different modes, including gain based on the color subcarrier amplitude, gain based on the depth of the horizontal sync pulse on the luma channel, or fixed manual gain.
- Chroma resample. The chroma data is digitally resampled to keep it perfectly aligned with the luma data. The resampling i corrects static and dynamic line length errors of the incoming video signal.
- Chroma 2D comb. The 2D, five-line, super adaptive comb filter provides high quality Y/C separation if the input signal is CVBS.
- AV code insertion. At this point, the demodulated chroma (Cr and Cb) signal is merged with the retrieved luma values. AV codes can be inserted (as per ITU-R BT.656).

ACE, I²P, AND DITHER PROCESSING BLOCKS

- ACE. This block offers improved visual detail by using an algorithm to automatically vary the contrast levels to enhance picture detail. See the ACE section.
- Dither. When enabled, this block converts the digital output of the ADV7280A, ADV7281A, and ADV7282A devices from 8-bit pixel data down to 6-bit pixel data. This function makes it easier for the devices to communicate with some liquid crystal display (LCD) panels. See the Dither Function section.
- Interlaced to progressive converter (I²P). This block is only available in the ADV7280A, ADV7280A-M, ADV7282A, and ADV7282A-M models. This block converts interlaced video formats (480i and 576i) into progressive video formats (480p and 576p).

SYNC PROCESSING

TheADV7280A, ADV7281A, and ADV7282A devices extract syncs embedded in the analog input video signal. The sync extraction is optimized to support imperfect video sources, such as VCRs with head switches. The coded algorithm used employs a coarse detection based on a threshold crossing, followed by a more detailed detection using an adaptive interpolation algorithm. The raw sync information is sent to a line length measurement and prediction block. The output of this then drives the digital resampling section to ensure the ADV7280A, ADV7281A, and ADV7282A devices output 720 active pixels per line.

The sync processing on the ADV7280A, ADV7281A, and ADV7282A devices also include the following specialized postprocessing blocks that filter and condition the raw sync information retrieved from the digitized analog video:

- VS single processor. This block provides extra filtering of the detected VSYNCs to improve vertical lock.
- HS single processor. The HSYNC processor is designed to filter incoming HSYNCs that were corrupted by noise, providing much improved performance for video signals with a stable time base, but poor SNR.

VBI DATA RECOVERY

The ADV7280A, ADV7281A, and ADV7282A devices can retrieve the following information from the input video vertical blanking interval:

- WSS
- (CGMS
- CCAP
- Rovi protection presence
- Teletext

The ADV7280A, ADV7281A, and ADV7282A devices are also capable of automatically detecting the incoming video standard with respect to the following:

- Color subcarrier frequency
- Field rate
- Line rate

The ADV7280A, ADV7281A, and ADV7282A devices can configure to support PAL B/PAL D/ PAL I/PAL G/PAL H, PAL M, PAL N, PAL Combination N, NTSC M/NTSC J, SECAM 50 Hz/ 60 Hz, NTSC 4.43, and PAL 60 formats.

GENERAL SETUP

Video Standard Selection

The VID_SEL[3:0] bits (Address 0x02, Bits[7:4]) allow the user to force the digital core into a specific video standard, which is not necessary under normal circumstances. The VID_SEL[3:0] bits default to an autodetection mode that supports PAL, NTSC, SECAM, and other variants.

Autodetection of SD Modes

To guide the autodetect system of the ADV7280A, ADV7281A, and ADV7282A devices, individual enable bits are provided for each of the supported video standards. Setting the relevant bit to 0 inhibits the standard from being detected automatically. Instead, the system chooses the closest of the remaining enabled standards. The results of the autodetection block can be read back via the status registers (see the Global Status Register section for more information).

VID_SEL[3:0], Address 0x02, Bits[7:4], User Sub Map

Table 23. VID_SEL Function

Setting	Description
0000 (default)	Autodetect PAL B/PAL G/PAL H/PAL I/PAL D, NTSC J (no pedestal), SECAM
0001	Autodetect PAL B/PAL G/PAL H/PAL I/PAL D, NTSC M (pedestal), SECAM
0010	Autodetect PAL N (pedestal), NTSC J (no pedestal), SECAM
0011	Autodetect PAL N (pedestal), NTSC M (pedestal), SECAM
0100	NTSC J
0101	NTSC M
0110	PAL 60
0111	NTSC 4.43
1000	PAL B/PAL G/PAL H/PAL I/PAL D
1001	PAL N = PAL B/PAL G/PAL H/PAL I/PAL D (with pedestal)
1010	PAL M (without pedestal)
1011	PAL M
1100	PAL Combination N
1101	PAL Combination N (with pedestal)
1110	SECAM
1111	SECAM

AD_SEC525_EN, Address 0x07, Bit 7, User Sub Map

Setting AD_SEC525_EN to 0 (default) disables the autodetection of a 525 line system with a SECAM style, FM-modulated color component.

Setting AD_SEC525_EN to 1 enables the detection of a SECAM style, FM modulated color component.

AD_SECAM_EN, Address 0x07, Bit 6, User Sub Map

Setting AD_SECAM_EN to 0 disables the autodetection of SECAM.

Setting AD_SECAM_EN to 1 (default) enables the detection of SECAM.

AD_N443_EN, Address 0x07, Bit 5, User Sub Map

Setting AD_N443_EN to 0 disables the autodetection of NTSC style systems with a 4.43 MHz color subcarrier.

Setting AD_N443_EN to 1 (default) enables the detection of NTSC style systems with a 4.43 MHz color subcarrier.

AD_P60_EN, Address 0x07, Bit 4, User Sub Map

Setting AD_P60_EN to 0 disables the autodetection of PAL systems with a 60 Hz field rate.

Setting AD_P60_EN to 1 (default) enables the detection of PAL systems with a 60 Hz field rate.

AD_PALN_EN, Address 0x07, Bit 3, User Sub Map

Setting AD_PALN_EN to 0 disables the detection of the PAL N standard.

Setting AD_PALN_EN to 1 (default) enables the detection of the PAL N standard.

AD_PALM_EN, Address 0x07, Bit 2, User Sub Map

Setting AD_PALM_EN to 0 disables the autodetection of PAL M.

Setting AD_PALM_EN to 1 (default) enables the detection of PAL M.

AD_NTSC_EN, Address 0x07, Bit 1, User Sub Map

Setting AD_NTSC_EN to 0 disables the detection of standard NTSC.

Setting AD_NTSC_EN to 1 (default) enables the detection of standard NTSC.

AD_PAL_EN, Address 0x07, Bit 0, User Sub Map

Setting AD_PAL_EN to 0 disables the detection of standard PAL.

Setting AD_PAL_EN to 1 (default) enables the detection of standard PAL.

SFL_INV, Address 0x41, Bit 6 (ADV7280A Only), User Sub Map

The subcarrier frequency lock (SFL) inversion bit controls the behavior of the PAL switch bit in the SFL (genlock telegram) data stream. Implemented to solve compatibility issues with video encoders, it solves two problems.

First, the PAL switch bit is meaningful only in PAL. Some encoders (including Analog devices encoders) also look at the state of this bit in NTSC.

Second, it overcomes interfacing issues between different generations of Analog devices video encoders. Older generations (for example, the ADV7194) used the SFL (genlock telegram) bit directly. Newer encoders (for example, the ADV7174/ADV7179, ADV7340/ADV7341, ADV7342/ADV7343, and ADV7344, ADV7390/ADV7391/ADV7392/ADV7393) invert the bit prior to using it, meaning the inversion compensated for the one-line delay of an SFL (genlock telegram) transmission.

As a result, for newer encoders, the PAL switch bit in the SFL (genlock telegram) must be set to 0 for NTSC to work. For older video encoders, the PAL switch bit in the SFL must be set to 1 to work in NTSC. If the state of the PAL switch bit is wrong, a 180° phase shift occurs.

In a decoder/encoder back to back system in which SFL is used, this bit must be set up properly for the specific encoder used.

Setting SFL_INV to 0 (default) makes the device SFL compatible with the ADV7174/ADV7179, ADV7340/ADV7341, ADV7342/ADV7343, ADV7344, and ADV7390/ADV7391/ADV7392/ADV7393 video encoders.

Setting SFL_INV to 1 makes the devices SFL compatible with the older video encoders.

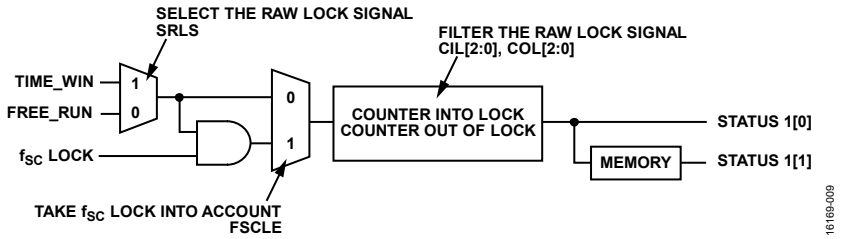

Figure 9. Lock Related Signal Path

Lock Related Controls

Lock information is presented to the user through Bits[2:0] of the Status 1 register (see the Status 1, Address 0x10, Bits[7:0] section). Figure 9 outlines the signal flow and the controls that are available to influence the way the lock status information is generated.

SRLS, Address 0x51, Bit 6, User Sub Map

Using the select raw lock signal (SRLS) bit, the user can choose between two sources for determining the lock status (per Bits[1:0] in the Status 1 register). See Figure 9.

- The FREE_RUN signal evaluates the properties of the incoming video over several fields, taking vertical synchronization information into account.
- The TIME_WIN signal is based on a line to line evaluation of the horizontal synchronization pulse of the incoming video.

Setting SRLS to 0 (default) selects the FREE_RUN signal to evaluate over several fields.

Setting SRLS to 1 selects the TIME_WIN signal to evaluate on a line to line basis.

FSCLE, Address 0x51, Bit 6, User Sub Map

The f_{SC} lock enable (FSCLE) bit allows the user to choose whether the status of the color subcarrier loop is taken into account when the overall lock status is determined and presented via Bits[1:0] in the Status 1 register. This bit must be set to 0 when operating the ADV7280A, ADV7281A, and ADV7282A devices in YPrPb component mode to generate a reliable INST_HLOCK status bit.

When FSCLE is set to 0 (default), the overall lock status is dependent only on horizontal sync lock.

When FSCLE is set to 1, the overall lock status is dependent on horizontal sync lock and f_{SC} lock.

COL[2:0], Address 0x51, Bits[5:3], User Sub Map

COL[2:0] determines the number of consecutive lines for which the out of lock condition must be true before the system switches into the unlocked state and reports this via Register Status 1, Bits[1:0]. It counts the value in lines of video.

Table 24. COL[2:0] Function

Setting	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

CIL[2:0], Address 0x51, Bits[2:0], User Sub Map

CIL[2:0] (count into lock) determines the number of consecutive lines for which the lock condition must be true before the system switches into the locked state and reports this via Register Status 1, Bits[1:0]. The bit counts the value in lines of video.

Table 25. CIL[2:0] Function

Setting	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

COLOR CONTROLS

These registers allow the user to control picture appearance, including control of active data in the event of video being lost. These controls are independent of any other controls. For instance, brightness control is independent of picture clamping, although both controls affect the dc level of the signal.

CON[7:0], Address 0x08, Bits[7:0], User Sub Map

This register allows the user to control contrast adjustment of the picture.

Table 26. CON[7:0] Function

Setting	Description
0x80 (default)	Gain on luma channel = 1
0x00	Gain on luma channel = 0
0xFF	Gain on luma channel = 2

SD_SAT_Cb[7:0], Address 0xE3, Bits[7:0], User Sub Map

This register allows the user to control the gain of the Cb channel only, which in turn adjusts the saturation of the picture.

Table 27. SD_SAT_Cb[7:0] Function

Setting	Description
0x80 (default)	Gain on Cb channel = 0 dB
0x00	Gain on Cb channel = −42 dB
0xFF	Gain on Cb channel = +6 dB

SD_SAT_Cr[7:0], Address 0xE4, Bits[7:0], User Sub Map

This register allows the user to control the gain of the Cr channel only, which in turn adjusts the saturation of the picture.

Table 28. SD_SAT_Cr[7:0] Function

Setting	Description
0x00	Gain on Cr channel = −42 dB
0x80 (default)	Gain on Cr channel = 0 dB
0xFF	Gain on Cr channel = +6 dB

SD_OFF_Cb[7:0], Address 0xE1, Bits[7:0], User Sub Map

This register allows the user to select an offset for the Cb channel only and to adjust the hue of the picture. There is a functional overlap with the HUE[7:0] register (Address 0x0B, User Sub Map).

Table 29. SD_OFF_Cb[7:0] Function

Setting	Description
0x00	−312 mV offset applied to the Cb channel
0x80 (default)	0 mV offset applied to the Cb channel
0xFF	+312 mV offset applied to the Cb channel

SD_OFF_Cr[7:0], Address 0xE2, Bits[7:0], User Sub Map

This register allows the user to select an offset for the Cr channel only and to adjust the hue of the picture. There is a functional overlap with the HUE[7:0] register.

Table 30. SD_OFF_Cr[7:0] Function

Setting	Description
0x00	−312 mV offset applied to the Cr channel
0x80 (default)	0 mV offset applied to the Cr channel
0xFF	+312 mV offset applied to the Cr channel

BRI[7:0], Address 0x0A, Bits[7:0], User Sub Map

This register controls the brightness of the video signal. It allows the user to adjust the brightness of the picture.

Table 31. BRI[7:0] Function

Setting	Description
0x00 (default)	Offset of the luma channel = 0 IRE
0x7F	Offset of the luma channel = +30 IRE
0x80	Offset of the luma channel = −30 IRE

HUE[7:0], Address 0x0B, Bits[7:0], User Sub Map

This register contains the value for the color hue adjustment. It allows the user to adjust the hue of the picture.

HUE[7:0] has a range of ±90°, with 0x00 equivalent to an adjustment of 0°. The resolution of HUE[7:0] is 1 bit = 0.7°.

The hue adjustment value is fed into the AM color demodulation block. Therefore, it applies only to video signals that contain chroma information in the form of an AM modulated carrier (CVBS or Y/C in PAL or NTSC). It does not affect SECAM and does not work on component video inputs (YPrPb).

Table 32. HUE[7:0] Function

Setting	Description
0x00 (default)	Phase of the chroma signal = 0°
0x7F	Phase of the chroma signal = −90°
0x80	Phase of the chroma signal = +90°

DEF_Y[5:0], Address 0x0C, Bits[7:2], User Sub Map

When the ADV7280A, ADV7281A, and ADV7282A devices lose lock on the incoming video signal or when there is no input signal, the DEF_Y[5:0] register allows the user to specify a default luma value to be output. This value is used under the following conditions:

- If the DEF_VAL_AUTO_EN bit is set to 1 and the ADV7280A, ADV7281A, and ADV7282A devices have lost lock to the input video signal, this is the intended mode of operation (automatic mode).
- If the DEF_VAL_EN bit is set to 1, regardless of the lock status of the video decoder, this is a forced mode that may be useful during configuration.

The DEF_Y[5:0] values define the six MSBs of the output video. The remaining LSBs are padded with 0s. For example, in 8-bit mode, the output is Y[7:0] = (DEF_Y[5:0], 0, 0).

The default value of Register 0x0C is 0x36, which equates to a value of 0x0D for DEF_Y[5:0]. The default output color is blue.

DEF_C[7:0], Address 0x0D, Bits[7:0], User Sub Map

The Default Value C (DEF_C[7:0]) register complements the DEF_Y[5:0] value. It defines the four MSBs of Cr and Cb values to be output if

- The DEF_VAL_AUTO_EN bit is set to high and the ADV7280A, ADV7281A, and ADV7282A devices cannot lock to the input video (automatic mode).
- The DEF_VAL_EN bit is set to high (forced output).

The DEF_C[7:0] control is composed of a red chroma control (Cr[3:0] is contained in DEF_C[7:4]) and a blue chroma control (Cb[3:0] is contained in DEF_C[3:0]).

The default value of DEF_C[7:0] is 0x7C. The default output colour is blue.

FREE RUN OPERATION

Free run mode provides the user with a stable clock and predictable data if the input signal cannot be decoded, for example, if input video is not present.

The ADV7280A, ADV7281A, and ADV7282A devices automatically enter free run mode if the input signal cannot be decoded. The user can prevent this operation by setting DEF_VAL_AUTO_EN to 0. When the DEF_VAL_AUTO_EN bit is set to 0, the ADV7280A, ADV7281A, and ADV7282A devices output noise if it cannot decode the input video. It is recommended that the user keep DEF_VAL_AUTO_EN set to 1.

The user can force free run mode by setting the DEF_VAL_EN bit to 1. The free run feature can be a useful tool in debugging system level issues.

The VID_SEL[3:0] bits can force the video standard output in free run mode (see the Video Standard Selection section).

The user can also specify which data is output in free run mode with the FREE_RUN_PAT_SEL[2:0] bits. The following test patterns can be set using this function:

- Single color
- Color bars
- Luma ramp
- Boundary box

Single Color Test Pattern

In this mode, the ADV7280A, ADV7281A, and ADV7282A devices can be set to output the default luma and chroma data stored in the DEF_Y[5:0] and DEF_C[7:0] controls (see the Color Controls section).

Color Bars Test Pattern

In this mode, the ADV7280A, ADV7281A, and ADV7282A devices output the 100% color bars pattern.

Luma Ramp Test Pattern

In this mode, the ADV7280A, ADV7281A, and ADV7282A devices output a series of vertical bars. Each vertical bar is progressively brighter than the vertical bar to its left.

Boundary Box Test Pattern

In this mode, the ADV7280A, ADV7281A, and ADV7282A devices output a black screen with a one-pixel depth white border (see Figure 10).

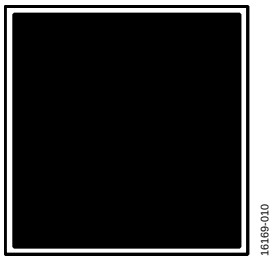

Figure 10. Boundary Box Free Run Test Pattern

DEF_VAL_AUTO_EN, Address 0x0C, Bit 1, User Sub Map

The default value automatic enable bit enables the ADV7280A, ADV7281A, and ADV7282A devices to enter free run mode if the devices cannot decode the video signal that is input.

Table 33. DEF_VAL_AUTO_EN Function

Setting	Description
0	The ADV7280A, ADV7281A, and ADV7282A devices output noise if the devices loses lock with the inputted video signal.
1 (default)	The ADV7280A, ADV7281A, and ADV7282A devices enter free run mode if the devices loses lock with the inputted video signal.

DEF_VAL_EN, Address 0x0C, Bit 0, User Sub Map

The default value enable bit forces free run mode.

Table 34. DEF_VAL_EN Function

Setting	Description
0 (default)	Do not force free run mode (that is, free run mode dependent on DEF_VAL_AUTO_EN)
1	Force free run mode

FREE_RUN_PAT_SEL[2:0] Address 0x14, Bits[2:0], User Sub Map

The free run pattern select bit selects what data is output in free run mode.

Table 35. FREE_FUN_PAT_SEL[2:0] Function

Setting	Description
000 (default)	Single color set by DEF_C[7:0] and DEF_Y[5:0] controls; see the Color Controls section
001	100% color bars
010	Luma ramp. To display properly, set the DEF_C[7:0] register to 0x88; see the Color Controls section
101	Boundary box

CLAMP OPERATION

The input video is ac-coupled into the ADV7280A, ADV7281A, and ADV7282A devices, which has the advantage of protecting the devices from STB events. However, the dc value of the input video must be restored. This process is referred to as clamping the video. This section explains the general process of clamping on the ADV7280A, ADV7281A, and ADV7282A devices in both single-ended and differential modes. This section also shows the different ways in which a user can configure clamp operation behavior.

Single-Ended CVBS Clamp Operation

The ADV7280A, ADV7281A, and ADV7282A devices use a combination of current sources and a digital processing block for clamping, as shown in Figure 11.

The analog processing channel shown is replicated three times inside the integrated circuit (IC). Whereas only a single channel is needed for a single-ended CVBS signal, two independent channels are needed for Y/C (S-VHS format) type signals, and three independent channels are needed to allow component signals (YPrPb) to be processed.

The clamping can be divided into two sections.

- Clamping before the ADC (analog domain): current sources and voltage sources.
- Clamping after the ADC (digital domain): digital processing block.

The analog clamping circuit ensures the video signal stays within the valid 1.0 V ADC input window so the analog-to-digital conversion can take place. The current sources in the AFE correct the dc level of the ac-coupled input video signal before it is fed into the ADC. The digitized data from the ADC is then fed into the video processor. The digital fine clamp block within the video processor corrects for any remaining variation in the dc level. The video processor also sends clamp control signals to the current sources. This feedback loop fine tunes the current clamp operation and compensates for any noise on the input video signal. This feedback loop maintains the dc level of the video signal during normal operation.

Differential CVBS Clamping Operation

This section applies to the ADV7281A-M, ADV7282A, and ADV7282A-M models only.

The differential clamping operation works in a similar manner to the single-ended clamping operation (see the Single-Ended CVBS Clamp Operation section). In differential mode, a coarse clamp pulls the positive and negative video input to a common-mode voltage level (V_{CML}) (see Figure 12). The feedback loop between the current clamps and the video processor fine tunes this coarse dc offset and makes the clamping robust to noise on the video input. The current clamps are controlled within a feedback loop between the AFE and the video processor; the coarse clamps are not.

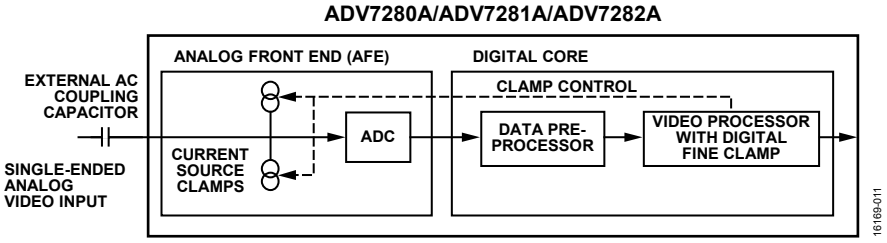

Figure 11. Single-Ended Clamping Overview

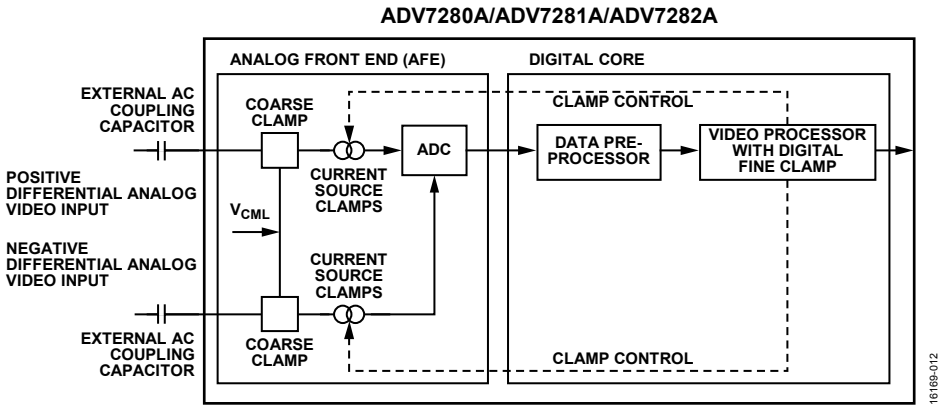

Figure 12. Differential Clamping Overview

Clamp Operation Controls

The following sections describe the I²C signals that can influence the behavior of the clamping block.

CCLEN, Address 0x14, Bit 4, User Sub Map

The current clamp enable bit allows the user to switch off all the current sources in the AFE simultaneously. Disabling the current source can be useful if the incoming analog video signal is clamped externally.

When CCLEN is set to 0, the current sources are switched off.

When CCLEN is set to 1 (default), the current sources are enabled.

DCT[1:0], Address 0x15, Bits[6:5], User Sub Map

The clamp timing bits determines the time constant of the digital fine clamp circuitry. Note that the digital fine clamp reacts quickly because it immediately corrects any residual dc level error for the active line. The time constant from the digital fine clamp must be much quicker than the one from the analog blocks.

By default, the time constant of the digital fine clamp is adjusted dynamically to suit the currently connected input signal.

Table 36. DCT[1:0] Function

Setting	Description
00 (default)	Slow (time constant (TC) = 1 sec)
01	Medium (TC = 0.5 sec)
10	Fast (TC = 0.1 sec)
11	Determined by ADV7280A, ADV7281A, and ADV7282A devices, depending on the input video parameters

DCFE, Address 0x15, Bit 4, User Sub Map

This bit allows users to freeze the digital clamp loop at any time (self clamping). Users can disable the current sources for analog clamping via the appropriate register bits, wait until the digital clamp loop settles, and then freeze it via the DCFE bit.

When DCFE is set to 0 (default), the digital clamp is operational.

When DCFE is set to 1, the digital clamp loop is frozen.

LUMA FILTER

Data from the digital fine clamp block is processed by the three sets of filters that follow. The data format at this point is CVBS for a CVBS input or luma only for Y/C and YPrPb input formats. The following describes the filters:

- Luma antialias filter (YAA). The ADV7280A, ADV7281A, and ADV7282A devices receive video based on an crystal (XTAL) frequency of 28.6363 MHz. In the case of 4× oversampled video, the ADC samples at 57.27 MHz, and the first decimation is performed inside the data preprocessor (DPP) filters. This decimation provides video data at the correct rate to the digital core.
  The ITU-R BT.601 standard recommends a sampling frequency of 13.5 MHz. The luma antialias filter decimates the oversampled video using a high quality linear phase, low-pass filter that preserves the luma signal while, at the same time, attenuating out of band components. The luma antialias filter (YAA) has a fixed response.
- Luma shaping filters (YSH). The shaping filter block is a programmable low-pass filter with a wide variety of responses. It can reduce selectively the luma video signal bandwidth (needed prior to scaling, for example). For some video sources that contain high frequency noise, reducing the bandwidth of the luma signal improves visual picture quality. If the video is compressed subsequent to the ADV7280A, ADV7281A, and ADV7282A, low-pass filtering can improve the effectiveness of the compression
  The ADV7280A, ADV7281A, and ADV7282A devices have two responses for the shaping filter: one that is used for good quality composite, component, and SVHS type sources, and a second for nonstandard CVBS signals.
  The YSH filter responses also include a set of notches for PAL and NTSC. However, using the comb filters for Y/C separation is recommended.
- Digital resampling filter. This block allows dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is chosen by the system with no requirement for user intervention.

Figure 14 through Figure 17 show the overall response of all filters together. Unless otherwise noted, the filters are set into a typical wideband mode.

Y Shaping Filter

For input signals in CVBS format, the luma shaping filters are essential in removing the chroma component from a composite signal. Y/C separation must aim for the best possible crosstalk reduction while still retaining as much bandwidth (especially on the luma component) as possible. High quality Y/C separation can be achieved by using the internal comb filters of the ADV7280A, ADV7281A, and ADV7282A devices. Comb filtering, however, relies on the frequency relationship of the luma component (multiples of the video line rate) and the color subcarrier frequency. For good quality CVBS signals, this relationship is known; the comb filter algorithms can separate luma and chroma with high accuracy.

In the case of nonstandard video signals, the frequency relationship can be disturbed, and the comb filters may not be able to remove all crosstalk artifacts without the assistance of the shaping filter block.

An automatic mode is provided that allows the ADV7280A, ADV7281A, and ADV7282A devices to evaluate the quality of the incoming video signal and select the filter responses in accordance with the signal quality and video standard. The YSFM[4:0], WYSFMOVR, and WYSFM[4:0] bits allow the user to manually override the automatic decisions in part or in full.

The luma shaping filter has the following control bits.

- YSFM[4:0] allows the user to manually select a shaping filter mode (applied to all video signals) or to enable an automatic selection (depending on video quality and video standard).
- WYSFMOVR allows the user to manually override the WYSFM[4:0] decision.
- WYSFM[4:0] allows the user to select a different shaping filter mode for good quality composite (CVBS), component (YPrPb), and SVHS (Y/C) input signals.

In automatic mode, the system preserves the maximum possible bandwidth for stable CVBS sources (because they can be combed) as well as for luma components of YPrPb and Y/C sources (because they do not need to be combed). For less stable CVBS sources (for example, VCRs), the system selects from a set of proprietary shaping filter responses that complements comb filter operation to reduce visual artifacts.

The decisions of the control logic are shown in Figure 13.

YSFM[4:0], Address 0x17, Bits[4:0], User Sub Map

The Y shaping filter mode bits allow the user to select from a wide range of low-pass and notch filters. When switched in automatic mode, the filter selection is based on other register selections, such as detected video standard, as well as properties extracted from the incoming video itself, such as quality and time base stability. The automatic selection always selects the widest possible bandwidth for the video input encountered (see Table 37).

The Y shaping filter mode operates as follows:

- If the YSFM[4:0] settings specify a filter (that is, YSFM[4:0] is set to values other than 00000, 00001, or 11111 (reserved)), the chosen filter is applied to all video, regardless of its quality.
- In automatic selection mode, use the notch filters for less stable video sources. For all other video signals, use wideband filters.

Table 37. YSFM[4:0] Function

Setting	Description
00000	Automatic selection including a wide notch response (PAL/NTSC/SECAM)
00001 (default)	Automatic selection including a narrow notch response (PAL/NTSC/SECAM)
00010	SVHS 1
00011	SVHS 2
00100	SVHS 3
00101	SVHS 4
00110	SVHS 5
00111	SVHS 6
01000	SVHS 7
01001	SVHS 8
01010	SVHS 9
01011	SVHS 10
01100	SVHS 11
01101	SVHS 12
01110	SVHS 13
01111	SVHS 14
10000	SVHS 15
10001	SVHS 16
10010	SVHS 17
10011	SVHS 18 (CCIR 601) (default)
10100	PAL NN1
10101	PAL NN2
10110	PAL NN3
10111	PAL WN1
11000	PAL WN2
11001	NTSC NN1
11010	NTSC NN2
11011	NTSC NN3
11100	NTSC WN1
11101	NTSC WN2
11110	NTSC WN3
11111	Reserved

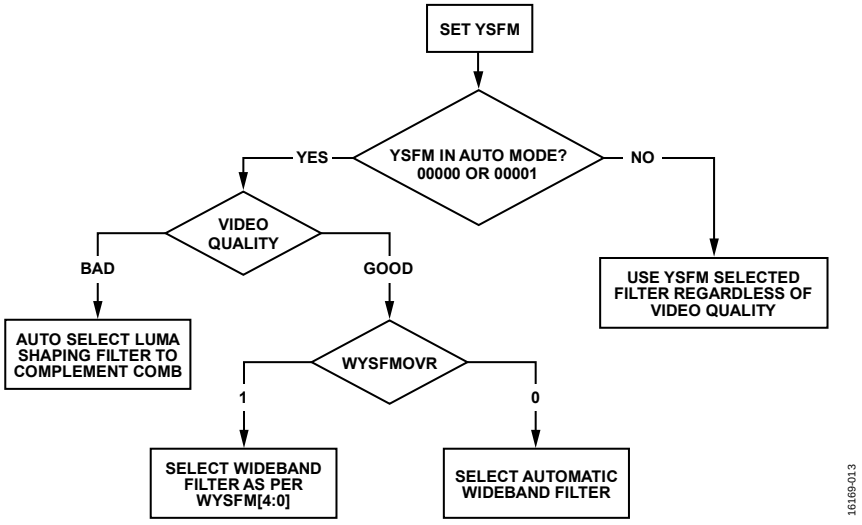

Figure 13. YSFM[4:0] and WYSFM[4:0] Control Flowchart

WYSFMOVR, Address 0x18, Bit 7, User Sub Map

Setting the Wideband Y Shaping Filter Override (WYSFMOVR) bit enables the use of the WYSFM[4:0] settings for good quality video signals. For more information on luma shaping filters, see the Y Shaping Filter section and the flowchart shown in Figure 13.

When WYSFMOVR is set to 0, the shaping filter for good quality video signals is selected automatically.

When WYSFMOVR is set to 1 (default), it enables manual override via WYSFM[4:0].

WYSFM[4:0], Wideband Y Shaping Filter Mode, Address 0x18[4:0]

The WYSFM[4:0] bits allow the user to manually select a shaping filter for good quality video signals, such as CVBS with stable time base, luma component of YPrPb, and luma component of Y/C. The WYSFM[4:0] bits are active only if the WYSFMOVR bit is set to 1. See the general discussion of the shaping filter settings in the Y Shaping Filter section.

Table 38. WYSFM[4:0] Function

WYSFM[4:0]	Description
00000	Reserved, do not use
00001	Reserved, do not use
00010	SVHS 1
00011	SVHS 2
00100	SVHS 3
00101	SVHS 4
00110	SVHS 5
00111	SVHS 6
01000	SVHS 7
01001	SVHS 8
01010	SVHS 9
01011	SVHS 10
01100	SVHS 11
s01101	SVHS 12
01110	SVHS 13
01111	SVHS 14
10000	SVHS 15
10001	SVHS 16
10010	SVHS 17
10011 (default)	SVHS 18 (CCIR 601) (default)
10100 to 11111	Reserved, do not use

Figure 14 shows the S-VHS 1 (narrowest) to S-VHS 18 (widest) shaping filter settings. Figure 15 shows the CCIR mode shaping filter response. Figure 16 shows the PAL notch filter responses. The NTSC notch filter responses are shown in Figure 17.

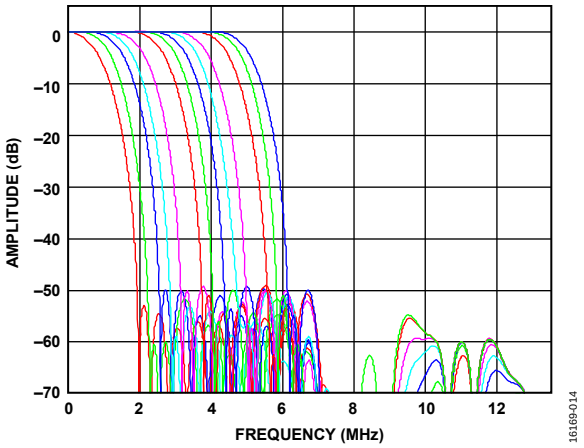

Figure 14. Combined Y Antialias, S-VHS Low-Pass Filter, and Y Resample Responses

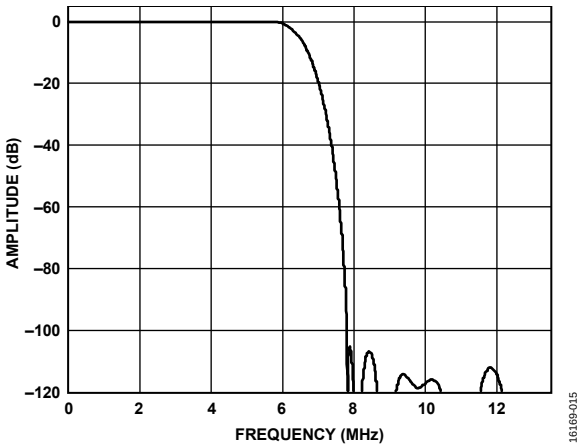

Figure 15. Combined Y Antialias, CCIR Mode Shaping Filter, Y Resample Responses

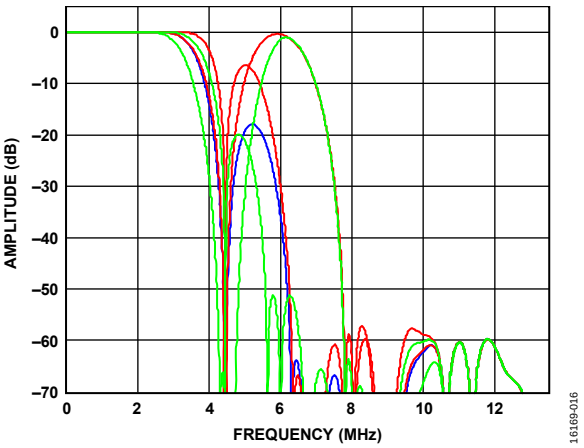

Figure 16. Combined Y Antialias, PAL Notch Filters, and Y Resample Responses

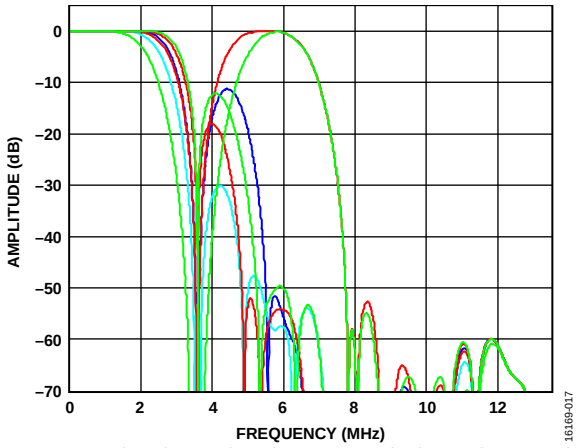

Figure 17. Combined Y Antialias Filter, NTSC Notch Filter, and Y Resample

CHROMA FILTER

Data from the digital fine clamp block is processed by the three sets of filters that follow. The data format at this point is CVBS for CVBS (or differential CVBS) inputs, chroma only for Y/C, or U/V interleaved for YPrPb input formats.

- Chroma antialias (CAA) filter. The ADV7280A, ADV7281A, and ADV7282A devices oversample the CVBS by a factor of 4 and the chroma/YPrPb by a factor of 2. A decimating filter (CAA) preserves the active video band and removes any out of band components. The CAA filter has a fixed response.
- Chroma shaping (CSH) filters. The CSH filter block can be programmed to perform a variety of low-pass filter responses. The CSH filter block can selectively reduce the bandwidth of the chroma signal for scaling or compression.
- Digital resampling filter. This block allows dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is chosen by the system without user intervention.

Figure 18 shows the overall response of all filters together.

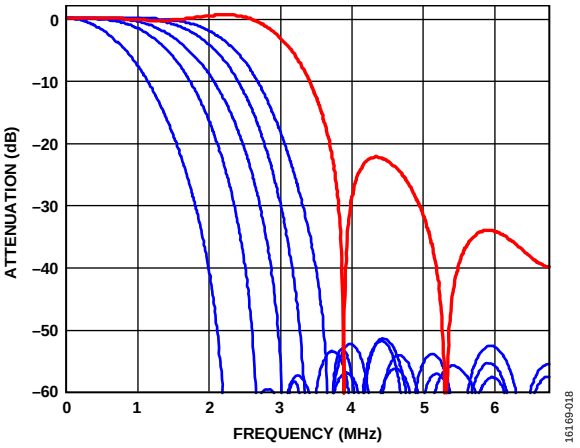

Figure 18. Chroma Shaping Filter Responses; Combined C Antialias, C Shaping Filter, and C Resampler

CSFM[2:0], Address 0x17, Bits[7:5], User Sub Map

The C shaping filter mode bits allow the user to select from a range of low-pass filters for the chrominance signal. When switched in automatic mode, the widest filter is selected based on the video standard/format and user choice (see the 000 and 001 settings in Table 39).

Table 39. CSFM[2:0] Function

Setting	Description
000 (default)	Autoselection 1.5 MHz bandwidth
001	Autoselection 2.17 MHz bandwidth
010	SH1
011	SH2
100	SH3
101	SH4
110	SH5
111	Wideband mode

Figure 18 shows the responses of SH1 (narrowest) to SH5 (widest) in addition to the wideband mode.

GAIN OPERATION

The gain control within the ADV7280A, ADV7281A, and ADV7282A devices is implemented on a purely digital basis. The input ADC supports a 10-bit range mapped into a 1.0 V analog voltage range. Gain correction takes place after the digitization in the form of a digital multiplier.

Advantages of this architecture over the commonly used programmable gain amplifier (PGA) before the ADC include the fact that the gain is completely independent of supply, temperature, and process variations.

As shown in Figure 21, the ADV7280A, ADV7281A, and ADV7282A devices can decode a video signal as long as it fits into the ADC window. The primary components that determine whether the video signal fits inside the ADC window are the amplitude of the input signal and the dc level it resides on. The dc level is set by the clamping circuitry (see the Clamp Operation section).

If the amplitude of the analog video signal is too high, clipping may occur, resulting in visual artifacts. The analog input range of the ADC, together with the clamp level, determines the maximum supported amplitude of the video signal.

Figure 19 and Figure 20 show the typical voltage divider networks required to keep the input video signal within the allowed range of the ADC, 0 V to 1 V. Place the circuit in Figure 19 before all the single-ended analog inputs to the ADV7280A, ADV7281A, and ADV7282A devices, and place the circuit in Figure 20 before all the differential inputs to the devices.

Differential inputs can only be applied directly to the ADV7281A-M, ADV7282A and ADV7282A-M models.

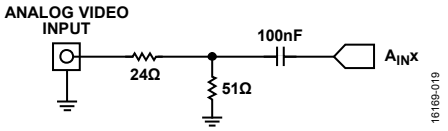

Figure 19. Single-Ended Input Voltage Divider Network

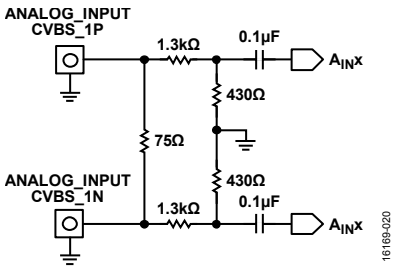

Figure 20. Differential Input Voltage Divider Network

The minimum supported amplitude of the input video is determined by the ability of the ADV7280A, ADV7281A, and ADV7282A devices to retrieve horizontal and vertical timing and to lock to the color burst, if present.

There are separate gain control units for luma and chroma data. Both can operate independently of each other. The chroma unit, however, can also take its gain value from the luma path.

The possible AGC modes are shown in Table 40.

Table 40. AGC Modes

Input Video Type	Luma Gain	Chroma Gain
Any	Manual gain luma	Manual gain chroma
CVBS	Dependent on horizontal sync depth	Dependent on color burst amplitude taken from luma path
	Peak white	Dependent on color burst amplitude taken from luma path
Y/C	Dependent on horizontal sync depth	Dependent on color burst amplitude taken from luma path
	Peak white	Dependent on color burst amplitude
YPrPb	Dependent on horizontal sync depth	Taken from luma path

It is possible to freeze the automatic gain control loops, causing the loops to stop updating and the AGC determined gain at the time of the freeze to stay active until the loop is either unfrozen or the gain mode of operation is changed.

The currently active gain from any of the modes can be read back. Refer to the description of the dual-function manual gain bits, LG[11:8] luma gain and CG[11:0] chroma gain, in the Luma Gain section and the Chroma Gain section, respectively.

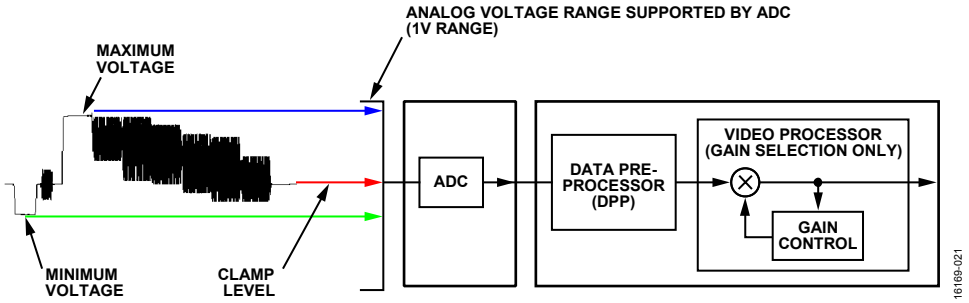

Figure 21. Gain Control Overview

Luma Gain

LAGC[2:0], Address 0x2C, Bits[6:4], User Sub Map

The luma automatic gain control mode bits select the operating mode for the gain control in the luma path.

The peak white algorithm detects if the input video amplitude exceeds the ADC input range of the ADV7280A, ADV7281A, and ADV7282A devices. If the amplitude exceeds the input range, then the devices reduce the internal luma gain to prevent the signal from becoming saturated.

Table 41. LAGC[2:0] Function

Setting	Description
000	Manual fixed gain (use LMG[11:8])
001	AGC, peak white algorithm off (blank level to sync tip)
010 (default)	AGC, peak white algorithm on (blank level to sync tip)
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Freeze gain

LAGT[1:0], Address 0x2F, Bits[7:6], User Sub Map

The luma automatic gain timing bits allows the user to influence the tracking speed of the luminance automatic gain control. This register has an effect only if the LAGC[2:0] register is set to 001 or 010 (automatic gain control modes).

If peak white AGC is enabled and active (see the Status 1, Address 0x10, Bits[7:0] section), the actual gain update speed is dictated by the peak white AGC loop and, as a result, the LAGT[1:0] settings have no effect. As soon as the device leaves peak white AGC, LAGT[1:0] becomes relevant again.

The update speed for the peak white algorithm can be customized by the use of internal parameters.

Table 42. LAGT[1:0] Function

Setting	Description
00	Slow (time constant = 2 sec)
01	Medium (time constant = 1 sec)
10	Fast (time constant = 0.2 sec)
11 (default)	Adaptive

PW_UPD, Address 0x2B, Bit 0, User Sub Map

The peak white and average video algorithms determine the gain based on measurements taken from the active video. The PW_UPD bit determines the rate of gain change. LAGC[2:0] must be set to the appropriate mode to enable the peak white or average video mode in the first place. For more information, see the LAGC[2:0], Address 0x2C, Bits[6:4] section.

Setting PW_UPD to 0 updates the gain once per video line.

Setting PW_UPD to 1 (default) updates the gain once per field.

LMG[11:8]/LG[11:8], Address 0x2F, Bits[3:0], and LMG[7:0]/LG[7:0]Address 0x30, Bits[7:0], User Sub Map

Luma gain (Bits[11:0]) is a dual-function register. If all of these bits are written to, a desired manual luma gain can be programmed. This gain becomes active if the LAGC[2:0] mode is switched to manual fixed gain. Equation 1 shows how to calculate a desired gain.

If read back, this register returns the current gain value. Depending on the setting in the LAGC[2:0] bits, the value is one of the following:

- Luma manual gain value (LAGC[2:0] set to luma manual gain mode)
- Luma automatic gain value (LAGC[2:0] set to either of the automatic modes)

Table 43. LG/LMG Function

Setting[1]	Read/Write	Description
LMG[11:0] = X	Write	Manual gain for luma path
LG[11:0] = X	Read	Actual used gain

[1] X means don't care.

$$Luma\ Gain \cong \frac{LMG[11{:}8]_{Decimal}}{Luma\ Calibration\ Factor} \quad (1)$$

where:
LMG[11:8] is a decimal value between 1024 and 4095.
Decimal informs the user to use the decimal values instead of the hexidecimal or binary values.

Calculation of the Luma Calibration Factor

1. Using a video source, set the content to a gray field and apply a standard CVBS signal to the CVBS input of the ADV7280A, ADV7281A, and ADV7282A devices.
2. Using an oscilloscope, measure the signal at the CVBS input to ensure that its sync depth, color burst, and luma are at the standard levels.
3. Connect the output of the ADV7280A, ADV7281A, and ADV7282A devices to a backend system that has unity gain and monitor the output voltage.
4. Measure the luma level correctly from the black level. Turn off the luma AGC and manually change the value of the luma manual gain control register, LMG[11:8], until the output luma level matches the input measured in Step 2.

This value, in decimal, is the luma calibration factor.

Chroma Gain

CAGC[1:0], Address 0x2C, Bits[1:0], User Sub Map

The two bits of the color automatic gain control mode select the basic mode of operation for the automatic gain control in the chroma path.

Table 44. CAGC[1:0] Function

Setting	Description
00	Manual fixed gain (use CMG[11:0])
01	Use luma gain for chroma
10 (default)	Automatic gain (based on color burst)
11	Freeze chroma gain

CAGT[1:0], Address 0x2D, Bits[7:6], User Sub Map

The chroma automatic gain timing bits allows the user to influence the tracking speed of the chroma automatic gain control. These bits an effect only if the CAGC[1:0] bits are set to 10 (automatic gain).

Table 45. CAGT[1:0] Function

CAGT[1:0]	Description
00	Slow (time constant = 2 sec)
01	Medium (time constant = 1 sec)
10	Reserved
11 (default)	Adaptive

CMG[11:8]/CG[11:8], Address 0x2D, Bits[3:0], and CMG[7:0]/CG[7:0] Address 0x2E, Bits[7:0], User Sub Map

Chroma gain (Bits[11:0]) is a dual-function register. If written to, a desired manual chroma gain can be programmed. This gain becomes active if the CAGC[1:0] function is switched to manual fixed gain. See Equation 2 for calculating a desired gain.

If read back, this register returns the current gain value. Depending on the setting in the CAGC[1:0] bits, this is either

- The chroma manual gain value (CAGC[1:0] set to chroma manual gain mode).
- The chroma automatic gain value (CAGC[1:0] set to either of the automatic modes).

Table 46. CMG/CG Function

Setting	Read/Write	Description
CMG[11:0]	Write	Manual gain for chroma path
CG[11:0]	Read	Currently active gain

$$Chroma\ Gain \cong \frac{CMG[11:0]_{Decimal}}{Chroma\ Calibration\ Factor} \quad (2)$$

where *Chroma Calibration Factor* is a decimal value between 0 and 4095.

Take the following steps to calculate the chroma calibration factor:

1. Apply a CVBS signal with the color bars/Society of Motion Picture and Television Engineers (SMPTE) bars test pattern content directly to measurement equipment, for example, an oscilloscope.
2. Ensure correct termination of 75 Ω on the measurement equipment. Measure chroma output levels.
3. Reconnect the source to the CVBS input of the ADV7280A, ADV7281A, and ADV7282A devices that has a back-end gain of 1. Repeat the measurement of chroma levels.
4. Turn off the chroma AGC, and manually change the chroma gain control register, CMG[11:0], until the chroma level matches that measured directly from the source.

This value, in decimal, is the chroma calibration factor.

CKE, Address 0x2B, Bit 6, User Sub Map

The color kill enable bit allows the optional color kill function to be switched on or off.

For quadrature amplitude modulation (QAM)-based video standards (PAL and NTSC), as well as frequency modulation (FM)-based systems (SECAM), the threshold for the color kill decision is selectable via the CKILLTHR[2:0] bits.

If color kill is enabled and the color carrier of the incoming video signal is less than the threshold for 128 consecutive video lines, color processing is switched off (black and white output). To switch the color processing back on, another 128 consecutive lines with a color burst greater than the threshold are required.

The color kill option works only for input signals with a modulated chroma part. For component input (YPrPb), there is no color kill.

Set CKE to 0 to disable color kill.

Set CKE to 1 (default) to enable color kill.

CKILLTHR[2:0], Address 0x3D, Bits[6:4], User Sub Map

The CKILLTHR[2:0] bits allow the user to select a threshold for the color kill function. The threshold applies only to QAM-based (NTSC and PAL) or FM-based (SECAM) video standards.

To enable the color kill function, the CKE bit must be set. For the 000, 001, 010, and 011 settings, chroma demodulation inside the ADV7280A, ADV7281A, and ADV7282A devices may not work satisfactorily for unstable CVBS sources.

Table 47. CKILLTHR[2:0] Function

	Description	
Setting	NTSC, PAL	SECAM
000	Kill at <0.5%	No color kill
001	Kill at <1.5%	Kill at <5%
010 (default)	Kill at <2.5%	Kill at <7%
011	Kill at <4%	Kill at <8%
100	Kill at <8.5%	Kill at <9.5%
101	Kill at <16%	Kill at <15%
110	Kill at <32%	Kill at <32%
111	Reserved	Reserved

CTI

The signal bandwidth allocated for chroma is typically much smaller than for luminance.

The uneven bandwidth, however, can lead to visual artifacts in sharp color transitions. At the border of two bars of color, both components (luma and chroma) change at the same time (see Figure 22). Due to the higher bandwidth, the signal transition of the luma component is usually much sharper than the chroma component signal transition. The color edge is not sharp, and in the worst case, it can be blurred over several pixels.

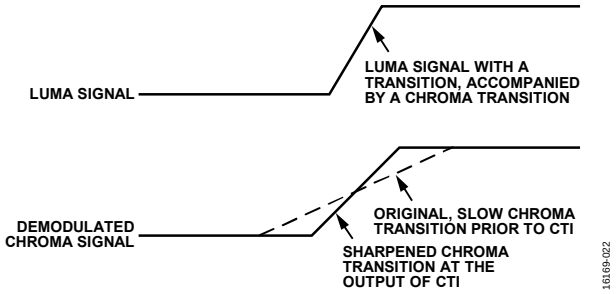

Figure 22. CTI Luma and Chroma Transition

The chroma transient improvement block examines the input video data. It detects transitions of chroma and can be programmed to create steeper chroma edges in an attempt to artificially restore lost color bandwidth. The CTI block, however, operates only on edges above a certain threshold to ensure noise is not emphasized. Ensure that edge ringing and undesirable saturation or hue distortion are avoided.

Chroma transient improvements are needed primarily for signals that have severe chroma bandwidth limitations. For those types of signals, it is strongly recommended to enable the CTI block via CTI_EN.

CTI_EN, Address 0x4D, Bit 0, User Sub Map

Set CTI_EN to 0 to disable the CTI block.

Set CTI_EN to 1 (default) to enable the CTI block.

CTI_AB_EN, Address 0x4D, Bit 1, User Sub Map

The CTI_AB_EN bit enables an alpha blend function within the CTI block. If set to 1, the alpha blender mixes the transient improved chroma with the original signal. The sharpness of the alpha blending can be configured via the CTI_AB[1:0] bits.

For the alpha blender to be active, enable the CTI block via the CTI_EN bit.

Set CTI_AB_EN to 0 to disable the CTI alpha blender.

Set CTI_AB_EN to 1 (default) to enable the CTI alpha blend mixing function.

CTI_AB[1:0], Address 0x4D, Bits[3:2], User Sub Map

The CTI_AB[1:0] controls the behavior of alpha blend circuitry that mixes the sharpened chroma signal with the original one and controls the visual impact of CTI on the output data.

For CTI_AB[1:0] to become active, the CTI block must be enabled via the CTI_EN bit, and the alpha blender must be switched on via CTI_AB_EN.

Sharp blending maximizes the effect of CTI on the picture; however, it may also increase the visual impact of small amplitude, high frequency chroma noise.

Table 48. CTI_AB[1:0] Function

Setting	Description
00	Sharpest mixing between sharpened and original chroma signal
01	Sharp mixing between sharpened and original chroma signal
10	Smooth mixing between sharpened and original chroma signal
11 (default)	Smoothest mixing between sharpened and original chroma signal

CTI_C_TH[7:0], Address 0x4E[7:0], User Sub Map

The CTI_C_TH[7:0] value is an unsigned, 8-bit number specifying the amplitude step size in a chroma transition, steepened by the CTI block. Programming a small value into this register causes even smaller edges to be steepened by the CTI block. Making CTI_C_TH[7:0] a large value causes the block to improve large transitions only.

The default value for CTI_C_TH[7:0] is 00001000.

DIGITAL NOISE REDUCTION (DNR) AND LUMA PEAKING FILTER

Digital noise reduction (DNR) is based on the assumption that high frequency signals with low amplitude are noise and their removal improves picture quality. The two DNR blocks in the ADV7280A, ADV7281A, and ADV7282A devices are the DNR1 block before the luma peaking filter and the DNR2 block after the luma peaking filter, as shown in Figure 23.

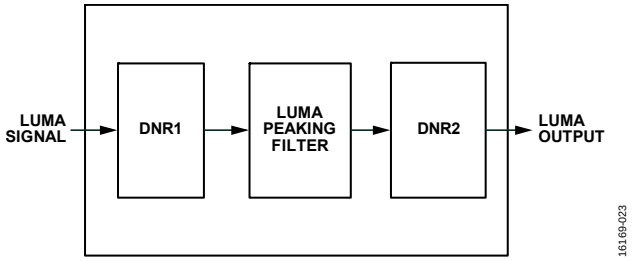

Figure 23. DNR and Peaking Block Diagram

DNR and Peaking

DNR_EN, Address 0x4D, Bit 5, User Sub Map

The DNR_EN bit enables or bypasses the DNRx blocks.

Table 49. DNR_EN Function

Setting	Description
0	Bypasses the DNRx blocks (disable)
1 (default)	Enables the DNRx blocks

DNR_TH[7:0], Address 0x50, Bits[7:0], User Sub Map

The DNR1 block is positioned before the luma peaking block. The DNR_TH[7:0] value is an unsigned, 8-bit number determines the maximum edge that is interpreted as noise and, therefore, blanked from the luma data. Programming a large value into DNR_TH[7:0] causes the DNRx blocks to interpret even large transients as noise and remove them. As a result, the effect on the video data is more visible. Programming a small value causes only small transients to be seen as noise and to be removed.

Table 50. DNR_TH[7:0] Function

Setting	Description
0x08 (default)	Threshold for maximum luma edges to be interpreted as noise

PEAKING_GAIN[7:0], Address 0xFB, Bits[7:0], User Sub Map

This filter can be manually enabled. The user can select to boost or to attenuate the midregion of the Y spectrum around 3 MHz. The peaking filter can visually improve the picture by showing more definition on the picture details that contain frequency components around 3 MHz. The default value on this register passes through the luma data unaltered. A lower value attenuates the signal, and a higher value gains the luma signal. Figure 24 shows the responses of the peaking filter.

Table 51. PEAKING_GAIN[7:0] Function

Setting	Description
0x40 (default)	Increases/decreases the gain for high frequency portions of the video signal

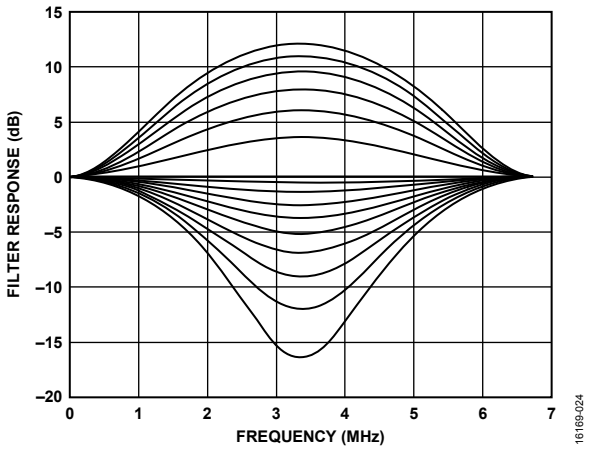

Figure 24. Peaking Filter Responses

DNR_TH2[7:0], Address 0xFC, Bits[7:0], User Sub Map

The DNR2 block is positioned after the luma peaking block and affects the gained luma signal. It operates similarly to the DNR1 block; however, there is an independent threshold control, DNR_TH2[7:0], for this block. This unsigned, 8-bit value determines the maximum edge that is interpreted as noise and blanked from the luma data. Programming a large value into DNR_TH2[7:0] causes the DNR2 block to interpret even large transients as noise and remove them. As a result, the effect on the video data is more visible. Programming a small value causes only small transients to be seen as noise and removed.

Table 52. DNR_TH2[7:0] Function

Setting	Description
0x04 (default)	Specifies the maximum luma edge that is interpreted as noise and therefore blanked

COMB FILTERS

The comb filters of the ADV7280A, ADV7281A, and ADV7282A devices can automatically handle video of all types, standards, and levels of quality. The NTSC and PAL comb filter configuration registers allow the user to customize the comb filter operation depending on which video standard is detected (by autodetection) or selected (by manual programming).

NTSC Comb Filter Settings

These settings are used for NTSC M/NTSC J CVBS inputs.

NSFSEL[1:0], Address 0x19, Bits[3:2], User Sub Map

The NSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A narrow split filter selection results in improved performance on diagonal lines but more dot crawl in the final output image. The opposite is true for selecting a wide bandwidth split filter.

Table 53. NSFSEL[1:0] Function

Setting	Description
00 (default)	Narrow
01	Medium
10	Medium
11	Wide

CTAPSN[1:0], Address 0x38, Bits[7:6], User Sub Map

CTAPSN[1:0] are the NTSC chroma comb taps bits that select how many lines the NTSC chroma comb uses in its operation.

Table 54. CTAPSN[1:0] Function

CTAPSN[1:0]	Description
00	Do not use
01	NTSC chroma comb adapts three lines to two lines
10 (default)	NTSC chroma comb adapts five lines to three lines
11	NTSC chroma comb adapts five lines to four lines

CCMN[2:0], Address 0x38, Bits[5:3], User Sub Map

CCMN[2:0] are the NTSC chroma comb mode bits that select how the NTSC chroma comb is configured.

Table 55. CCMN[2:0] Function

Setting	Description	Configuration
000 (default)	Adaptive comb mode	Three-line adaptive chroma comb for CTAPSN = 01, four-line adaptive chroma comb for CTAPSN = 10, or five-line adaptive chroma comb for CTAPSN = 11
100	Disable chroma comb	
101	Fixed chroma comb (top lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01, fixed three-line chroma comb for CTAPSN = 10, or fixed four-line chroma comb for CTAPSN = 11
110	Fixed chroma comb (all lines of line memory)	Fixed three-line chroma comb for CTAPSN = 01, fixed four-line chroma comb for CTAPSN = 10, or fixed five-line chroma comb for CTAPSN = 11
111	Fixed chroma comb (bottom lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01, fixed three-line chroma comb for CTAPSN = 10, or fixed four-line chroma comb for CTAPSN = 11

YCMN[2:0], Address 0x38, Bits[2:0], User Sub Map

NTSC luma comb mode bits.

Table 56. YCMN Function

YCMN[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Three-line adaptive, (three taps) luma comb
100	Disable luma comb	Use low-pass/notch filter; see the Y Shaping Filter section
101	Fixed luma comb (top lines of line memory)	Fixed luma comb two-line (two taps)
110	Fixed luma comb (all lines of line memory)	Fixed luma comb three-line (three taps)
111	Fixed luma comb (bottom lines of line memory)	Fixed luma comb two-line (two taps)

PAL Comb Filter Settings

These settings are used for PAL B/PAL G/PAL H/PAL I/PAL D, PAL M, PAL Combinational N, PAL 60, and NTSC 4.43 CVBS inputs.

PSFSEL[1:0], Address 0x19, Bits[1:0], User Sub Map

The PSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A wide split filter selection eliminates dot crawl but shows imperfections on diagonal lines. The opposite is true for selecting a narrow bandwidth split filter.

Table 57. PSFSEL[1:0] Function

Setting	Description
00	Narrow
01 (default)	Medium
10	Wide
11	Widest

CTAPSP[1:0], Address 0x39, Bits[7:6], User Sub Map

CTAPSP[1:0] are the PAL chroma comb taps bits that select how many lines the PAL chroma comb uses in its operation.

Table 58. CTAPSP[1:0] Function

Setting	Description
00	Do not use
01	PAL chroma comb adapts five lines (three taps) to three lines (two taps); cancels cross luma only
10	PAL chroma comb adapts five lines (five taps) to three lines (three taps); cancels cross luma and hue error less well
11 (default)	PAL chroma comb adapts five lines (five taps) to four lines (four taps); cancels cross luma and hue error well

CCMP[2:0], Address 0x39, Bits[5:3], User Sub Map

CCMP[2:0] are the PAL chroma comb mode bits that select how the PAL chroma comb is configured

Table 59. CCMP[2:0] Function

Setting	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive three-line chroma comb for CTAPSN = 01 Adaptive four-line chroma comb for CTAPSN = 10 Adaptive five-line chroma comb for CTAPSN = 11
100	Disable chroma comb	
101	Fixed chroma comb (top lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11
110	Fixed chroma comb (all lines of line memory)	Fixed three-line chroma comb for CTAPSN = 01 Fixed four-line chroma comb for CTAPSN = 10 Fixed five-line chroma comb for CTAPSN = 11
111	Fixed chroma comb (bottom lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11

YCMP[2:0], Address 0x39, Bits[2:0], User Sub Map

PAL luma comb mode bits.

Table 60. YCMP Function

Setting	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive five-line (three taps) luma comb
100	Disable luma comb	Use low-pass/notch filter; see the Y Shaping Filter section
101	Fixed luma comb (top lines of line memory)	Fixed three-line (two taps) luma comb
110	Fixed luma comb (all lines of line memory)	Fixed five-line (three taps) luma comb
111	Fixed luma comb (bottom lines of line memory)	Fixed three-line (two taps) luma comb

IF FILTER COMPENSATION

IFFILTSEL[2:0], Address 0xF8, Bits[2:0], User Sub Map

The IFFILTSEL[2:0] bits allows the user to compensate for surface acoustic wave (SAW) filter characteristics on a composite input, as observed on tuner outputs. Figure 25 and Figure 26 show intermediate frequency (IF) filter compensation for NTSC and PAL, respectively.

The options for this feature are as follows:

- Bypass mode
- NTSC, consisting of three filter characteristics
- PAL, consisting of three filter characteristics

See Table 92 for programming details.

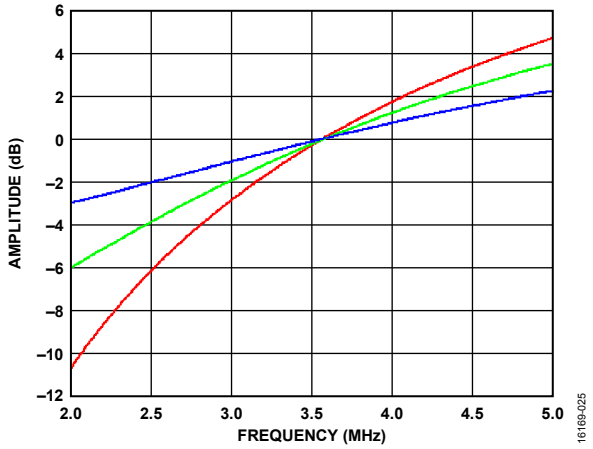

Figure 25. NTSC IF Filter Compensation (Zoomed Around f_{SC})

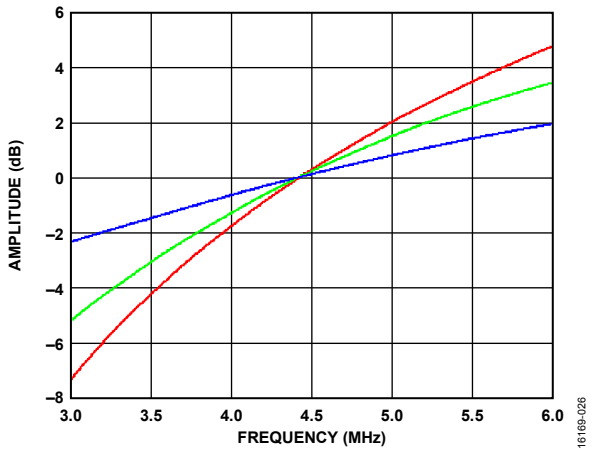

Figure 26. PAL IF Filter Compensation (Zoomed Around f_{SC})

ACE

The ADV7280A, ADV7281A, and ADV7282A devices can increase the contrast of an image depending on the content of the picture, brightening bright areas and darkening dark areas. ACE is an algorithm that automatically varies the contrast level applied across an image to enhance the picture detail visible. This automatic variation enables the contrast in the dark areas of an image to be increased without saturating the bright areas, which is useful in automotive applications where it can be important to clearly discern objects in shaded areas.

The ACE function is disabled by default. To enable the ACE function, execute the register writes shown in Table 61. To disable the ACE function, execute the register writes shown in Table 62.

The ACE feature works by sampling the chroma and luma levels in the input image. This information is then histogrammed, and the resulting correction is applied to the entire image. This correction is done in a nonlinear fashion so more correction can be applied to dark areas, if required.

For normal use, use the luma and chroma gain controls; however, in automotive applications, when dark areas may need further enhancement, use the gamma gain controls.

The reaction time of the ACE function can be set using the ACE_RESPONSE_SPEED[3:0] bits (see Table 93). The corrected image is faded over the original image using alpha blending, giving a gradual change in contrast with scene changes. The ACE_RESPONSE_SPEED[3:0] bits determine the duration of the transition from the original to the corrected image. A larger value for these bits results in a faster transition time; however, a smaller value gives more stability to rapid scene changes.

The ACE_CHROMA_MAX[3:0] bits set a maximum value that clips the chroma gain regardless of the ACE_CHROMA_GAIN[3:0] settings.

The ACE_GAMMA_GAIN[3:0] bits are useful in automotive applications because they allow dramatic image enhancement in dark regions by stretching the contrast of pixels at the low (dark) values of the image histogram. The luma and chroma gain controls are normally used; however, use the ACE_GAMMA_GAIN[3:0] bits when further stretching of the contrast in the dark areas of an image is needed.

Table 61. Register Writes to Enable the ACE Function

Register Map	Register Address	Register Write	Description
User Sub Map	0x0E	0x40	Enter User Sub Map 2
	0x80	0x80	Enable ACE
	0x0E	0x00	Reenter User Sub Map

Table 62. Register Writes to Disable the ACE Function

Register Map	Register Address	Register Write	Description
User Sub Map	0x0E	0x40	Enter User Sub Map 2
	0x80	0x00	Disable ACE
	0x0E	0x00	Reenter User Sub Map

ACE_ENABLE, Address 0x80, Bit 7, User Sub Map 2

This control enables ACE.

Table 63. ACE_ENABLE Function

Setting	Description
0 (default)	Disables ACE
1	Enables ACE

ACE_LUMA_GAIN[4:0], Address 0x83, Bits[4:0], User Sub Map 2

This is a control to set the autocontrast level for the luma channel when ACE_ENABLE is set to 1.

Table 64. ACE_LUMA_GAIN[4:0] Function

Setting	Description
00000	Sets ACE luma autocontrast level to minimum value
01101 (default)	Sets ACE luma autocontrast level to default value
11111	Sets ACE luma autocontrast level to maximum value

ACE_RESPONSE_SPEED[3:0], Address 0x85, Bits[7:4], User Sub Map 2

This control sets the reaction time of the ACE function.

Table 65. ACE_RESPONSE_SPEED[3:0] Function

Setting	Description
0000	Sets speed of ACE response to slowest value
1111 (default)	Sets speed of ACE response
1111	Sets speed of ACE response to fastest value

ACE_CHROMA_GAIN[3:0], Address 0x84, Bits[3:0], User Sub Map 2

This control sets the color saturation level for the color channels when ACE_ENABLE is set to 1.

Table 66. ACE_CHROMA_GAIN[3:0] Function

Setting	Description
0000	Sets ACE color autosaturation level to minimum value
1000 (default)	Sets ACE color autosaturation level to default value
1111	Sets ACE color autosaturation level to maximum value

ACE_CHROMA_MAX[3:0], Address 0x84, Bits[7:4], User Sub Map 2

This control sets a maximum threshold value that clips the chroma gain regardless of the ACE_CHROMA_GAIN[3:0] settings.

Table 67. ACE_CHROMA_MAX[3:0] Function

Setting	Description
4b'0000	Sets maximum threshold for ACE color autosaturation level to minimum value
1000 (default)	Sets maximum threshold for ACE color autosaturation level to default value
4b'1111	Sets maximum threshold for ACE color autosaturation level to maximum value

ACE_GAMMA_GAIN[3:0], Address 0x85[3:0] User Sub Map 2

This control provides further contrast enhancement to the luma and chroma gain controls and is particularly effective in the darker areas of an image.

Table 68. ACE_GAMMA_GAIN[3:0] Function

ACE_GAMMA_GAIN[3:0]	Description
4b'0000	Sets further contrast enhancement to minimum value
1000 (default)	Sets further contrast enhancements to default value
4b'1111	Sets further contrast enhancement to maximum value

DITHER FUNCTION

The dither function converts the digital output of the ADV7280A, ADV7281A, and ADV7282A devices from 8-bit pixel data down to 6-bit pixel data. This function makes it easier for the devices to communicate with some LCD panels. The dither function is turned off by default. It is activated by the BR_DITHER_MODE bit.

BR_DITHER_MODE, Address 0x92, Bit 0, User Sub Map 2

BR_DITHER_MODE sets whether 8-bit to 6-bit downditering is enabled or disabled. It is contained in the User Sub Map 2.

Table 69. BR_DITHER_MODE Function

BR_DITHER_MODE	Description
0 (default)	8-bit to 6-bit downdither disabled
1	8-bit to 6-bit downdither enabled

The script described in Table 70 and Table 71 explains how to enable and disable the 8-bit to 6-bit downdither function.

Table 70. Register Writes to Enable the Dither Function

Register Map	Register Address	Register Write	Description
User Sub Map	0x0E	0x40	Enter User Sub Map 2
	0x92	0x07	Enable 8-bit to 6-bit downdither
	0x0E	0x00	Reenter user sub map

Table 71. Register Writes to Disable the Dither Function

Register Map	Register Address	Register Write	Description
User Sub Map	0x0E	0x40	Enter User Sub Map 2
	0x92	0x06	Disable 8-bit to 6-bit downdither
	0x0E	0x00	Reenter user sub map

I²P FUNCTION

This section applies only to the ADV7280A, ADV7280A-M, ADV7282A, and ADV7282A-M models.

The I²P function converts an interlaced video input into a progressive video output. This function is performed without the need for external memory. Edge adaptive technology minimizes video defects on low angle lines.

The I²P function is disabled by default. To enable the I²P function, see the recommended scripts for each device at http://www.analog.com.

OUTPUT VIDEO FORMAT

All ADV7280A, ADV7281A, and ADV7282A devices (MIPI Tx or ITU-R BT.656 output models) output video data in YCbCr 4:2:2 format. The video timing is compliant with the ITU-R BT.656-3 or ITU-R BT.656-4 standards.

The following bits modify the video output of all ADV7280A, ADV7281A, and ADV7282A devices. For more output controls, see the ITU-R BT.656 Output section and MIPI CSI-2 Tx Output section.

SWAP COLOR OUTPUT

SWPC, Address 0x27, Bit 7, User Sub Map

This bit allows Cr and Cb output samples to be swapped. This bit affects the ADV7280A, ADV7280A-M, ADV7281A-M, ADV7282A, and ADV7282A-M models.

When SWPC is 0 (default), no swapping is allowed.

When SWPC is 1, the Cr and Cb output values are swapped.

OUTPUT FORMAT CONTROL

BT.656-4, Address 0x04, Bit 7, User Sub Map

The BT.656-4 bit allows the user to select an output mode compatible with the ITU-R BT.656-3 or ITU-R BT.656-4 standard.

When the BT.656-4 bit equals 0 (default), the ADV7280A, ADV7281A, and ADV7282A devices output video that is compatible with the ITU-R BT.656-3 standard.

When the BT.656-4 bit equals 1, the ADV7280A, ADV7281A, and ADV7282A devices output video that is compatible with the ITU-R BT.656-4 standard.

The BT.656-4 bit also affects the MIPI Tx active video output resolution from ADV7280A-M, ADV7281A-M, and ADV7282A-M devices. Table 72 shows all the possible active video output resolutions from the ADV7280A, ADV7280A-M, ADV7281A-M, ADV7282A, and ADV7282A-M devices.

Events such as video source disconnection or reconnection can cause the ADV7280A, ADV7281A, and ADV7282A devices to output nonstandard line lengths during the event.

Table 72. Output Resolution from the ADV7280A, ADV7281A, and ADV7282A Devices

Digital Format	Frames	Active Video Output Resolution in ITU-R BT.656-3 Mode (BT.656-4 Bit Equal to 0)	Active Video Output Resolution in ITU-R BT.656-4 Mode (BT.656-4 Bit Equal to 1)
480i	Even frames	720 × 253	720 × 243
	Odd frames	720 × 254	720 × 244
480p	Even frames	720 × 507	720 × 487
	Odd frames	720 × 507	720 × 487
576i	Even frames	720 × 288	720 × 288
	Odd frames	720 × 288	720 × 288
576p	Even frames	720 × 576	720 × 576
	Odd frames	720 × 576	720 × 576

ITU-R BT.656 OUTPUT

ITU-R BT.656 OUTPUT CONTROL REGISTERS

The following are controls for the ITU-R BT.656 output for the ADV7280A and ADV7282A devices. See the Global Control Registers section for further control registers.

Tristate Output Drivers

This section applies only to the ADV7280A model.

TOD, Address 0x03, Bit 6, User Sub Map

This bit allows the user to tristate the output drivers of the ADV7280A.

Upon setting the TOD bit, the P7 to P0, HS, and VS/FIELD/SFL pins are tristated.

The timing pins (HS and VS/FIELD/SFL pins) can be forced active via the TIM_OE bit. Note the HS and VS/FIELD/SFL pins are only available on the ADV7280A model.

When TOD is set to 0, the output drivers are enabled.

When TOD is set to 1 (default), the output drivers are tristated.

Tristate LLC Driver

This section applies only to the ADV7280A and ADV7282A models.

TRI_LLC, Address 0x1D, Bit 7, User Sub Map

This bit allows the output drivers for the LLC pin of the ADV7280A and ADV7282A models to be tristated.

When TRI_LLC is set to 0, the LLC pin drivers work according to the DR_STR_C[1:0] setting (pin enabled).

When TRI_LLC is set to 1 (default), the LLC pin drivers are tristated.

Timing Signals Output Enable

This section applies only to the ADV7280A model.

TIM_OE, Address 0x04, Bit 3, User Sub Map

The TIM_OE bit must be regarded as an addition to the TOD bit. Setting it high forces the output drivers for the HS and VS/FIELD/SFL pins into the active state (that is, driving state) even if the TOD bit is set. If TIM_OE is set to low, the HS and VS/FIELD/SFL pins are tristated depending on the TOD bit. This functionality is beneficial if the decoder is used only as a timing generator, for example, if only the timing signals are extracted from an incoming signal or if the device is in free run mode where a separate chip can output a company logo.

When TIM_OE is set to 0 (default), the HS and VS/FIELD/SFL pinsare tristated according to the TOD bit.

When TIM_OE is set to 1, the HS and VS/FIELD/SFL pins are forced active all the time.

VS/FIELD/SFL Sync Mux Selection

This section applies only to the ADV7280A model.

FLD_OUT_SEL[2:0], Address 0x6B, Bits[2:0], User Sub Map

The FLD_OUT_SEL[2:0] bits select whether the VS/FIELD/SFL pin outputs vertical sync, horizontal sync, field sync, data enable (DE), or SFL signals.

Note that the VS/FIELD/SFL pin must be active for this selection to occur. See the ITU-R BT.656 Output Control Registers section for more information.

Table 73. FLD_OUT_SEL[2:0] Function

Setting	Description
000	The VS/FIELD/SFL pin outputs horizontal sync information
001	The VS/FIELD/SFL pin outputs vertical sync information
010 (default)	The VS/FIELD/SFL pin outputs field sync information
011	The VS/FIELD/SFL pin outputs DE information
100	The VS/FIELD/SFL pin outputs SFL information.

HS Mux Selection

This section applies only to the ADV7280A model.

HS_OUT_SEL[2:0], Address 0x6A, Bits[2:0], User Sub Map

The HS_OUT_SEL[2:0] bits allow the user to change the operation of the HS pin. The HS pin is set to output horizontal sync signals as the default. The user can also set the HS pin to output vertical sync, field sync, DE, or SFL information.

Note that the HS pin must be active for this selection to occur. See the ITU-R BT.656 Output Control Registers section for more information.

Table 74. HS_OUT_SEL[2:0] Function

HS_OUT_SEL[2:0]	Description
000 (default)	The HS pin output horizontal sync information.
001	The HS pin outputs vertical sync information.
010	The HS pin outputs field sync information.
011	The HS pin outputs DE information.
100	The HS pin outputs SFL information.

Drive Strength Selection (Data)

This section applies only to the ADV7280A and ADV7282A models.

DR_STR[1:0], Address 0xF4, Bits[5:4], User Sub Map

For EMC and crosstalk reasons, it can be desirable to strengthen or weaken the drive strength of the output drivers. The DR_STR[1:0] bits affect the drive strength for the pixel output pins (P7 to P0) and the timing pins (HS and VS/FIELD/SFL). Note the HS and VS/FIELD/SFL pins are only available on the ADV7280A model.

Table 75. DR_STR[1:0] Function

Setting	Description
00	Low drive strength (1×)[1]
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

[1] The low drive strength setting is not recommended for the optimal performance of the ADV7280A and ADV7282A models.

Drive Strength Selection (Clock)

This section applies only to the ADV7280A and ADV7282A models.

DR_STR_C[1:0], Address 0xF4, Bits[3:2], User Sub Map

The DR_STR_C[1:0] bits can select the strength of the LLC clock signal output driver.

Table 76. DR_STR_C[1:0] Function

Setting	Description
00	Low drive strength (1×)[1]
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

[1] The low drive strength setting is not recommended for the optimal performance of the ADV7280A and ADV7282A models.

Enable Subcarrier Frequency Lock Pin

This section applies only to the ADV7280A model.

EN_SFL_PIN, Address 0x04, Bit 1, User Sub Map

The EN_SFL_PIN bit enables the output of subcarrier lock information (also known as genlock) from the ADV7280A core to an encoder in a decoder/encoder back to back arrangement.

When the EN_SFL_PIN is set to 0 (default), the SFL output is disabled.

When EN_SFL_PIN is set to 1, the subcarrier frequency lock information is output on the SFL pin.

Polarity LLC Pin

This section applies only to the ADV7280A and ADV7282A models.

PCLK, Address 0x37, Bit 0, User Sub Map

The polarity of the clock that exits the ADV7280A and ADV7282A models via the LLC pin can be inverted using the PCLK bit. Changing the polarity of the LLC clock output can be necessary to meet the setup and hold time expectations of subsequent devices follow on.

When PCLK is set to 0, the LLC output polarity is inverted.

When PCLK is set to 1 (default), the LLC output polarity is normal.

MIPI CSI-2 TX OUTPUT

This section applies to the ADV7280A-M, ADV7281A-M, and ADV7282A-M models only.

The decoder in theADV7280A-M, ADV7281A-M, and ADV7282A-M output an ITU-R BT.656 data stream. The ITU-R BT.656 data stream is connected into a MIPI Tx module. Data from the MIPI Tx module is fed into a D-PHY physical layer and output serially from the device.

ULTRALOW POWER STATE

The ADV7280A-M, ADV7281A-M and ADV7282A-M MIPI Tx can be programmed to enter the ultralow power state (ULPS) by the CSITX_PWRDN bit (see Table 77 and Table 96, the MIPI CSI-2 Tx Map, Address 0x00, Bit 7). In this mode, the MIPI Tx clock and data lanes transition to the low level Thevenin output voltage (V_{OL}) and do not oscillate.

Alternatively, the MIPI Tx clock and data lanes can be programmed to enter the ULPS state separately using the ESC_MODE_EN_CLK, ESC_XSHUTDOWN_CLK, ESC_MODE_EN_D0, and ESC_XSHUTDOWN_D0 bits.

Table 77. CSITX_PWRDN Function

Setting	Description
0	Power up CSI output block. The clock and data lanes output the ultralow power state exit sequence and exit the ultralow power state.
1 (default)	Power down CSI output block. The clock and data lanes output the ultralow power state entry sequence and enter ultralow power state.

ESC_MODE_EN_D0, Address 0x26, Bit 7 and ESC_XSHUTDOWN_D0, Address 0x26, Bit 6 (User Sub Map)

The MIPI Tx data lanes (D0P and D0N) can be programmed to enter and exit the ULPS using the ESC_MODE_EN_D0 and ESC_XSHUTDOWN_D0 bits.

To force the data lanes to enter the ULPS state, use the writes listed in Table 78.

Table 78. Writes to Force MIPI Tx Data Lanes (D0P and D0N) to Enter ULPS

Order of Writes	ESC_MODE_EN_D0 Setting	ESC_XSHUTDOWN_D0 Setting	Description
First write	0	0	Normal operation.
Second write	1	0	The ULPS entry sequence is transmitted and then D0P and D0N enter ULPS state. D0P and D0N go to V_{OL}.

To force the data lanes to exit the ULPS state, use the read and writes listed in Table 79.

Table 79. Reads/Writes to Force MIPI Tx Data Lanes (D0P and D0N) to Exit Ultralow ULPS

Order of Reads/ Writes	ESC_MODE_EN_D0 Setting	ESC_XSHUTDOWN_D0 Setting	Description
Read	1	0	Data lanes in ULPS state.
First write	1	1	The ULPS exit sequence is transmitted and then D0P and D0N exit ULPS state. D0P and D0N go to the high level Thevenin output voltage (V_{OH}).
Second write	0	1	Data lanes enter normal operation.
Third write	0	0	No change. Data lanes remain in normal operation.

ESC_MODE_EN_CLK, Address 0x26, Bit 5 and ESC_XSHUTDOWN_CLK, Address 0x26, Bit 4, User Sub Map

The MIPI Tx clock lanes (CLKP and CLKN) can be programmed to enter and exit the ULPS using the ESC_MODE_EN_D0 and ESC_XSHUTDOWN_D0 bits.

To force the data lanes to enter the ULPS state, use the writes listed in Table 80.

Table 80. Writes to Force MIPI Tx Clock Lanes (CLKP and CLKN) to Enter ULPS

Order of Writes	ESC_MODE_EN_CLK Setting	ESC_XSHUTDOWN_CLK Setting	Description
First write	0	0	Normal operation.
Second write	1	0	The ULPS entry sequence is transmitted and then CLKP and CLKN enter ULPS state. CLKP and CLKN go to V_{OL}.

To force the data lanes to exit the ULPS state, use the read and writes listed in Table 81.

Table 81. Reads/Writes to Force MIPI Tx Clock Lanes (CLKP and CLKN) to Exit ULPS

Order of Reads/Writes	ESC_MODE_EN_CLK Setting	ESC_XSHUTDOWN_D0 Setting	Description
Read	1	0	Clock lanes in ULPS state.
First write	1	1	The ULPS exit sequence is transmitted and then CLKP and CLKN exit ULPS state. CLKP and CLKN go to V_{OH}.
Second write	0	1	Clock lanes enter normal operation.
Third write	0	0	No change. Clock lanes remain in normal operation.

VPP_SLAVE_ADDR, Bits[6:0], Address 0xFD, Bits[7:1], User Sub Map

These bits program the I^2C address of the VPP map.

Table 82. Program VPP Register Map Address

Setting	Description
0000000 (default)	When set to this value, the VPP register map cannot be written to or read from.
1000100 (recommended)	This sets the VPP register map to a write address of 0x84 and a read address of 0x85. This is the recommended setting.

CSI_TX_SLAVE_ADDR[6:0], Address 0xFE, Bits[7:1], User Sub Map

Table 83. Program CSI_Tx Register Map Address

Setting	Description
0000000 (default)	When set to this value, the CSI_Tx register map cannot be written to or read from.
1000100 (recommended)	This sets the CSI_Tx register map to a write address of 0x88 and a read address of 0x89. This is the recommended setting.

POWER SUPPLY REQUIREMENTS

Table 84 and Table 85 show the current rating recommendations for power supply design. Use these values when designing a power supply section to ensure that an adequate current can be supplied to the ADV7280A, ADV7281A, and ADV7282A devices.

Table 84. Current Supply Design Recommendations for the ADV7280A and ADV7282A Models

Parameter	Rating (mA)
Digital I/O supply current (I_{DVDDIO})	20
Digital supply current (I_{DVDD})	110
Analog supply current (I_{AVDD})	100
Phase-locked loop supply current (I_{PVDD})	20

Table 85. Current Supply Design Recommendations for the ADV7280A-M, ADV7281A-M, and ADV7282A-M Models

Parameter	Rating (mA)
I_{DVDDIO}	5
I_{DVDD}	110
I_{AVDD}	100
I_{PVDD}	20
MIPI Tx supply current (I_{MVDD})	20

I²C REGISTER MAPS

To access all the registers listed in Table 87, SUB_USR_EN[1:0] in Register Address 0x0E must be programmed to 00. All reserved bits are left blank.

To understand the read/write modes, see Table 86.

Table 86. Register Access Conventions

Mode	Description
R/W	Memory location has read and write access.
R	Memory location is read access only. A read always returns 0 unless otherwise specified.
W	Memory location is write access only.

Table 87. User Sub Map Register Map Details

Addr	Register Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0x00	Input control	R/W				INSEL[4]	INSEL[3]	INSEL[2]	INSEL[1]	INSEL[0]	0x0E
0x01	Video Selection 1	R/W		ENHSPLL	Betacam		ENVSPROC				0xC8
0x02	Video Selection 2	R/W	VID_SEL[3]	VID_SEL[2]	VID_SEL[1]	VID_SEL[0]					0x04
0x03	Output control	R/W	VBI_EN	TOD							0x4C
0x04	Extended output control	R/W	BT.656-4				TIM_OE	BL_C_VBI	EN_SFL_PIN	Range	0x35
0x05	Reserved										
0x06	Reserved										
0x07	Autodetect enable	R/W	AD_SEC525_EN	AD_SECAM_EN	AD_N443_EN	AD_P60_EN	AD_PALN_EN	AD_PALM_EN	AD_NTSC_EN	AD_PAL_EN	0x7F
0x08	Contrast	R/W	CON[7]	CON[6]	CON[5]	CON[4]	CON[3]	CON[2]	CON[1]	CON[0]	0x80
0x09	Reserved										
0x0A	Brightness adjust	R/W	BRI[7]	BRI[6]	BRI[5]	BRI[4]	BRI[3]	BRI[2]	BRI[1]	BRI[0]	0x00
0x0B	Hue adjust	R/W	HUE[7]	HUE[6]	HUE[5]	HUE[4]	HUE[3]	HUE[2]	HUE[1]	HUE[0]	0x00
0x0C	Default Value Y	R/W	DEF_Y[5]	DEF_Y[4]	DEF_Y[3]	DEF_Y[2]	DEF_Y[1]	DEF_Y[0]	DEF_VAL_AUTO_EN	DEF_VAL_EN	0x36
0x0D	Default Value C	R/W	DEF_C[7]	DEF_C[6]	DEF_C[5]	DEF_C[4]	DEF_C[3]	DEF_C[2]	DEF_C[1]	DEF_C[0]	0x7C
0x0E	Analog Devices Control 1	R/W		SUB_USR_EN[1]	SUB_USR_EN[0]						0x00
0x0F	Power management	R/W	Reset		PWRDWN						0x20
0x10	Status 1	R	COL_KILL	AD_RESULT[2]	AD_RESULT[1]	AD_RESULT[0]	FOLLOW_PW	FSC_LOCK	LOST_LOCK	IN_LOCK	
0x11	IDENT	R	IDENT[7]	IDENT[6]	IDENT[5]	IDENT[4]	IDENT[3]	IDENT[2]	IDENT[1]	IDENT[0]	0x42
0x12	Status 2	R			FSC_NSTD	LL_NSTD	MV_AGC_DET	MV_PS_DET	MVCS_T3	MVCS_DET	
0x13	Status 3	R	PAL_SW_LOCK	Interlaced	STD_FLD_LEN	FREE_RUN_ACT	Reserved	SD_OP_50Hz	Reserved	INST_HLOCK	
0x14	Analog clamp control	R/W				CCLEN		FREE_RUN_PAT_SEL[2]	FREE_RUN_PAT_SEL[1]	FREE_RUN_PAT_SEL[0]	0x10
0x15	Digital Clamp Control 1	R/W		DCT[1]	DCT[0]	DCFE					0x00
0x16	Reserved										
0x17	Shaping Filter Control 1	R/W	CSFM[2]	CSFM[1]	CSFM[0]	YSFM[4]	YSFM[3]	YSFM[2]	YSFM[1]	YSFM[0]	0x01
0x18	Shaping Filter Control 2	R/W	WYSFMOVR			WYSFM[4]	WYSFM[3]	WYSFM[2]	WYSFM[1]	WYSFM[0]	0x93
0x19	Comb filter control	R/W					NSFSEL[1]	NSFSEL[0]	PSFSEL[1]	PSFSEL[0]	0xF1
0x1D	Analog Devices Control 2	R/W	TRI_LLC								0xC0
0x27	Pixel delay control	R/W	SWPC	AUTO_PDC_EN	CTA[2]	CTA[1]	CTA[0]		LTA[1]	LTA[0]	0x58
0x2B	Misc gain control	R/W		CKE						PW_UPD	0xE1
0x2C	AGC mode control	R/W		LAGC[2]	LAGC[1]	LAGC[0]			CAGC[1]	CAGC[0]	0xAE

Addr	Register Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0x2D	Chroma Gain Control 1	W	CAGT[1]	CAGT[0]			CMG[11]	CMG[10]	CMG[9]	CMG[8]	0xF4
0x2D	Chroma Gain 1	R					CG[11]	CG[10]	CG[9]	CG[8]	
0x2E	Chroma Gain Control 2	W	CMG[7]	CMG[6]	CMG[5]	CMG[4]	CMG[3]	CMG[2]	CMG[1]	CMG[0]	0x00
0x2E	Chroma Gain 2	R	CG[7]	CG[6]	CG[5]	CG[4]	CG[3]	CG[2]	CG[1]	CG[0]	
0x2F	Luma Gain Control 1	W	LAGT[1]	LAGT[0]			LMG[11]	LMG[10]	LMG[9]	LMG[8]	0xF0
0x2F	Luma Gain 1	R					LG[11]	LG[10]	LG[9]	LG[8]	
0x30	Luma Gain Control 2	W	LMG[7]	LMG[6]	LMG[5]	LMG[4]	LMG[3]	LMG[2]	LMG[1]	LMG[0]	0x00
0x30	Luma Gain 2	R	LG[7]	LG[6]	LG[5]	LG[4]	LG[3]	LG[2]	LG[1]	LG[0]	
0x31	VS/FIELD Control 1	R/W				NEWAVMODE	HVSTIM				0x02
0x32	VS/FIELD Control 2	R/W	VSBHO	VSBHE							0x41
0x33	VS/FIELD Control 3	R/W	VSEHO	VSEHE							0x84
0x34	HS Position Control 1	R/W		HSB[10]	HSB[9]	HSB[8]		HSE[10]	HSE[9]	HSE[8]	0x00
0x35	HS Position Control 2	R/W	HSB[7]	HSB[6]	HSB[5]	HSB[4]	HSB[3]	HSB[2]	HSB[1]	HSB[0]	0x02
0x36	HS Position Control 3	R/W	HSE[7]	HSE[6]	HSE[5]	HSE[4]	HSE[3]	HSE[2]	HSE[1]	HSE[0]	0x00
0x37	Polarity	R/W	PHS		PVS		PF			PCLK	0x09
0x38	NTSC comb control	R/W	CTAPSN[1]	CTAPSN[0]	CCMN[2]	CCMN[1]	CCMN[0]	YCMN[2]	YCMN[1]	YCMN[0]	0x80
0x39	PAL comb control	R/W	CTAPSP[1]	CTAPSP[0]	CCMP[2]	CCMP[1]	CCMP[0]	YCMP[2]	YCMP[1]	YCMP[0]	0xC0
0x3A	ADC control	R/W					PWRDWN_ MUX_0P	PWRDWN_MUX_1	PWRDWN_MUX_2	MUX_PDN_ OVERRIDE	0x00
0x3D	Manual window control	R/W		CKILLTHR[2]	CKILLTHR[1]	CKILLTHR[0]					0x22
0x41	Resample control	R/W		SFL_INV							0x01
0x4D	CTI DNR Control 1	R/W			DNR_EN		CTI_AB[1]	CTI_AB[0]	CTI_AB_EN	CTI_EN	0xEF
0x4E	CTI DNR Control 2	R/W	CTI_C_TH[7]	CTI_C_TH[6]	CTI_C_TH[5]	CTI_C_TH[4]	CTI_C_TH[3]	CTI_C_TH[2]	CTI_C_TH[1]	CTI_C_TH[0]	0x08
0x50	DNR Noise Threshold 1	R/W	DNR_TH[7]	DNR_TH[6]	DNR_TH[5]	DNR_TH[4]	DNR_TH[3]	DNR_TH[2]	DNR_TH[1]	DNR_TH[0]	0x08
0x51	Lock count	R/W	FSCLE	SRLS	COL[2]	COL[1]	COL[0]	CIL[2]	CIL[1]	CIL[0]	0x24
0x5D	DIAG1 control	R/W		DIAG1_ SLICER_ PWRDN		DIAG1_SLICE_ LEVEL[2]	DIAG1_SLICE_ LEVEL[1]	DIAG1_SLICE_ LEVEL[0]			0x6D
0x5E	DIAG2 control	R/W		DIAG2_ SLICER_ PWRDN		DIAG2_SLICE_ LEVEL[2]	DIAG2_SLICE_ LEVEL[1]	DIAG2_SLICE_ LEVEL[0]			0x6D
0x59	GPO	R/W				GPO_ENABLE		GPO[2]	GPO[1]	GPO[0]	0x00
0x60	ADC Switch 3	R/W					MUX_0N[3]	MUX_0N[2]	MUX_0N[1]	MUX_0N[0]	0x10
0x6A	Output Sync Select 1	R/W						HS_OUT_SEL[2]	HS_OUT_SEL[1]	HS_OUT_ SEL[0]	0x00
0x6B	Output Sync Select 2	R/W						FLD_OUT_SEL[2]	FLD_OUT_SEL[1]	FLD_OUT_ SEL[0]	0x12
0x8F	Free Run Line Length 1	W		LLC_PAD_ SEL[2]	LLC_PAD_ SEL[1]	LLC_PAD_ SEL[0]					0x00
0x99	CCAP1	R	CCAP1[7]	CCAP1[6]	CCAP1[5]	CCAP1[4]	CCAP1[3]	CCAP1[2]	CCAP1[1]	CCAP1[0]	
0x9A	CCAP2	R	CCAP2[7]	CCAP2[6]	CCAP2[5]	CCAP2[4]	CCAP2[3]	CCAP2[2]	CCAP2[1]	CCAP2[0]	
0x9B	Letterbox 1	R	LB_LCT[7]	LB_LCT[6]	LB_LCT[5]	LB_LCT[4]	LB_LCT[3]	LB_LCT[2]	LB_LCT[1]	LB_LCT[0]	
0x9C	Letterbox 2	R	LB_LCM[7]	LB_LCM[6]	LB_LCM[5]	LB_LCM[4]	LB_LCM[3]	LB_LCM[2]	LB_LCM[1]	LB_LCM[0]	
0x9D	Letterbox 3	R	LB_LCB[7]	LB_LCB[6]	LB_LCB[5]	LB_LCB[4]	LB_LCB[3]	LB_LCB[2]	LB_LCB[1]	LB_LCB[0]	
0xB2	CRC enable	W						CRC_ENABLE			0x1C
0xC3	ADC Switch 1	R/W	MUX_1[3]	MUX_1[2]	MUX_1[1]	MUX_1[0]	MUX_0P[3]	MUX_0P[2]	MUX_0P[1]	MUX_0P[0]	0x00
0xC4	ADC Switch 2	R/W	MAN_MUX_EN				MUX_2[3]	MUX_2[2]	MUX_2[1]	MUX_2[0]	0x00

Addr	Register Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0xDC	Letterbox Control 1	R/W				LB_TH[4]	LB_TH[3]	LB_TH[2]	LB_TH[1]	LB_TH[0]	0xAC
0xDD	Letterbox Control 2	R/W	LB_SL[3]	LB_SL[2]	LB_SL[1]	LB_SL[0]	LB_EL[3]	LB_EL[2]	LB_EL[1]	LB_EL[0]	0x4C
0xDE	ST Noise Readback 1	R					ST_NOISE_VLD	ST_NOISE[10]	ST_NOISE[9]	ST_NOISE[8]	
0xDF	ST Noise Readback 2	R	ST_NOISE[7]	ST_NOISE[6]	ST_NOISE[5]	ST_NOISE[4]	ST_NOISE[3]	ST_NOISE[2]	ST_NOISE[1]	ST_NOISE[0]	
0xE1	SD offset Cb channel	R/W	SD_OFF_Cb[7]	SD_OFF_Cb[6]	SD_OFF_Cb[5]	SD_OFF_Cb[4]	SD_OFF_Cb[3]	SD_OFF_Cb[2]	SD_OFF_Cb[1]	SD_OFF_Cb[0]	0x80
0xE2	SD offset Cr channel	R/W	SD_OFF_Cr[7]	SD_OFF_Cr[6]	SD_OFF_Cr[5]	SD_OFF_Cr[4]	SD_OFF_Cr[3]	SD_OFF_Cr[2]	SD_OFF_Cr[1]	SD_OFF_Cr[0]	0x80
0xE3	SD saturation Cb channel	R/W	SD_SAT_Cb[7]	SD_SAT_Cb[6]	SD_SAT_Cb[5]	SD_SAT_Cb[4]	SD_SAT_Cb[3]	SD_SAT_Cb[2]	SD_SAT_Cb[1]	SD_SAT_Cb[0]	0x80
0xE4	SD saturation Cr channel	R/W	SD_SAT_Cr[7]	SD_SAT_Cr[6]	SD_SAT_Cr[5]	SD_SAT_Cr[4]	SD_SAT_Cr[3]	SD_SAT_Cr[2]	SD_SAT_Cr[1]	SD_SAT_Cr[0]	0x80
0xE5	NTSC V bit begin	R/W	NVBEGDELO	NVBEGDELE	NVBEGSIGN	NVBEG[4]	NVBEG[3]	NVBEG[2]	NVBEG[1]	NVBEG[0]	0x25
0xE6	NTSC V bit end	R/W	NVENDDELO	NVENDDELE	NVENDSIGN	NVEND[4]	NVEND[3]	NVEND[2]	NVEND[1]	NVEND[0]	0x04
0xE7	NTSC F bit toggle	R/W	NFTOGDELO	NFTOGDELE	NFTOGSIGN	NFTOG[4]	NFTOG[3]	NFTOG[2]	NFTOG[1]	NFTOG[0]	0x63
0xE8	PAL V bit begin	R/W	PVBEGDELO	PVBEGDELE	PVBEGSIGN	PVBEG[4]	PVBEG[3]	PVBEG[2]	PVBEG[1]	PVBEG[0]	0x65
0xE9	PAL V bit end	R/W	PVENDDELO	PVENDDELE	PVENDSIGN	PVEND[4]	PVEND[3]	PVEND[2]	PVEND[1]	PVEND[0]	0x14
0xEA	PAL F bit toggle	R/W	PFTOGDELO	PFTOGDELE	PFTOGSIGN	PFTOG[4]	PFTOG[3]	PFTOG[2]	PFTOG[1]	PFTOG[0]	0x63
0xEB	Vblank Control 1	R/W	NVBIOLCM[1]	NVBIOLCM[0]	NVBIELCM[1]	NVBIELCM[0]	PVBIOLCM[1]	PVBIOLCM[0]	PVBIELCM[1]	PVBIELCM[0]	0x55
0xEC	Vblank Control 2	R/W	NVBIOCCM[1]	NVBIOCCM[0]	NVBIECCM[1]	NVBIECCM[0]	PVBIOCCM[1]	PVBIOCCM[0]	PVBIECCM[1]	PVBIECCM[0]	0x55
0xF3	AFE Control 1	R/W				AA_FILT_MAN_OVR	AA_FILT_EN[3]	AA_FILT_EN[2]	AA_FILT_EN[1]	AA_FILT_EN[0]	0x00
0xF4	Drive strength	R/W	GLITCH_FILT_BYP		DR_STR[1]	DR_STR[0]	DR_STR_C[1]	DR_STR_C[0]	DR_STR_S[1]	DR_STR_S[0]	0x15
0xF8	IF_COMP_CONTROL	R/W						IFFILTSEL[2]	IFFILTSEL[1]	IFFILTSEL[0]	0x00
0xF9	VS mode control	R/W					VS_COAST_MODE[1]	VS_COAST_MODE[0]	EXTEND_VS_MIN_FREQ	EXTEND_VS_MAX_FREQ	0x03
0xFB	Peaking gain	R/W	PEAKING_GAIN[7]	PEAKING_GAIN[6]	PEAKING_GAIN[5]	PEAKING_GAIN[4]	PEAKING_GAIN[3]	PEAKING_GAIN[2]	PEAKING_GAIN[1]	PEAKING_GAIN[0]	0x40
0xFC	DNR Noise Threshold 2	R/W	DNR_TH2[7]	DNR_TH2[6]	DNR_TH2[5]	DNR_TH2[4]	DNR_TH2[3]	DNR_TH2[2]	DNR_TH2[1]	DNR_TH2[0]	0x04
0xFD	VPP slave address	R/W	VPP_SLAVE_ADDR[6]	VPP_SLAVE_ADDR[5]	VPP_SLAVE_ADDR[4]	VPP_SLAVE_ADDR[3]	VPP_SLAVE_ADDR[2]	VPP_SLAVE_ADDR[1]	VPP_SLAVE_ADDR[0]		
0xFE	CSI Tx slave address	R/W	CSI_TX_SLAVE_ADDR[6]	CSI_TX_SLAVE_ADDR[5]	CSI_TX_SLAVE_ADDR[4]	CSI_TX_SLAVE_ADDR[3]	CSI_TX_SLAVE_ADDR[2]	CSI_TX_SLAVE_ADDR[1]	CSI_TX_SLAVE_ADDR[0]		0x00

To access the registers listed in Table 88, SUB_USR_EN[1:0] in Register Address 0x0E, user sub map, must be programmed to 10. All read only bits are left blank.

Table 88. User Sub Map 2 Register Map Details

Addr	Register Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0x80	ACE Control 1	R/W	ACE_ENABLE								0x00
0x83	ACE Control 4	R/W				ACE_LUMA_GAIN[4]	ACE_LUMA_GAIN[3]	ACE_LUMA_GAIN[2]	ACE_LUMA_GAIN[1]	ACE_LUMA_GAIN[0]	0x0D
0x84	ACE Control 5	R/W	ACE_CHROMA_MAX[3]	ACE_CHROMA_MAX[2]	ACE_CHROMA_MAX[1]	ACE_CHROMA_MAX[0]	ACE_CHROMA_GAIN[3]	ACE_CHROMA_GAIN[2]	ACE_CHROMA_GAIN[1]	ACE_CHROMA_GAIN[0]	0x88
0x85	ACE Control 6	R/W	ACE_RESPONSE_SPEED[3]	ACE_RESPONSE_SPEED[2]	ACE_RESPONSE_SPEED[2]	ACE_RESPONSE_SPEED[1]	ACE_GAMMA_GAIN[3]	ACE_GAMMA_GAIN[2]	ACE_GAMMA_GAIN[1]	ACE_GAMMA_GAIN[0]	0xF8
0x92	Dither control	R/W								BR_DITHER_MODE	0x00
0xD9	MIN_MAX_0	R/W	MIN_THRESH_Y[7]	MIN_THRESH_Y[6]	MIN_THRESH_Y[5]	MIN_THRESH_Y[4]	MIN_THRESH_Y[3]	MIN_THRESH_Y[2]	MIN_THRESH_Y[1]	MIN_THRESH_Y[0]	0x00

Addr	Register Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0xDA	MIN_MAX_1	R/W	MAX_THRESH_Y[7]	MAX_THRESH_Y[6]	MAX_THRESH_Y[5]	MAX_THRESH_Y[4]	MAX_THRESH_Y[3]	MAX_THRESH_Y[2]	MAX_THRESH_Y[1]	MAX_THRESH_Y[0]	0xFF
0xDB	MIN_MAX_2	R/W	MIN_THRESH_C[7]	MIN_THRESH_C[6]	MIN_THRESH_C[5]	MIN_THRESH_C[4]	MIN_THRESH_C[3]	MIN_THRESH_C[2]	MIN_THRESH_C[1]	MIN_THRESH_C[0]	0x00
0xDC	MIN_MAX_3	R/W	MAX_THRESH_C[7]	MAX_THRESH_C[6]	MAX_THRESH_C[5]	MAX_THRESH_C[4]	MAX_THRESH_C[3]	MAX_THRESH_C[2]	MAX_THRESH_C[1]	MAX_THRESH_C[0]	0xFF
0xDD	MIN_MAX_4	R/W	MIN_SAMPLES_ALLOWED_Y[3]	MIN_SAMPLES_ALLOWED_Y[2]	MIN_SAMPLES_ALLOWED_Y[1]	MIN_SAMPLES_ALLOWED_Y[0]	MAX_SAMPLES_ALLOWED_Y[3]	MAX_SAMPLES_ALLOWED_Y[2]	MAX_SAMPLES_ALLOWED_Y[1]	MAX_SAMPLES_ALLOWED_Y[0]	0xCC
0xDE	MIN_MAX_5	R/W	MIN_SAMPLES_ALLOWED_C[3]	MIN_SAMPLES_ALLOWED_C[2]	MIN_SAMPLES_ALLOWED_C[1]	MIN_SAMPLES_ALLOWED_C[0]	MAX_SAMPLES_ALLOWED_C[3]	MAX_SAMPLES_ALLOWED_C[2]	MAX_SAMPLES_ALLOWED_C[1]	MAX_SAMPLES_ALLOWED_C[0]	0xCC
0xE0	FL control	R/W								FL_ENABLE	0x00
0xE1	Y Average 0	R/W	LINE_START[8]	LINE_START[7]	LINE_START[6]	LINE_START[5]	LINE_START[4]	LINE_START[3]	LINE_START[2]	LINE_START[1]	0x11
0xE2	Y Average 1	R/W	LINE_END[8]	LINE_END[7]	LINE_END[6]	LINE_END[5]	LINE_END[4]	LINE_END[3]	LINE_END[2]	LINE_END[1]	0x88
0xE3	Y Average 2	R/W	SAMPLE_START[9]	SAMPLE_START[8]	SAMPLE_START[7]	SAMPLE_START[6]	SAMPLE_START[5]	SAMPLE_START[4]	SAMPLE_START[3]	SAMPLE_START[2]	0x1B
0xE4	Y Average 3	R/W	SAMPLE_END[9]	SAMPLE_END[8]	SAMPLE_END[7]	SAMPLE_END[6]	SAMPLE_END[5]	SAMPLE_END[4]	SAMPLE_END[3]	SAMPLE_END[2]	0xD7
0xE5	Y Average 4	R/W	SAMPLE_END[1]	SAMPLE_END[0]	SAMPLE_START[1]	SAMPLE_START[0]			LINE_END[0]	LINE_START[0]	0x23
0xE6	Y Average 5	R/W				Y_AVG_TIME_CONST[2]	Y_AVG_TIME_CONST[1]	Y_AVG_TIME_ONST[0]	Y_AVG_FILT_EN	CAPTURE_VALUE	0x10
0xE7	Y average data MSB	R	Y_AVERAGE[9]	Y_AVERAGE[8]	Y_AVERAGE[7]	Y_AVERAGE[6]	Y_AVERAGE[5]	Y_AVERAGE[4]	Y_AVERAGE[3]	Y_AVERAGE[2]	
0xE8	Y average data LSB	R							Y_AVERAGE[1]	Y_AVERAGE[0]	

To access the registers listed in Table 89, SUB_USR_EN[1:0] in Register Address 0x0E, user sub map, must be programmed to 01. All read only registers are left blank.

Table 89. Interrupt/VDP Sub Map Details

Addr	Register Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0x40	Interrupt Configuration 1	R/W	INTRQ_DUR_SEL[1]	INTRQ_DUR_SEL[0]	MV_INTRQ_SEL[1]	MV_INTRQ_SEL[0]		MPU_STIM_INTRQ	INTRQ_OP_SEL[1]	INTRQ_OP_SEL[0]	0x10
0x42	Interrupt Status 1	R		MV_PS_CS_Q	SD_FR_CHNG_Q				SD_UNLOCK_Q	SD_LOCK_Q	
0x43	Interrupt Clear 1	W		MV_PS_CS_CLR	SD_FR_CHNG_CLR				SD_UNLOCK_CLR	SD_LOCK_CLR	0x00
0x44	Interrupt Mask 1	R/W		MV_PS_CS_MSKB[1]	SD_FR_CHNG_MSKB[1]				SD_UNLOCK_MSKB[1]	SD_LOCK_MSKB[1]	0x00
0x45	Raw Status 2	R	MPU_STIM_INTRQ		CHX_MIN_MAX_INTRQ	EVEN_FIELD				CCAPD	
0x46	Interrupt Status 2	R	MPU_STIM_INTRQ_Q			SD_FIELD_CHNGD_Q				CCAPD_Q	
0x47	Interrupt Clear 2	W	MPU_STIM_INTRQ_CLR		CHX_MIN_MAX_INTRQ_CLR	SD_FIELD_CHNGD_CLR				CCAPD_CLR	0x00
0x48	Interrupt Mask 2	R/W	MPU_STIM_INTRQ_MSKB[1]		CHX_MIN_MAX_INTRQ_MSKB[1]	SD_FIELD_CHNGD_MSKB[1]				CCAPD_MSKB[1]	0x00
0x49	Raw Status 3	R				SCM_LOCK		SD_H_LOCK	SD_V_LOCK	SD_OP_50Hz	
0x4A	Interrupt Status 3	R			PAL_SW_LK_CHNG_Q	SCM_LOCK_CHNG_Q	SD_AD_CHNG_Q	SD_H_LOCK_CHNG_Q	SD_V_LOCK_CHNG_Q	SD_OP_CHNG_Q	
0x4B	Interrupt Clear 3	W			PAL_SW_LK_CHNG_CLR	SCM_LOCK_CHNG_CLR	SD_AD_CHNG_CLR	SD_H_LOCK_CHNG_CLR	SD_V_LOCK_CHNG_CLR	SD_OP_CHNG_CLR	0x00
0x4C	Interrupt Mask 3	R/W			PAL_SW_LK_CHNG_MSKB[1]	SCM_LOCK_CHNG_MSKB[1]	SD_AD_CHNG_MSKB[1]	SD_H_LOCK_CHNG_MSKB[1]	SD_V_LOCK_CHNG_MSKB[1]	SD_OP_CHNG_MSKB[1]	0x00
0x4E	Interrupt Status 4	R						VDP_CGMS_WSS_CHNGD_Q		VDP_CCAPD_Q	

Addr	Register Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0x4F	Interrupt Clear 4	W						VDP_CGMS_WSS_CHNGD_CLR		VDP_CCAPD_CLR	0x00
0x50	Interrupt Mask 4	R/W						VDP_CGMS_WSS_CHNGD_MSKB[1]		VDP_CCAPD_MSKB[1]	0x00
0x51	Interrupt Latch 0	R			Y_CHANNEL_MIN_VIOLATION	Y_CHANNEL_MAX_VIOLATION	CB_CHANNEL_MIN_VIOLATION	CB_CHANNEL_MAX_VIOLATION	CR_CHANNEL_MIN_VIOLATION	CR_CHANNEL_MAX_VIOLATION	
0x53	Interrupt Status 5	R					DIAG_TRI2_L1		DIAG_TRI1_L1		
0x54	Interrupt Clear 5	W					DIAG_TRI2_L1_CLR		DIAG_TRI1_L1_CLR		0x00
0x55	Interrupt Mask 5	R/W					DIAG_TRI2_L1_MSK		DIAG_TRI1_L1_MSK		0x00
0x60	VDP_CONFIG_1	R/W					WST_PKT_DECODE_DISABLE	VDP_TTXT_TYPE_MAN_ENABLE	VDP_TTXT_TYPE_MAN[1]	VDP_TTXT_TYPE_MAN[0]	0x88
0x62	VDP_ADF_CONFIG_1	R/W	ADF_ENABLE	ADF_MODE[1]	ADF_MODE[0]	ADF_DID[4]	ADF_DID[3]	ADF_DID[2]	ADF_DID[1]	ADF_DID[0]	0x15
0x63	VDP_ADF_CONFIG_2	R/W	DUPLICATE_ADF		ADF_SDID[5]	ADF_SDID[4]	ADF_SDID[3]	ADF_SDID[2]	ADF_SDID[1]	ADF_SDID[0]	0x2A
0x64	VDP_LINE_00E	R/W	MAN_LINE_PGM				VBI_DATA_P318[3]	VBI_DATA_P318[2]	VBI_DATA_P318[1]	VBI_DATA_P318[0]	0x00
0x65	VDP_LINE_00F	R/W	VBI_DATA_P6_N23[3]	VBI_DATA_P6_N23[2]	VBI_DATA_P6_N23[1]	VBI_DATA_P6_N23[0]	VBI_DATA_P319_N286[3]	VBI_DATA_P319_N286[2]	VBI_DATA_P319_N286[1]	VBI_DATA_P319_N286[0]	0x00
0x66	VDP_LINE_010	R/W	VBI_DATA_P7_N24[3]	VBI_DATA_P7_N24[2]	VBI_DATA_P7_N24[1]	VBI_DATA_P7_N24[0]	VBI_DATA_P320_N287[3]	VBI_DATA_P320_N287[2]	VBI_DATA_P320_N287[1]	VBI_DATA_P320_N287[0]	0x00
0x67	VDP_LINE_011	R/W	VBI_DATA_P8_N25[3]	VBI_DATA_P8_N25[2]	VBI_DATA_P8_N25[1]	VBI_DATA_P8_N25[0]	VBI_DATA_P321_N288[3]	VBI_DATA_P321_N288[2]	VBI_DATA_P321_N288[1]	VBI_DATA_P321_N288[0]	0x00
0x68	VDP_LINE_012	R/W	VBI_DATA_P9[3]	VBI_DATA_P9[2]	VBI_DATA_P9[1]	VBI_DATA_P9[0]	VBI_DATA_P322[3]	VBI_DATA_P322[2]	VBI_DATA_P322[1]	VBI_DATA_P322[0]	0x00
0x69	VDP_LINE_013	R/W	VBI_DATA_P10[3]	VBI_DATA_P10[2]	VBI_DATA_P10[1]	VBI_DATA_P10[0]	VBI_DATA_P323[3]	VBI_DATA_P323[2]	VBI_DATA_P323[1]	VBI_DATA_P323[0]	0x00
0x6A	VDP_LINE_014	R/W	VBI_DATA_P11[3]	VBI_DATA_P11[2]	VBI_DATA_P11[1]	VBI_DATA_P11[0]	VBI_DATA_P324_N272[3]	VBI_DATA_P324_N272[2]	VBI_DATA_P324_N272[1]	VBI_DATA_P324_N272[0]	0x00
0x6B	VDP_LINE_015	R/W	VBI_DATA_P12_N10[3]	VBI_DATA_P12_N10[2]	VBI_DATA_P12_N10[1]	VBI_DATA_P12_N10[0]	VBI_DATA_P325_N273[3]	VBI_DATA_P325_N273[2]	VBI_DATA_P325_N273[1]	VBI_DATA_P325_N273[0]	0x00
0x6C	VDP_LINE_016	R/W	VBI_DATA_P13_N11[3]	VBI_DATA_P13_N11[2]	VBI_DATA_P13_N11[1]	VBI_DATA_P13_N11[0]	VBI_DATA_P326_N274[3]	VBI_DATA_P326_N274[2]	VBI_DATA_P326_N274[1]	VBI_DATA_P326_N274[0]	0x00
0x6D	VDP_LINE_017	R/W	VBI_DATA_P14_N12[3]	VBI_DATA_P14_N12[2]	VBI_DATA_P14_N12[1]	VBI_DATA_P14_N12[0]	VBI_DATA_P327_N275[3]	VBI_DATA_P327_N275[2]	VBI_DATA_P327_N275[1]	VBI_DATA_P327_N275[0]	0x00
0x6E	VDP_LINE_018	R/W	VBI_DATA_P15_N13[3]	VBI_DATA_P15_N13[2]	VBI_DATA_P15_N13[1]	VBI_DATA_P15_N13[0]	VBI_DATA_P328_N276[3]	VBI_DATA_P328_N276[2]	VBI_DATA_P328_N276[1]	VBI_DATA_P328_N276[0]	0x00
0x6F	VDP_LINE_019	R/W	VBI_DATA_P16_N14[3]	VBI_DATA_P16_N14[2]	VBI_DATA_P16_N14[1]	VBI_DATA_P16_N14[0]	VBI_DATA_P329_N277[3]	VBI_DATA_P329_N277[2]	VBI_DATA_P329_N277[1]	VBI_DATA_P329_N277[0]	0x00
0x70	VDP_LINE_01A	R/W	VBI_DATA_P17_N15[3]	VBI_DATA_P17_N15[2]	VBI_DATA_P17_N15[1]	VBI_DATA_P17_N15[0]	VBI_DATA_P330_N278[3]	VBI_DATA_P330_N278[2]	VBI_DATA_P330_N278[1]	VBI_DATA_P330_N278[0]	0x00
0x71	VDP_LINE_01B	R/W	VBI_DATA_P18_N16[3]	VBI_DATA_P18_N16[2]	VBI_DATA_P18_N16[1]	VBI_DATA_P18_N16[0]	VBI_DATA_P331_N279[3]	VBI_DATA_P331_N279[2]	VBI_DATA_P331_N279[1]	VBI_DATA_P331_N279[0]	0x00
0x72	VDP_LINE_01C	R/W	VBI_DATA_P19_N17[3]	VBI_DATA_P19_N17[2]	VBI_DATA_P19_N17[1]	VBI_DATA_P19_N17[0]	VBI_DATA_P332_N280[3]	VBI_DATA_P332_N280[2]	VBI_DATA_P332_N280[1]	VBI_DATA_P332_N280[0]	0x00
0x73	VDP_LINE_01D	R/W	VBI_DATA_P20_N18[3]	VBI_DATA_P20_N18[2]	VBI_DATA_P20_N18[1]	VBI_DATA_P20_N18[0]	VBI_DATA_P333_N281[3]	VBI_DATA_P333_N281[2]	VBI_DATA_P333_N281[1]	VBI_DATA_P333_N281[0]	0x00
0x74	VDP_LINE_01E	R/W	VBI_DATA_P21_N19[3]	VBI_DATA_P21_N19[2]	VBI_DATA_P21_N19[1]	VBI_DATA_P21_N19[0]	VBI_DATA_P334_N282[3]	VBI_DATA_P334_N282[2]	VBI_DATA_P334_N282[1]	VBI_DATA_P334_N282[0]	0x00
0x75	VDP_LINE_01F	R/W	VBI_DATA_P22_N20[3]	VBI_DATA_P22_N20[2]	VBI_DATA_P22_N20[1]	VBI_DATA_P22_N20[0]	VBI_DATA_P335_N283[3]	VBI_DATA_P335_N283[2]	VBI_DATA_P335_N283[1]	VBI_DATA_P335_N283[0]	0x00
0x76	VDP_LINE_020	R/W	VBI_DATA_P23_N21[3]	VBI_DATA_P23_N21[2]	VBI_DATA_P23_N21[1]	VBI_DATA_P23_N21[0]	VBI_DATA_P336_N284[3]	VBI_DATA_P336_N284[2]	VBI_DATA_P336_N284[1]	VBI_DATA_P336_N284[0]	0x00
0x77	VDP_LINE_021	R/W	VBI_DATA_P24_N22[3]	VBI_DATA_P24_N22[2]	VBI_DATA_P24_N22[1]	VBI_DATA_P24_N22[0]	VBI_DATA_P337_N285[3]	VBI_DATA_P337_N285[2]	VBI_DATA_P337_N285[1]	VBI_DATA_P337_N285[0]	0x00
0x78	VDP_STATUS	R	TTXT_AVL					CGMS_WSS_AVL	CC_EVEN_FIELD	CC_AVL	
0x78	VDP_STATUS_CLEAR	W						CGMS_WSS_CLEAR		CC_CLEAR	0x00

Addr	Register Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0x79	VDP_CCAP_DATA_0	R	CCAP_BYTE_1[7]	CCAP_BYTE_1[6]	CCAP_BYTE_1[5]	CCAP_BYTE_1[4]	CCAP_BYTE_1[3]	CCAP_BYTE_1[2]	CCAP_BYTE_1[1]	CCAP_BYTE_1[0]	
0x7A	VDP_CCAP_DATA_1	R	CCAP_BYTE_2[7]	CCAP_BYTE_2[6]	CCAP_BYTE_2[5]	CCAP_BYTE_2[4]	CCAP_BYTE_2[3]	CCAP_BYTE_2[2]	CCAP_BYTE_2[1]	CCAP_BYTE_2[0]	
0x7D	VDP_CGMS_WSS_DATA_0	R					CGMS_CRC[5]	CGMS_CRC[4]	CGMS_CRC[3]	CGMS_CRC[2]	
0x7E	VDP_CGMS_WSS_DATA_1	R	CGMS_CRC[1]	CGMS_CRC[0]	CGMS_WSS[13]	CGMS_WSS[12]	CGMS_WSS[11]	CGMS_WSS[10]	CGMS_WSS[9]	CGMS_WSS[8]	
0x7F	VDP_CGMS_WSS_DATA_2	R	CGMS_WSS[7]	CGMS_WSS[6]	CGMS_WSS[5]	CGMS_WSS[4]	CGMS_WSS[3]	CGMS_WSS[2]	CGMS_WSS[1]	CGMS_WSS[0]	
0x9C	VDP_OUTPUT_SEL	R/W				WSS_CGMS_CB_CHANGE					0x30

[1] B at the end of the bit name means an overbar for the whole bit name.

To access the registers listed in Table 90, set the VPP I²C slave address by writing to Register 0xFD in the user sub map. All read only bits are left blank.

Table 90. VPP Map Details

Address	Register Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	0	Hex
0x41	DEINT_RESET	R/W								DEINT_RESET	0x00
0x55	I2C_DEINT_ENABLE	R/W	I2C_DEINT_ENABLE								0x00
0x5B	ADV_TIMING_MODE_EN	R/W	ADV_TIMING_MODE_EN								0x00

To access the registers listed in Table 91, set the MIPI CSI-2 Tx I²C slave address by writing to Register 0xFE in the user sub map. All read only registers are left blank.

Table 91. MIPI CSI-2 Tx Map Details

Addr	Register Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0x00	CSITX_PWRDN	R/W	CSITX_PWRDN								0x80
0x01	TLPX	R/W	TLPX[4]	TLPX[3]	TLPX[2]	TLPX[1]	TLPX[0]				0x18
0x02	THSPREP	R/W	THSPREP[4]	THSPREP[3]	THSPREP[2]	THSPREP[1]	THSPREP[0]				0x18
0x03	THSZEROS	R/W	THSZEROS[4]	THSZEROS[3]	THSZEROS[2]	THSZEROS[1]	THSZEROS[0]				0x30
0x04	THSTRAIL	R/W	THSTRAIL[4]	THSTRAIL[3]	THSTRAIL[2]	THSTRAIL[1]	THSTRAIL[0]				0x20
0x05	THSEXIT	R/W	THSEXIT[4]	THSEXIT[3]	THSEXIT[2]	THSEXIT[1]	THSEXIT[0]				0x28
0x06	TCLK_PREP	R/W	TCLK_PREP[2]	TCLK_PREP[1]	TCLK_PREP[0]						0x40
0x07	TCLK_ZEROS	R/W	TCLK_ZEROS[4]	TCLK_ZEROS[3]	TCLK_ZEROS[2]	TCLK_ZEROS[1]	TCLK_ZEROS[0]				0x58
0x08	TCLK_TRAIL	R/W	TCLK_TRAIL[3]	TCLK_TRAIL[2]	TCLK_TRAIL[1]	TCLK_TRAIL[0]					0x30
0x09	ANCILLARY_DI	R/W	ANCILLARY_DI[5]	ANCILLARY_DI[4]	ANCILLARY_DI[3]	ANCILLARY_DI[2]	ANCILLARY_DI[1]	ANCILLARY_DI[0]			0xC0
0x0A	VBIVIDEO_DI	R/W	VBIVIDEO_DI[5]	VBIVIDEO_DI[4]	VBIVIDEO_DI[3]	VBIVIDEO_DI[2]	VBIVIDEO_DI[1]	VBIVIDEO_DI[0]			0xC4
0x0B	LSPKT_DI	R/W	LSPKT_DI[5]	LSPKT_DI[4]	LSPKT_DI[3]	LSPKT_DI[2]	LSPKT_DI[1]	LSPKT_DI[0]			0x08
0x0C	LEPKT_DI	R/W	LEPKT_DI[5]	LEPKT_DI[4]	LEPKT_DI[3]	LEPKT_DI[2]	LEPKT_DI[1]	LEPKT_DI[0]			0x0C
0x0D	VC_REF	R/W	VC_REF[1]	VC_REF[0]							0x00
0x0E	CKSUM_EN	R/W	CKSUM_EN								0x80
0x1F	CSI_FRAME_NUM_CTL	R/W	FRAMENUMBER_INTERLACED	FBIT_VAL_AT_FIELD1START_INTERLACED							0x40
0x20	CSI_LINENUM_INCR_INTERLACED	R/W	LINENUMBER_INCR_INTERLACED								0x00
0x26	ESC_MODE_CTL	R/W	ESC_MODE_EN_D0	ESC_XSHUTDOWN_D0	ESC_MODE_EN_CLK	ESC_XSHUTDOWN_CLK					0x50
0xDE	DPHY_PWDN_CTL	R/W							DPHY_PWDN_OVERRIDE	DPHY_PWDN	0x01

USER SUB MAP DESCRIPTION

To access all the registers listed in Table 92, SUB_USR_EN[1:0] in Register Address 0x0E must be programmed to 00. The gray shading is the default.

Table 92. User Sub Map Register Descriptions

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x00	Input control	INSEL[4:0]; the INSEL bits allow the user to select an input channel and the input format				0	0	0	0	0	CVBS input on $A_{IN}1$	
						0	0	0	0	1	CVBS input on $A_{IN}2$	
						0	0	0	1	0	CVBS input on $A_{IN}3$	
						0	0	0	1	1	CVBS input on $A_{IN}4$	
						0	1	0	0	0	Y input on $A_{IN}1$, C input on $A_{IN}2$	
						0	1	0	0	1	Y input on $A_{IN}3$, C input on $A_{IN}4$	
						0	1	1	0	0	Y input on $AI_{IN}1$, Pb input on $A_{IN}2$, Pr input on $A_{IN}3$	
						0	1	1	1	0	Differential positive on $A_{IN}1$, differential negative on $A_{IN}2$	
						0	1	1	1	1	Differential positive on $A_{IN}3$, differential negative on $A_{IN}4$	
0x01	Video Selection 1	Reserved						0	0	0	Sets to default	
		ENVSPROC					0				Disables VSYNC processor	
							1				Enables VSYNC processor	
		Reserved				0					Sets to default	
		Betacam; enables betacam levels			0						Standard video input	
					1						Betacam input enable	
		ENHSPLL		0							Disables HSYNC processor	
				1							Enables HSYNC processor	
		Reserved	1								Sets to default	
0x02	Video Selection 2	Reserved					0	1	0	0	Sets to default	
		VID_SEL[3:0]; the VID_SEL bits allow the user to select the input video standard	0	0	0	0					Autodetects PAL B/PAL G/PAL H/ PAL I/PAL D, NTSC J (no pedestal), SECAM	
			0	0	0	1					Autodetects PAL B/PAL G/PAL H/ PAL I/PAL D, NTSC M (pedestal), SECAM	
			0	0	1	0					Autodetects PAL N (pedestal), NTSC J (no pedestal), SECAM	
			0	0	1	1					Autodetects PAL N (pedestal), NTSC M (pedestal) SECAM	
			0	1	0	0					NTSC J	
			0	1	0	1					NTSC M	
			0	1	1	0					PAL 60	
			0	1	1	1					NTSC 4.43	
			1	0	0	0					PAL B/PAL G/PAL H/PAL I/PAL D	
			1	0	0	1					PAL N = PAL B/PAL G/PAL H/ PAL I/PAL D (with pedestal)	
			1	0	1	0					PAL M (without pedestal)	
			1	0	1	1					PAL M	
			1	1	0	0					PAL Combination N	
			1	1	0	1					PAL Combination N (with pedestal)	
			1	1	1	0					SECAM	
			1	1	1	1					SECAM	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x03	Output control	Reserved			0	0	1	1	0	0	Reserved	
		TOD; tristate output drivers; this bit allows the user to tristate the output drivers; pixel outputs, HS and VS/FIELD/SFL		0							Output drivers enabled	See also TIM_OE and TRI_LLC
				1							Output drivers tristated	
		VBI_EN; vertical blanking interval data enable; allows VBI data (Line 1 to Line 21) to be passed through with only a minimum amount of filtering performed	0								All lines filtered and scaled	
			1								Only active video region filtered	
0x04	Extended output control	Range; allows the user to select the range of output values; can be ITU-R BT.656 compliant or can fill the whole accessible number range								0	16 ≤ Y ≤ 235, 16 ≤ C/P ≤ 240	ITU-R BT.656
										1	1 ≤ Y ≤ 254, 1 ≤ C/P ≤ 254	Extended range
		EN_SFL_PIN							0		Disables SFL output	SFL output enables encoder and decoder to be connected directly
									1		Outputs SFL information on the SFL pin	
		BL_C_VBI; blank chroma during VBI; if set, it enables data in the VBI region to be passed through the decoder undistorted						0			Decode and output color during VBI	
								1			Blank Cr and Cb values during VBI	
		TIM_OE; enables timing signals output					0				HS and VS/FIELD/SFL tristated	Controlled by TOD
							1				HS and VS/FIELD/SFL forced active	
		Reserved		0	1	1						
		BT.656-4; allows the user to select an output mode compatible with ITU-R BT.656-3/-4	0								ITU-R BT.656-3 compatible	
			1								ITU-R BT.656-4 compatible	
0x07	Autodetect enable	AD_PAL_EN; PAL B/ PAL D/PAL I/PAL G/ PAL H autodetect enable								0	Disables	
										1	Enables	
		AD_NTSC_EN; NTSC autodetect enable							0		Disables	
									1		Enables	
		AD_PALM_EN; PAL M autodetect enable						0			Disables	
								1			Enables	
		AD_PALN_EN; PAL N autodetect enable					0				Disables	
							1				Enables	
		AD_P60_EN; PAL 60 autodetect enable				0					Disables	
						1					Enables	
		AD_N443_EN; NTSC 4.43 autodetect enable			0						Disables	
					1						Enables	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
		AD_SECAM_EN; SECAM autodetect enable		0							Disables	
				1							Enables	
		AD_SEC525_EN; SECAM 525 autodetect enable	0								Disables	
			1								Enables	
0x08	Contrast	CON[7:0]; contrast adjust; this is the user control for contrast adjustment	1	0	0	0	0	0	0	0	0x00 = 0 gain on luma channel 0x80 = unity gain on luma channel 0xFF = 2× gain on luma channel	
0x0A	Brightness adjust	BRI[7:0]; this register controls the brightness of the video signal	0	0	0	0	0	0	0	0	0x00 = 0 IRE luma channel offset	
											0x7F = +30 IRE luma channel offset	
											0x80 = −30 IRE luma channel offset	
0x0B	Hue adjust	HUE[7:0]; this register contains the value for the color hue adjustment	0	0	0	0	0	0	0	0	0x00 = 0° chroma phase adjust	
											0x7F = −90° chroma phase adjust	
											0x80 = +90° chroma phase adjust	
0x0C	Default Value Y	DEF_VAL_EN; default value enable								0	Free run mode dependent on DEF_VAL_AUTO_EN	
										1	Forces free run mode on	
		DEF_VAL_AUTO_EN; default value automatic enable							0		Disables free run mode	When lock is lost, free run mode can be enabled to output stable timing, clock, and a set color
									1		Enables automatic free run mode	
		DEF_Y[5:0]; default value is Y; this register holds the Y default value	0	0	1	1	0	1			Y[7:0] = (DEF_Y[5:0], 0, 0)	Default Y value output in free run mode
0x0D	Default Value C	DEF_C[7:0]; default value is C; the Cr and Cb default values are defined in this register	0	1	1	1	1	1	0	0	Cr[3:0] = (DEF_C[7:4]), Cb[3:0] = (DEF_C[3:0])	Default Cb/Cr value output in free run mode; default values output a blue
0x0E	Analog devices Control 1	Reserved				0	0	0	0	0	Sets as default	
		SUB_USR_EN[1:0]; enables user to access the Interrupt/VDP Sub map and User Sub Map 2		0	0						Accesses user sub map register space	
				0	1						Accesses the interrupt/VDP sub map register space	
				1	0						Accesses User Sub Map 2	
		Reserved	0								Sets as default	
0x0F	Power management	Reserved				0	0	0	0	0	Sets to default	
		PWRDWN; power-down places the decoder into a full power-down mode			0						System functional	
					1						Powered down	
		Reserved		0							Sets to default	
		Reset; chip reset, loads all I²C bits with default values	0								Normal operation	
			1								Starts reset sequence	Executing reset takes approximately 2 ms; this bit is self clearing

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x10	Status 1 (read only)	IN_LOCK								X	1 = in lock (now)	Provides information about the internal status of the decoder
		LOST_LOCK							X		1 = lost lock (since last read)	
		FSC_LOCK						X			1 = f_{SC} lock (now)	
		FOLLOW_PW					X				1 = peak white AGC mode active	
		AD_RESULT[2:0]; autodetection result reports the standard of the input video		0	0	0					NTSC M/NTSC J	Detected standard
				0	0	1					NTSC 4.43	
				0	1	0					PAL M	
				0	1	1					PAL 60	
				1	0	0					PAL B/PAL G/PAL H/PAL I/PAL D	
				1	0	1					SECAM	
				1	1	0					PAL Combination N	
				1	1	1					SECAM 525	
		COL_KILL	X								1 = color kill is active	Color kill
0x11	IDENT (read only)	IDENT[7:0]; provides ID on the revision of the device	0	1	0	0	0	0	1	0		Power-up value = 0x42
0x12	Status 2 (read only)	MVCS_DET								X	Rovi color striping detected	1 = detected
		MVCS_T3							X		MV color striping type	0 = Type 2, 1 = Type 3
		MV_PS_DET						X			MV pseudosync detected	1 = detected
		MV_AGC_DET					X				MV AGC pulses detected	1 = detected
		LL_NSTD				X					Nonstandard line length	1 = detected
		FSC_NSTD			X						Nonstandard f_{SC}	1 = detected
		Reserved	X	X								
0x13	Status 3 (read only)	INST_HLOCK								X	1 = horizontal lock achieved	Unfiltered
		Reserved							X		Reserved	
		SD_OP_50Hz						0			SD 60 Hz detected	SD field rate detect
								1			SD 50 Hz detected	
		Reserved					X					
		FREE_RUN_ACT				X					1 = free run mode active	
		STD_FLD_LEN			X						1 = field length standard	Correct field length found
		Interlaced		X							1 = interlaced video detected	Field sequence found
		PAL_SW_LOCK	X								1 = swinging burst detected	Reliable swinging burst sequence
0x14	Analog clamp control	FREE_RUN_PAT_SEL[2:0]						0	0	0	Single color set by DEF_C and DEF_Y; see the Color Controls section	
								0	0	1	100% color bars	
								0	1	0	Luma ramp	
								1	0	1	Boundary box	
		Reserved					0				Sets to default	
		CCLEN; current clamp enable allows the user to switch off the current sources in the analog front				0					Current sources switched off	
						1					Current sources enabled	
		Reserved	0	0	0						Sets to default	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x15	Digital Clamp Control 1	Reserved					X	X	X	X	Sets to default	
		DCFE; digital clamp freeze enable				0					Digital clamp on	
						1					Digital clamp off	
		DCT[1:0]; digital clamp timing determines the time constant of the digital fine clamp circuitry		0	0						Slow (TC = 1 sec)	
				0	1						Medium (TC = 0.5 sec)	
				1	0						Fast (TC = 0.1 sec)	
				1	1						TC dependent on video	
		Reserved	0								Sets to default	
0x17	Shaping Filter Control 1	YSFM[4:0]; selects Y shaping filter mode in CVBS-only mode; allows the user to select a wide range of low-pass/notch filters; if either auto mode is selected, the decoder selects the optimum Y filter depending on the CVBS video source quality (good vs. poor)				0	0	0	0	0	Autowide notch for poor quality sources or wideband filter with comb for good quality input	Decoder selects optimum Y shaping filter depending on CVBS quality
						0	0	0	0	1	Autonarrow notch for poor quality sources or wideband filter with comb for good quality input	
						0	0	0	1	0	SVHS 1	If one of these modes is selected, the decoder does not change filter modes; depending on video quality, a fixed filter response (the one selected) is used for stable and less stable video sources
						0	0	0	1	1	SVHS 2	
						0	0	1	0	0	SVHS 3	
						0	0	1	0	1	SVHS 4	
						0	0	1	1	0	SVHS 5	
						0	0	1	1	1	SVHS 6	
						0	1	0	0	0	SVHS 7	
						0	1	0	0	1	SVHS 8	
						0	1	0	1	0	SVHS 9	
						0	1	0	1	1	SVHS 10	
						0	1	1	0	0	SVHS 11	
						0	1	1	0	1	SVHS 12	
						0	1	1	1	0	SVHS 13	
						0	1	1	1	1	SVHS 14	
						1	0	0	0	0	SVHS 15	
						1	0	0	0	1	SVHS 16	
						1	0	0	1	0	SVHS 17	
						1	0	0	1	1	SVHS 18 (CCIR 601)	
						1	0	1	0	0	PAL NN1	
						1	0	1	0	1	PAL NN2	
						1	0	1	1	0	PAL NN3	
						1	0	1	1	1	PAL WN1	
						1	1	0	0	0	PAL WN2	
						1	1	0	0	1	NTSC NN1	
						1	1	0	1	0	NTSC NN2	
						1	1	0	1	1	NTSC NN3	
						1	1	1	0	0	NTSC WN1	
						1	1	1	0	1	NTSC WN2	
						1	1	1	1	0	NTSC WN3	
						1	1	1	1	1	Reserved	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
		CSFM[2:0]: C shaping filter mode allows selection from a range of low-pass chrominance filters; if either auto mode is selected, the decoder selects the optimum C filter depending on the CVBS video source quality (good vs. bad); nonauto settings force a C filter for all standards and quality of CVBS video	0	0	0						Autoselection 1.5 MHz	Automatically selects a C filter based on video standard and quality
			0	0	1						Autoselection 2.17 MHz	
			0	1	0						SH1	Selects a C filter for all video standards and for good and bad video
			0	1	1						SH2	
			1	0	0						SH3	
			1	0	1						SH4	
			1	1	0						SH5	
			1	1	1						Wideband mode	
0x18	Shaping Filter Control 2	WYSFM[4:0]; wideband Y shaping filter mode allows the user to select which Y shaping filter is used for the Y component of Y/C, YPrPb, bandwidth input signals; it is also used when a good quality input CVBS signal is detected; for all other inputs, the Y shaping filter chosen is controlled by YSFM[4:0]				0	0	0	0	0	Reserved, do not use	
						0	0	0	0	1	Reserved, do not use	
						0	0	0	1	0	SVHS 1	
						0	0	0	1	1	SVHS 2	
						0	0	1	0	0	SVHS 3	
						0	0	1	0	1	SVHS 4	
						0	0	1	1	0	SVHS 5	
						0	0	1	1	1	SVHS 6	
						0	1	0	0	0	SVHS 7	
						0	1	0	0	1	SVHS 8	
						0	1	0	1	0	SVHS 9	
						0	1	0	1	1	SVHS 10	
						0	1	1	0	0	SVHS 11	
						0	1	1	0	1	SVHS 12	
						0	1	1	1	0	SVHS 13	
						0	1	1	1	1	SVHS 14	
						1	0	0	0	0	SVHS 15	
						1	0	0	0	1	SVHS 16	
						1	0	0	1	0	SVHS 17	
						1	0	0	1	1	SVHS 18 (CCIR 601)	
						1	0	1	0	0	Reserved, do not use	
						1	1	1	1	1	Reserved, do not use	
		Reserved		0	0						Sets to default	
		WYSFMOVR; enables use of the automatic WYSFM filter	0								Autoselection of best filter	
			1								Manual select filter using WYSFM[4:0]	
0x19	Comb filter control	PSFSEL[1:0]; controls the signal bandwidth that is fed to the comb filters (PAL)							0	0	Narrow	
									0	1	Medium	
									1	0	Wide	
									1	1	Widest	
		NSFSEL[1:0]; controls the signal bandwidth that is fed to the comb filters (NTSC)					0	0			Narrow	
							0	1			Medium	
							1	0			Medium	
							1	1			Wide	
		Reserved	1	1	1	1						
0x1D	Analog devices Control 2	Reserved			0	0	0	X	X	X		
		Reserved		1								
		TRI_LLC; tristate LLC driver	0								LLC pin active	
			1								LLC pin tristated	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x27	Pixel delay control	LTA[1:0]; luma timing adjust allows the user to specify a timing difference between chroma and luma samples							0	0	No delay	CVBS mode, LTA[1:0] = 00b; Y/C mode, LTA[1:0] = 01b; YPrPb mode, LTA[1:0] = 01b
									0	1	Luma one clock (37 ns) late	
									1	0	Luma two clocks (74 ns) early	
									1	1	Luma one clock (37 ns) early	
		Reserved						0			Sets to 0	
		CTA[2:0]; chroma timing adjust allows a specified timing difference between the luma and chroma samples			0	0	0				Reserved	CVBS mode, CTA[2:0] = 011b; Y/C mode, CTA[2:0] = 101b; YPrPb mode, CTA[2:0] = 110b
					0	0	1				Chroma + two pixels (early)	
					0	1	0				Chroma + one pixel (early)	
					0	1	1				No delay	
					1	0	0				Chroma − one pixel (late)	
					1	0	1				Chroma − two pixels (late)	
					1	1	0				Chroma − three pixels (late)	
					1	1	1				Reserved	
		AUTO_PDC_EN; automatic programmed delay control. automatically programs the LTA/CTA values so that luma and chroma are aligned at the output for all modes of operation		0							Use values in LTA[1:0] and CTA[2:0] for delaying luma/chroma	
				1							LTA and CTA values determined automatically	
		SWPC; allows the Cr and Cb samples to be swapped	0								No swapping	
			1								Swaps the Cr and Cb output samples	
0x2B	Misc gain control	PW_UPD; peak white update determines the rate of gain								0	Updates once per video line	Peak white must be enabled; see LAGC[2:0]
										1	Updates once per field	
		Reserved			1	0	0	0	0		Sets to default	
		CKE; color kill enable allows the color kill function to be switched on and off		0							Color kill disabled	For SECAM color kill, the threshold is set at 8%; see CKILLTHR[2:0]
				1							Color kill enabled	
		Reserved	1								Sets to default	
0x2C	AGC mode control	CAGC[1:0]; chroma automatic gain control selects the basic mode of operation for the AGC in the chroma path							0	0	Manual fixed gain	Use CMG[11:0]
									0	1	Uses luma gain for chroma	
									1	0	Automatic gain	Based on color burst
									1	1	Freeze chroma gain	
		Reserved					1	1			Sets to 1	
		LAGC[2:0]; luma automatic gain control selects the mode of operation for the gain control in the luma path		0	0	0					Manual fixed gain	Uses LMG[11:8]
				0	0	1					AGC peak white algorithm off	Blank level to sync tip
				0	1	0					AGC peak white algorithm on	Blank level to sync tip
				0	1	1					Reserved	
				1	0	0					Reserved	
				1	0	1					Reserved	
				1	1	0					Reserved	
				1	1	1					Freeze gain	
		Reserved	1								Sets to 1	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x2D	Chroma Gain Control 1, Chroma Gain 1 (CG)	CMG[11:8]/CG[11:8]; in manual mode, the chroma gain control can program a desired manual chroma gain; in auto mode, it can read back the current gain value					0	1	0	0		CAGC[1:0] settings decide in which mode CMG[11:0] operates
		Reserved			1	1					Sets to 1	Has an effect only if CAGC[1:0] is set to autogain (10)
		CAGT[1:0]; chroma automatic gain timing allows adjustment of the chroma AGC tracking speed	0	0							Slow (TC = 2 sec)	
			0	1							Medium (TC = 1 sec)	
			1	0							Reserved	
			1	1							Adaptive	
0x2E	Chroma Gain Control 2, Chroma Gain 2 (CG)	CMG[7:0]/CG[7:0]; chroma manual gain lower eight bits; see CMG[11:8]/CG[11:8] for description	0	0	0	0	0	0	0	0	CMG[11:0] = see the Chroma Gain section	Minimum value = 0 decimal, maximum value = 4095 decimal
0x2F	Luma Gain Control 1, Luma Gain 1 (LG)	LMG[11:8]/LG[11:8]; in manual mode, luma gain control can program a desired manual luma gain; in auto mode, it can read back the actual gain value used					X	X	X	X	LAGC[1:0] settings decide in which mode LMG[11:8] operates	
		Reserved			1	1					Sets to 1	
		LAGT[1:0]; luma automatic gain timing allows adjustment of the luma AGC tracking speed	0	0							Slow (TC = 2 sec)	Has an effect only if LAGC[1:0] is set to autogain (001, 010)
			0	1							Medium (TC = 1 sec)	
			1	0							Fast (TC = 0.2 sec)	
			1	1							Adaptive	
0x30	Luma Gain Control 2, Luma Gain 2 (LG)	LMG[7:0]/LG[7:0]; luma manual gain/ luma gain lower eight bits; see LMG[11:8]/LG[11:8] for description	X	X	X	X	X	X	X	X	LMG[7:0]/LG[7:0]; luma manual gain/luma gain lower eight bits; see LMG[11:8]/LG[11:8] for description	Minimum value = 1024 decimal, Maximum value = 4095 decimal
0x31	VS/FIELD Control 1	Reserved						0	1	0	Sets to default	
		HVSTIM; horizontal VSYNC timing; selects where within a line of video the VSYNC signal is asserted					0				Start of line relative to HSE	HSE = HSC end
							1				Start of line relative to HSB	HSB = HS begin
		NEWAVMODE; sets the EAV/SAV mode				0					EAV/SAV codes generated to suit Analog devices encoders	
						1					Manual VS/FIELD position controlled by the Register 0x32, Register 0x33, and Register 0xE5 to Register 0xEA	
		Reserved	0	0	0						Sets to default	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x32	VS/FIELD Control 2	Reserved			0	0	0	0	0	1	Sets to default	NEWAVMODE bit must be set high
		VSBHE		0							VSYNC signal goes high in the middle of the line (even field)	
				1							VSYNC signal changes state at the start of the line (even field)	
		VSBHO	0								VSYNC signal goes high in the middle of the line (odd field)	
			1								VSYNC signal changes state at the start of the line (odd field)	
0x33	VS/FIELD Control 3	Reserved			0	0	0	1	0	0	Sets to default	
		VSEHE		0							VSYNC signal goes low in the middle of the line (even field)	NEWAVMODE bit must be set high
				1							VSYNC signal changes state at the start of the line (even field)	
		VSEHO	0								VSYNC signal goes low in the middle of the line (odd field)	
			1								VSYNC signal changes state at the start of the line odd field	
0x34	HS Position Control 1	HSE[10:8]; HSYNC end allows positioning of the HSYNC output within the video line						0	0	0	HSYNC output ends HSE[10:0] pixels after the falling edge of HSYNC	Using HSB and HSE, the position/length of the output HSYNC can be programmed
		Reserved					0				Sets to 0	
		HSB[10:8]; HSYNC begin allows positioning of the HSYNC output within the video line		0	0	0					HS output starts HSB[10:0] pixels after the falling edge of HSYNC	
		Reserved	0								Sets to 0	
0x35	HS Position Control 2	HSB[7:0]; see Address 0x34, using HSB[10:0] and HSE[10:0], users can program the position and length of the HSYNC output signal	0	0	0	0	0	0	1	0		
0x36	HS Position Control 3	HSE[7:0]; see Address 0x35 description	0	0	0	0	0	0	0	0		
0x37	Polarity	PCLK; sets polarity of LLC								0	Inverts polarity	
										1	Normal polarity as per the timing diagrams in the ADV7280A and ADV7282A data sheets	
		Reserved						0	0		Sets to 0	
		PF; sets the FIELD polarity					0					
							1					
		Reserved				0						
		PVS; sets the VSYNC polarity			0						Active high	
					1						Active low	
		Reserved		0							Sets to 0	
		PHS; sets HSYNC polarity	0		0						Active high	
			1		1						Active low	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x38	NTSC comb control	YCMN[2:0]; luma comb mode, NTSC						0	0	0	Adaptive three-line, three-tap luma comb	
								1	0	0	Disables luma comb; low-pass/notch filter enabled	
								1	0	1	Fixed luma comb two-line (two taps)	Top lines of memory
								1	1	0	Fixed luma comb three-line (three taps)	All lines of memory
								1	1	1	Fixed luma comb two-line (two taps)	Bottom lines of memory
		CCMN[2:0]; chroma comb mode, NTSC			0	0	0				Adaptive three-line for CTAPSN = 01, adaptive four-line for CTAPSN = 10, adaptive five-line for CTAPSN = 11	
					1	0	0				Disables chroma comb	
					1	0	1				Fixed two-line for CTAPSN = 01, fixed three-line for CTAPSN = 10, fixed four-line for CTAPSN = 11	Top lines of memory
					1	1	0				Fixed three-line for CTAPSN = 01, fixed four-line for CTAPSN = 10, fixed five-line for CTAPSN = 11	All lines of memory
					1	1	1				Fixed two-line for CTAPSN = 01, fixed three-line for CTAPSN = 10, fixed four-line for CTAPSN = 11	Bottom lines of memory
		CTAPSN[1:0]; chroma comb taps, NTSC	0	0							Not used	
			0	1							Adapts three lines to two lines	
			1	0							Adapts five lines to three lines	
			1	1							Adapts five lines to four lines	
0x39	PAL comb control	YCMP[2:0]; luma comb mode, PAL						0	0	0	Adaptive five-line, three-tap luma comb	
								1	0	0	Disables luma comb; low-pass/notch filter enabled	
								1	0	1	Fixed three lines (two taps) luma comb (three-line)	Top lines of memory
								1	1	0	Fixed five lines (three taps) luma comb (five-line)	All lines of memory
								1	1	1	Fixed three lines (two taps) luma comb (three-line)	Bottom lines of memory
		CCMP[2:0]; chroma comb mode, PAL			0	0	0				Adaptive three-line chroma for CTAPSN = 01, adaptive four-line chroma for CTAPSN = 10, adaptive five-line chroma for CTAPSN = 11	
					1	0	0				Disable chroma comb	
					1	0	1				Fixed two-line chroma for CTAPSN = 01, fixed three-line chroma for CTAPSN = 10, fixed four-line chroma for CTAPSN = 11	Top lines of memory
					1	1	0				Fixed three-line chroma for CTAPSN = 01, fixed four-line chroma for CTAPSN = 10, fixed five-line chroma for CTAPSN = 11	All lines of memory
					1	1	1				Fixed two-line chroma for CTAPSN = 01, fixed three-line chroma for CTAPSN = 10, fixed four-line chroma for CTAPSN = 11	Bottom lines of memory

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
		CTAPSP[1:0]; chroma comb taps, PAL	0	0							Do not use	
			0	1							Adapts five lines (three taps) to three lines (two taps)	
			1	0							Adapts five lines (five taps) to three lines (three taps)	
			1	1							Adapts five lines (three taps) to four lines (four taps)	
0x3A	ADC control	MUX PDN override; mux power-down override								0		No control over power-down for muxes and associated channel circuit
										1		Allows power-down of MUX_0P/MUX_1/MUX_2 and associated channel circuit; when INSEL[4:0] is used, unused channels are automatically powered down
		PWRDWN_MUX_2; enables power-down of MUX_2 and associated channel clamp and buffer							0		MUX_2 and associated channel in normal operation	
									1		Power down MUX_2 and associated channel operation	MUX PDN override = 1
		PWRDWN_MUX_1; enables power-down of MUX_1 and associated channel clamp and buffer						0			MUX_1 and associated channel in normal operation	
								1			Power down MUX_1 and associated channel operation	MUX PDN override = 1
		PWRDWN_MUX_0P; enables power-down of MUX_0P and associated channel clamp and buffer					0				MUX_0P and associated channel in normal operation	
							1				Power down MUX_0P and associated channel operation	MUX PDN override = 1
		Reserved	0	0	0	0					Sets as default	
0x3D	Manual window control	Reserved					0	0	1	0	Sets to default	
		CKILLTHR[2:0]; color kill threshold		0	0	0					NTSC, PAL color kill at <0.5%, SECAM no color kill	CKE = 1 enables the color kill function and must be enabled for CKILLTHR[2:0] to take effect
				0	0	1					NTSC, PAL color kill at <1.5%, SECAM color kill at <5%	
				0	1	0					NTSC, PAL color kill at <2.5%, SECAM color kill at <7%	
				0	1	1					NTSC, PAL color kill at <4%, SECAM color kill at <8%	
				1	0	0					NTSC, PAL color kill at <8.5%, SECAM color kill at <9.5%	
				1	0	1					NTSC, PAL color kill at <16%, SECAM color kill at <15%	
				1	1	0					NTSC, PAL color kill at <32%, SECAM color kill at <32%	
				1	1	1					Reserved	
		Reserved	0								Sets to default	
0x41	Resample control	Reserved			0	0	0	0	0	1	Sets to default	
		SFL_INV; controls the behavior of the PAL switch bit		0							SFL compatible with the Analog devices video encoders (see the SFL_INV, Address 0x41, Bit 6 (ADV7280A Only) section)	
				1							SFL compatible with older Analog devices video encoders (see the SFL_INV, Address 0x41, Bit 6 (ADV7280A Only) section)	
		Reserved	0								Sets to default	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x4D	CTI DNR Control 1	CTI_EN; CTI enable								0	Disables CTI	
										1	Enables CTI	
		CTI_AB_EN; enables the mixing of the transient improved chroma with the original signal							0		Disables CTI alpha blender	
									1		Enables CTI alpha blender	
		CTI_AB[1:0]; controls the behavior of the alpha-blend circuitry					0	0			Sharpest mixing between sharpened/original chroma signal	
							0	1			Sharp mixing between sharpened and original chroma signal	
							1	0			Smooth mixing between sharpened/original chroma signal	
							1	1			Smoothest mixing between sharpened and original chroma signal	
		Reserved				0					Sets to default	
		DNR_EN; enables or bypasses the DNRx blocks			0						Bypasses the DNRx blocks	
					1						Enables the DNRx blocks	
		Reserved	1	1							Sets to default	
0x4E	CTI DNR Control 2	CTI_C_TH[7:0]; specifies how big the amplitude step must be to be steepened by the CTI block	0	0	0	0	1	0	0	0		
0x50	DNR Noise Threshold 1	DNR_TH[7:0]; specifies the maximum luma edge that is interpreted as noise and is therefore blanked	0	0	0	0	1	0	0	0		
0x51	Lock count	CIL[2:0]; count into lock determines the number of lines the system must remain in lock before showing a locked status						0	0	0	One line of video	
								0	0	1	Two lines of video	
								0	1	0	Five lines of video	
								0	1	1	10 lines of video	
								1	0	0	100 lines of video	
								1	0	1	500 lines of video	
								1	1	0	1000 lines of video	
								1	1	1	100,000 lines of video	
		COL[2:0]; count out of lock determines the number of lines the system must remain out-of-lock before showing a lost-locked status			0	0	0				One line of video	
					0	0	1				Two lines of video	
					0	1	0				Five lines of video	
					0	1	1				10 lines of video	
					1	0	0				100 lines of video	
					1	0	1				500 lines of video	
					1	1	0				1000 lines of video	
					1	1	1				100,000 lines of video	
		SRLS; select raw lock signal and selects the determination of the lock status		0							Over field with vertical info	
				1							Line-to-line evaluation	
		FSCLE; f_{SC} lock enable	0								Lock status set only by horizontal lock	
			1								Lock status set by horizontal lock and subcarrier lock	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x5D	DIAG1 Control	Reserved							0	1		Note that it recommended that the DIAG1 slice level not be set to 75 mV, 225 mV, or 375 mV to achieve optimal performance of the ADV7281A and ADV7282A devices
		DIAG1_SLICE_LEVEL[2:0]				0	0	0			Set the DIAG1 slice level to 75 mV	
						0	0	1			Set the DIAG1 slice level to 225 mV	
						0	1	0			Set the DIAG1 slice level to 375 mV	
						0	1	1			Set the DIAG1 slice level to 525 mV	
						1	0	0			Set the DIAG1 slice level to 675 mV	
						1	0	1			Set the DIAG1 slice level to 825 mV	
						1	1	0			Set the DIAG1 slice level to 975 mV	
						1	1	1			Set the DIAG1 slice level to 1.125 V	
		Reserved			1						Reserved	
		DIAG1_SLICER_PWRDN		0							Power up the DIAG1 slicer	
				1							Power down the DIAG1 slicer	
		Reserved	0								Reserved	
0x5E	DIAG2 Control	Reserved							0	1		Note that it recommended that the DIAG2 slice level not be set to 75 mV, 225 mV, or 375 mV to achieve optimal performance of the ADV7281A and ADV7282A devices
		DIAG2_SLICE_LEVEL[2:0]				0	0	0			Set the DIAG2 slice level to 75 mV	
						0	0	1			Set the DIAG2 slice level to 225 mV	
						0	1	0			Set the DIAG2 slice level to 375 mV	
						0	1	1			Set the DIAG2 slice level to 525 mV	
						1	0	0			Set the DIAG2 slice level to 675 mV	
						1	0	1			Set the DIAG2 slice level to 825 mV	
						1	1	0			Set the DIAG2 slice level to 975 mV	
						1	1	1			Set the DIAG2 slice level to 1.125 V	
		Reserved			1						Reserved	
		DIAG1_SLICER_PWRDN		0							Power up the DIAG1 slicer	
				1							Power down the DIAG1 slicer	
		Reserved	0								Reserved	
0x59	GPO	GPO[0]								0	Logic 0 output from GPO0 pin	GPO_ENABLE must be set to 1 for the GPO outputs to be enabled. GPO outputs only available on ADV7280A-M, ADV7281A-M and ADV7282A-M models.
										1	Logic 1 output from GPO0 pin	
		GPO[1]							0		Logic 0 output from GPO1 pin	
									1		Logic 1 output from GPO1 pin	
		GPO[2]						0			Logic 0 output from GPO2 pin	
								1			Logic 1 output from GPO2 pin	
		Reserved					0				Reserved	
		GPO_ENABLE				0					GPO pins are tristated	
						1					GPO pins are enabled	
		Reserved	0	0	0							

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x60	ADC Switch 3	MUX_0N[3:0]					0	0	0	0	AINx selection. See Table 11, Table 12, Table 14, Table 15 for specific values	To enable this control, please set MAN_MUX_EN = 1. This control varies in functionality for the ADV7280A, ADV7281A, and ADV7282A. See the Manual Muxing Mode section for more information.
							0	0	0	1		
							0	0	1	0		
							0	0	1	1		
							0	1	0	0		
							0	1	0	1		
							0	1	1	0		
							0	1	1	1		
							1	0	0	0		
		Reserved	0	0	0	1						
0x6A	Output Sync Select 1	HS_OUT_SEL[2:0] selects which sync comes out on the HS pin						0	0	0	The HS pin output horizontal sync information.	
								0	0	1	The HS pin outputs vertical sync information.	
								0	1	0	The HS pin outputs field sync information.	
								0	1	1	The HS pin outputs data enable (DE) information.	
								1	0	0	The HS pin outputs subcarrier frequency lock (SFL) information.	
		Reserved	0	0	0	0	0					
0x6B	Output Sync Select 2	FLD_OUT_SEL[2:0] selects which sync comes out on the VS/FIELD/SFL pin						0	0	0	HS	
								0	0	1	VS	
								0	1	0	Field sync	
								0	1	1	DE	
								1	0	0	SFL	
		Reserved	0	0	0	1	0				Set as default	
0x8F	Free Run Line Length 1	Reserved					0	0	0	0	Set as default	
		LLC_PAD_SEL[2:0]; enables manual selection of the clock for the LLC pin		0	0	0					LLC (nominal 27 MHz) selected out on LLC pin	
				1	0	1					LLC (nominal 13.5 MHz) selected out on LLC pin	
		Reserved	0								Sets to default	
0x99	CCAP1 (read only)	CCAP1[7:0]; closed caption data register	X	X	X	X	X	X	X	X	CCAP1[7] contains parity bit for Byte 0	
0x9A	CCAP2 (read only)	CCAP2[7:0]; closed caption data register	X	X	X	X	X	X	X	X	CCAP2[7] contains parity bit for Byte 0	
0x9B	Letterbox 1 (read only)	LB_LCT[7:0]; letterbox data register	X	X	X	X	X	X	X	X	Reports the number of black lines detected at the top of active video	This feature examines the active video at the start and end of each field; it enables format detection even if the video is not accompanied by a CGMS or WSS sequence
0x9C	Letterbox 2 (read only)	LB_LCM[7:0]; letterbox data register	X	X	X	X	X	X	X	X	Reports the number of black lines detected in the middle half of active video if subtitles are detected	
0x9D	Letterbox 3 (read only)	LB_LCB[7:0]; letterbox data register	X	X	X	X	X	X	X	X	Reports the number of black lines detected at the bottom of active video	
0xB2	CRC enable (write only)	Reserved							0	0	Sets as default	
		CRC_ENABLE; enable CRC checksum to validate the derivative of CGMS						0			Turns off CRC check	
								1			The derivative of CGMS goes high with valid checksum	
		Reserved	0	0	0	1	1				Sets as default	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0xC3	ADC Switch 1	MUX_0P[3:0]; manual muxing control for the MUX_0P multiplexor; this setting controls which input is routed to the ADC for processing					0	0	0	0	AINx selection. See Table 11, Table 12, Table 14, Table 15 for specific values	To enable this control, set MAN_MUX_EN = 1. This control varies in function for the ADV7280A, ADV7281A, and ADV7282A. See the Manual Muxing Mode section for more information
							0	0	0	1		
							0	0	1	0		
							0	0	1	1		
							0	1	0	0		
							0	1	0	1		
							0	1	1	0		
							0	1	1	1		
							1	0	0	0		
		MUX_1[3:0]; manual muxing control for the MUX_1 multiplexor; this setting controls which input is routed to the ADC for processing	0	0	0	0					AINx selection. See Table 11, Table 12, Table 14, Table 15 for specific values	To enable this control, please set MAN_MUX_EN = 1. This control varies in function for the ADV7280A, ADV7281A, and ADV7282A. See the Manual Muxing Mode section for more information.
			0	0	0	1						
			0	0	1	0						
			0	0	1	1						
			0	1	0	0						
			0	1	0	1						
			0	1	1	0						
			0	1	1	1						
			1	0	0	0						
0xC4	ADC Switch 2	MUX_2[3:0]; manual muxing control for the MUX_2 multiplexor; this setting controls which input is routed to the ADC for processing					0	0	0	0	AINx selection. Please see Table 11, Table 12, Table 14, Table 15 for specific values	To enable this control, please set MAN_MUX_EN = 1. This control varies in function for the ADV7280A, ADV7281A, and ADV7282A. See the Manual Muxing Mode section for more information.
							0	0	0	1		
							0	0	1	0		
							0	0	1	1		
							0	1	0	0		
							0	1	0	1		
							0	1	1	0		
							0	1	1	1		
							1	0	0	0		
		Reserved		0	0	0						
		MAN_MUX_EN; enable manual setting of input signal muxing	0								Disables	This bit must be set to 1 for manual muxing
			1								Enables	
0xDC	Letterbox Control 1	LB_TH[4:0]; sets the threshold value that determines if a line is black				0	1	1	0	0	Default threshold for the detection of black lines 01101 to 10000—increase threshold, 00000 to 01011—decrease threshold	
		Reserved	1	0	1						Sets as default	
0xDD	Letterbox Control 2	LB_EL[3:0]; programs the end line of the activity window for LB detection (end of field)					1	1	0	0	Letterbox detection ends with the last line of active video on a field, 1100b: 262/525	
		LB_SL[3:0]; programs the start line of the activity window for LB detection (start of field)	1	1	0	0					Letterbox detection aligned with the start of active video, 0100: 23/286 NTSC	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0xDE	ST Noise Readback 1 (read only)	ST_NOISE[10:8]						X	X	X		ST noise[10:0] measures the noise on the horizontal sync tip of video source
		ST_NOISE_VLD					X				When = 1, ST_NOISE[10:0] is valid	
		Reserved										
0xDF	ST Noise Readback 2 (read only)	ST_NOISE[7:0]	X	X	X	X	X	X	X	X		
0xE1	SD offset Cb channel	SD_OFF_Cb[7:0]; adjusts the hue by selecting the offset for the Cb channel	0	0	0	0	0	0	0	0	−312 mV offset applied to the Cb channel	
			1	0	0	0	0	0	0	0	0 mV offset applied to the Cb channel	
			1	1	1	1	1	1	1	1	+312 mV offset applied to the Cb channel	
0xE2	SD offset Cr channel	SD_OFF_Cr[7:0]; adjusts the hue by selecting the offset for the Cr channel	0	0	0	0	0	0	0	0	−312 mV offset applied to the Cr channel	
			1	0	0	0	0	0	0	0	0 mV offset applied to the Cr channel	
			1	1	1	1	1	1	1	1	+312 mV offset applied to the Cr channel	
0xE3	SD saturation Cb channel	SD_SAT_Cb[7:0]; adjusts the saturation by affecting gain on the Cb channel	0	0	0	0	0	0	0	0	Gain on Cb channel = −42 dB	
			1	0	0	0	0	0	0	0	Gain on Cb channel = 0 dB	
			1	1	1	1	1	1	1	1	Gain on Cb channel = +6 dB	
0xE4	SD saturation Cr channel	SD_SAT_Cr[7:0]; adjusts the saturation by affecting gain on the Cr channel	0	0	0	0	0	0	0	0	Gain on Cr channel = −42 dB	
			1	0	0	0	0	0	0	0	Gain on Cr channel = 0 dB	
			1	1	1	1	1	1	1	1	Gain on Cr channel = +6 dB	
0xE5	NTSC V bit begin	NVBEG[4:0]; number of lines after line count rollover to set VS high				0	0	1	0	1	NTSC default (ITU-R BT.656)	
		NVBEGSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		NVBEGDELE; delay V bit going high by one line relative to NVBEG (even field)		0							No delay	
				1							Additional delay by one line	
		NVBEGDELO; delay V bit going high by one line relative to NVBEG (odd field)	0								No delay	
			1								Additional delay by one line	
0xE6	NTSC V bit end	NVEND[4:0]; number of lines after ICOUNT rollover to set VS low				0	0	1	0	0	NTSC default (ITU-R BT.656)	
		NVENDSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		NVENDDELE; delay V bit going low by one line relative to NVEND (even field)		0							No delay	
				1							Additional delay by one line	
		NVENDDELO; delay V bit going low by one line relative to NVEND (odd field)	0								No delay	
			1								Additional delay by one line	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0xE7	NTSC F bit toggle	NFTOG[4:0]; number of lines after lCOUNT rollover to toggle F signal				0	0	0	1	1	NTSC default	
		NFTOGSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		NFTOGDELE; delay F transition by one line relative to NFTOG (even field)		0							No delay	
				1							Additional delay by one line	
		NFTOGDELO; delay F transition by one line relative to NFTOG (odd field)	0								No delay	
			1								Additional delay by one line	
0xE8	PAL V bit begin	PVBEG[4:0]; number of lines after line count rollover to set VS high				0	0	1	0	1	PAL default (ITU-R BT.656)	
		PVBEGSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		PVBEGDELE; delay V bit going high by one line relative to PVBEG (even field)		0							No delay	
				1							Additional delay by one line	
		PVBEGDELO; delay V bit going high by one line relative to PVBEG (odd field)	0								No delay	
			1								Additional delay by one line	
0xE9	PAL V bit end	PVEND[4:0]; number of lines after line count rollover to set VS low.				1	0	1	0	0	PAL default (ITU-R BT.656)	
		PVENDSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		PVENDDELE; delay V bit going low by one line relative to PVEND (even field)		0							No delay	
				1							Additional delay by one line	
		PVENDDELO; delay V bit going low by one line relative to PVEND (odd field)	0								No delay	
			1								Additional delay by one line	
0xEA	PAL F bit toggle	PFTOG[4:0]; number of lines after line count rollover to toggle F signal				0	0	0	1	1	PAL default (ITU-R BT.656)	
		PFTOGSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		PFTOGDELE; delay F transition by one line relative to PFTOG (even field)		0							No delay	
				1							Additional delay by one line	
			0								No delay	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
		PFTOGDELO; delay F transition by one line relative to PFTOG (odd field)	0								No delay	
			1								Additional delay by one line	
0xEB	Vblank Control 1	PVBIELCM[1:0]; PAL VBI even field line control							0	0	VBI ends one line earlier (Line 335)	Controls position of first active (comb filtered) line after VBI on even field in PAL
									0	1	ITU-R BT.470 compliant (Line 336)	
									1	0	VBI ends one line later (Line 337)	
									1	1	VBI ends two lines later (Line 338)	
		PVBIOLCM[1:0]; PAL VBI odd field line control					0	0			VBI ends one line earlier (Line 22)	Controls position of first active (comb filtered) line after VBI on odd field in PAL
							0	1			ITU-R BT.470 compliant (Line 23)	
							1	0			VBI ends one line later (Line 24)	
							1	1			VBI ends two lines later (Line 25)	
		NVBIELCM[1:0]; NTSC VBI even field line control			0	0					VBI ends one line earlier (Line 282)	Controls position of first active (comb filtered) line after VBI on even field in NTSC
					0	1					ITU-R BT.470 compliant (Line 283)	
					1	0					VBI ends one line later (Line 284)	
					1	1					VBI ends two lines later (Line 285)	
		NVBIOLCM[1:0]; NTSC VBI odd field line control	0	0							VBI ends one line earlier (Line 20)	Controls position of first active (comb filtered) line after VBI on odd field in NTSC
			0	1							ITU-R BT.470 compliant (Line 21)	
			1	0							VBI ends one line later (Line 22)	
			1	1							VBI ends two lines later (Line 23)	
0xEC	Vblank Control 2	PVBIECCM[1:0]; PAL VBI even field color control							0	0	Color output beginning Line 335	Controls the position of first line that outputs color after VBI on even field in PAL
									0	1	ITU-R BT.470 compliant color output beginning Line 336	
									1	0	Color output beginning Line 337	
									1	1	Color output beginning Line 338	
		PVBIOCCM[1:0]; PAL VBI odd field color control					0	0			Color output beginning Line 22	Controls the position of first line that outputs color after VBI on odd field in PAL
							0	1			ITU-R BT.470 compliant color output beginning Line 23	
							1	0			Color output beginning Line 24	
							1	1			Color output beginning Line 25	
		NVBIECCM[1:0]; NTSC VBI even field color control			0	0					Color output beginning Line 282	Controls the position of first line that outputs color after VBI on even field in NTSC
					0	1					ITU-R BT.470 compliant color output beginning Line 283	
					1	0					VBI ends one line later (Line 284)	
					1	1					Color output beginning Line 285	
		NVBIOCCM[1:0]; NTSC VBI odd field color control	0	0							Color output beginning Line 20	Controls the position of first line that outputs color after VBI on odd field in NTSC
			0	1							ITU-R BT.470 compliant color output beginning Line 21	
			1	0							Color output beginning Line 22	
			1	1							Color output beginning Line 23	
0xF3	AFE Control 1	AA_FILT_EN[3:0] antialiasing filter enable								0	Antialiasing Filter 1 disabled	AA_FILT_MAN_OVR must be enabled to change settings defined by INSEL[4:0]
										1	Antialiasing Filter 1 enabled	
									0		Antialiasing Filter 2 disabled	
									1		Antialiasing Filter 2 enabled	
								0			Antialiasing Filter 3 disabled	
								1			Antialiasing Filter 3 enabled	
							0				Antialiasing Filter 4 enabled	
							1				Antialiasing Filter 4 enabled	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
		AA_FILT_MAN_OVR; antialiasing filter override				0					Override disabled	
						1					Override enabled	
		Reserved	0	0	0							
0xF4	Drive strength	DR_STR_S[1:0]; selects the drive strength for the sync output signals							0	0	Low drive strength (1×)	The low drive strength settings for DR_STR, DR_STR_C and DR_STR_S are not recommended for the optimal performance of the ADV7281A, and ADV7282A devices.
									0	1	Medium low drive strength (2×)	
									1	0	Medium high drive strength (3×)	
									1	1	High drive strength (4×)	
		DR_STR_C[1:0]; selects the drive strength for the clock output signal					0	0			Low drive strength (1×)	
							0	1			Medium low drive strength (2×)	
							1	0			Medium high drive strength (3×)	
							1	1			High drive strength (4×)	
		DR_STR[1:0]; selects the drive strength for the data output signals; can be increased or decreased for EMC or crosstalk reasons			0	0					Low drive strength (1×)	
					0	1					Medium low drive strength (2×)	
					1	0					Medium high drive strength (3×)	
					1	1					High drive strength (4×)	
		Reserved		X								
		GLITCH_FILT_BYP	0									
			1									
0xF8	IF_COMP_ CONTROL	IFFILTSEL[2:0]; IF filter selection for PAL and NTSC						0	0	0	Bypass mode	0 dB
											2 MHz NTSC filters	
								0	0	1	−3 dB	
								0	1	0	−6 dB	
								0	1	1	−10 dB	
								1	0	0	Reserved	
											3 MHz PAL filters	
								1	0	1	−2 dB	
								1	1	0	−5 dB	
								1	1	1	−7 dB	
		Reserved	0	0	0	0	0					
0xF9	VS mode control	EXTEND_VS_MAX_ FREQ								0	Limits maximum VS frequency to 66.25 Hz (475 lines/frame)	
										1	Limits maximum VS frequency to 70.09 Hz (449 lines/frame)	
		EXTEND_VS_MIN_ FREQ							0		Limits minimum VS frequency to 42.75 Hz (731 lines/frame)	
									1		Limits minimum VS frequency to 39.51 Hz (791 lines/frame)	
		VS_COAST_ MODE[1:0]					0	0			Autocoast mode	This value forces the video standard output during free run mode
							0	1			576i, 50 Hz coast mode	
							1	0			480i, 60 Hz coast mode	
							1	1			Reserved	
		Reserved	0	0	0	0						
0xFB	Peaking gain	PEAKING_GAIN[7:0]; luma peaking gain	0	1	0	0	0	0	0	0	Increases/decreases the gain for high frequency portions of the video signal	
0xFC	DNR Noise Threshold 2	DNR_TH2[7:0]	0	0	0	0	0	1	0	0	Specifies the maximum luma edge that is interpreted as noise and therefore blanked	

User Sub Map			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0xFD	VPP slave address	Reserved								0	Reserved	
		VPP_SLAVE_ ADDR[6:0]	0	0	0	0	0	0	0		Programs the I²C address of the video post processor (VPP) map	Applies only to the ADV7280A, ADV7280A-M, and ADV7282A-M models. The VPP map cannot be accessed when this register is set to 0x00. Analog devices recommended scripts set this register to 0x84.
0xFE	CSI Tx slave address	Reserved								0	Reserved	
		CSI_TX_SLAVE_ ADDR[6:0]	0	0	0	0	0	0	0		Programs the I²C address of the MIPI CSI-2 TX map	Applies only to the ADV7280A-M, ADV7281A-M and ADV7282A-M models. The MIPI CSI-2 TX map cannot be accessed when this register is set to 0x00. Analog devices recommended script sets this register to 0x88.

[1] X means don't care.

USER SUB MAP 2 DESCRIPTION

To access the registers listed in Table 93, SUB_USR_EN[1:0] in Register Address 0x0E, user sub map, must be programmed to 10. The gray shading is the default.

Table 93. User Sub Map 2 Register Map Descriptions

User Sub Map 2			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x80	ACE Control 1	Reserved		0	0	0	0	0	0	0	Reserved.	
		ACE_ENABLE	0								Disables ACE	
			1								Enables ACE	
0x83	ACE Control 4	ACE_LUMA_GAIN[4:0]				0	1	1	0	1	Set ACE luma autocontrast level to default value. 5b'00000 minimum value … 5b'11111 maximum value	When ACE_ENABLE is set to 1
		Reserved	0	0	0							
0x84	ACE Control 5	ACE_CHROMA_GAIN[3:0]					1	0	0	0	Sets ACE color autosaturation level 4b'0000 minimum value … 4b'1111 maximum value	
		ACE_CHROMA_MAX[3:0]	1	0	0	0					Sets maximum threshold for ACE color saturation level 4b'0000 = minimum value … 4b'1111 = maximum value	
0x85	ACE Control 6	ACE_GAMMA_GAIN[3:0]					1	0	0	0	Sets further contrast enhancement 4b'0000 = minimum value … 4b'1111 = maximum value	
		ACE_RESPONSE_SPEED[3:0]	1	1	1	1					Set speed of ACE response 4b'0000 slowest value … 4b'1111 fastest value	
0x92	Dither control	BR_DITHER_MODE								0	8-bit to 6-bit downdither disabled	
										1	8-bit to 6-bit downdither enabled	
		Reserved	0	0	0	0	0	0	0			

User Sub Map 2			Bits[1]									
Addr	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0xD9	MIN_MAX_0	MIN_THRESH_Y[7:0]	0	0	0	0	0	0	0	0	Selects the minimum threshold for the incoming luma video signal.	
0xDA	MIN_MAX_1	MAX_THRESH_Y[7:0]	1	1	1	1	1	1	1	1	Selects the maximum threshold for the incoming luma video signal.	
0xDB	MIN_MAX_2	MIN_THRESH_C[7:0]	0	0	0	0	0	0	0	0	Selects the minimum threshold for the incoming chroma video signal.	
0xDC	MIN_MAX_3	MAX_THRESH_C[7:0]	1	1	1	1	1	1	1	1	Selects the maximum threshold for the incoming chroma video signal.	
0xDD	MIN_MAX_4	MAX_SAMPLES_ALLOWED_Y[3:0]					1	1	0	0	Selects the number of maximum luma samples allowed in a given window before an interrupt is triggered.	
		MIN_SAMPLES_ALLOWED_Y[3:0]	1	1	0	0					Selects the number of minimum luma samples allowed in a given window before an interrupt is triggered.	
0xDE	Min Max 5	MAX_SAMPLES_ALLOWED_C[3:0]					1	1	0	0	Selects the number of maximum chroma samples allowed in a given window before an interrupt is triggered.	
		MIN_SAMPLES_ALLOWED_C[3:0]	1	1	0	0					Selects the number of minimum chroma samples allowed in a given window before an interrupt is triggered.	
0xE0	FL control	FL_ENABLE								0	Fast lock mode not enabled	
										1	Enables fast lock mode	
		Reserved	0	0	0	0	0	0	0			See Subaddress 0xE5 for least significant bits
0xE1	Y Average 0	LINE_START[8:1]	0	0	0	1	0	0	0	1	Selects starting line for field averaging	See Subaddress 0xE5 for least significant bits
0xE2	Y Average 1	LINE_END[8:1]	1	0	0	0	1	0	0	0	Selects end line for field averaging	
0xE3	Y Average 2	SAMPLE_START[9:2]	0	0	0	1	0	1	1	1	Selects starting sample for line averaging	
0xE4	Y Average 3	SAMPLE_END[9:2]	1	1	0	1	0	1	1	1	Selects end sample for line averaging	
0xE5	Y Average 4	LINE_START[0]								1		
		LINE_END[0]							1			
		Reserved					0	0				
		SAMPLE_START[1:0]			1	0						
		SAMPLE_END[1:0]	0	0								
0xE6	Y Average 5	CAPTURE_VALUE								0	Trigger that stores the readback value	
		Y_AVG_FILT_EN							0		Enable low pass filtering of the y averaged data	
		Y_AVG_TIME_CONST[2:0]				1	0	0			Selects the filter cutoff to be used for filtering the y averaged data. 3'b1xx = least filtered 3'b000 = next least … 3'b011 = heavily filtered	
		Reserved	0	0	0							These are read only bits
0xE7	Y average data MSB	Y_AVERAGE[9:2]	X	X	X	X	X	X	X	X	Contains the averaged video data	
0xE8	Y average data LSB	Y_AVERAGE[1:0]							X	X		

[1] X means don't care.

INTERRUPT/VDP SUB MAP DESCRIPTION

To access the registers listed in Table 94, SUB_USR_EN[1:0] in Register Address 0x0E, user sub map, must be programmed to 01. The gray shading is the default.

Table 94. Interrupt/VDP Sub Map Register Descriptions

Interrupt/VDP Sub Map			Bits[1]									
Address	**Register Name**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Functionality**	**Comments**
0x40	Interrupt Configuration 1	INTRQ_OP_SEL[1:0]; interrupt drive level select							0	0	Open drain	
									0	1	Drive low when active	
									1	0	Drive high when active	
									1	1	Reserved	
		MPU_STIM_INTRQ; manual interrupt set mode						0			Manual interrupt mode disabled	
								1			Manual interrupt mode enabled	
		Reserved					X				Not used	
		MV_INTRQ_SEL[1:0]; Rovi interrupt select			0	0					Reserved	
					0	1					Pseudo sync only	
					1	0					Color stripe only	
					1	1					Pseudo sync or color stripe	
		INTRQ_DUR_SEL[1:0]; interrupt duration select	0	0							3 XTAL periods	
			0	1							15 XTAL periods	
			1	0							63 XTAL periods	
			1	1							Active until cleared	
0x42	Interrupt Status 1 (read only)	SD_LOCK_Q								0	No change	These bits can be cleared or masked in Register 0x43 and Register 0x44, respectively
										1	SD input has caused the decoder to go from an unlocked state to a locked state	
		SD_UNLOCK_Q							0		No change	
									1		SD input has caused the decoder to go from a locked state to an unlocked state	
		Reserved				X	X	X				
		SD_FR_CHNG_Q			0						No change	
					1						Denotes a change in the free run status	
		MV_PS_CS_Q		0							No change	
				1							Pseudo sync/color striping detected; see Register 0x40 MV_INTRQ_SEL[1:0] for selection	
		Reserved	X									
0x43	Interrupt Clear 1 (write only)	SD_LOCK_CLR								0	Do not clear	
										1	Clears SD_LOCK_Q bit	
		SD_UNLOCK_CLR							0		Do not clear	
									1		Clears SD_UNLOCK_Q bit	
		Reserved				0	0	0			Not used	
		SD_FR_CHNG_CLR			0						Do not clear	
					1						Clears SD_FR_CHNG_Q bit	
		MV_PS_CS_CLR		0							Do not clear	
				1							Clears MV_PS_CS_Q bit	
		Reserved	X								Not used	

Interrupt/VDP Sub Map			Bits[1]									
Address	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x44	Interrupt Mask 1 (read/write)	$\overline{\text{SD\_LOCK\_MSK}}$								0	Masks SD_LOCK_Q bit	
										1	Unmasks SD_LOCK_Q bit	
		$\overline{\text{SD\_UNLOCK\_MSK}}$							0		Masks SD_UNLOCK_Q bit	
									1		Unmasks SD_UNLOCK_Q bit	
		Reserved				0	0	0			Not used	
		$\overline{\text{SD\_FR\_CHNG\_MSK}}$			0						Masks SD_FR_CHNG_Q bit	
					1						Unmasks SD_FR_CHNG_Q bit	
		$\overline{\text{MV\_PS\_CS\_MSK}}$		0							Masks MV_PS_CS_Q bit	
				1							Unmasks MV_PS_CS_Q bit	
		Reserved	X								Not used	
0x45	Raw Status 2 (read only)	CCAPD								0	No CCAPD data detected—VBI System 2	These bits are status bits only; they cannot be cleared or masked; use Register 0x46
										1	CCAPD data detected—VBI System 2	
		Reserved					X	X	X			
		EVEN_FIELD				0					Current SD field is odd numbered	
						1					Current SD field is even numbered	
		CHX_MIN_MAX_INTRQ			0						If the input to the ADC is within the correct range this is 0	
					1						If the input to the ADC is outside the range, this is set to 1; the range is set by User Sub Map 2	
		Reserved		X							Not used	
		MPU_STIM_INTRQ	0								MPU_STIM_INTRQ = 0	
			1								MPU_STIM_INTRQ = 1	
0x46	Interrupt Status 2 (read only)	CCAPD_Q								0	Closed captioning not detected in the input video signal—VBI System 2	These bits can be cleared or masked by Register 0x47 and Register 0x48, respectively; note that the interrupt in Register 0x46 for the CCAP, CGMS, and WSS data uses the Mode 1 data slicer
										1	Closed captioning data detected in the video input signal—VBI System 2	
		Reserved					X	X	X		Not used	
		SD_FIELD_CHNGD_Q				0					SD signal has not changed field from odd to even or vice versa	
						1					SD signal has changed field from odd to even or vice versa	
		Reserved		X	X						Not used	
		MPU_STIM_INTRQ_Q	0								Manual interrupt not set	
			1								Manual interrupt set	
0x47	Interrupt Clear 2 (write only)	CCAPD_CLR								0	Do not clear—VBI System 2	Note that interrupt in Register 0x46 for the CCAP, CGMS, and WSS data uses the Mode 1 data slicer
										1	Clears CCAPD_Q bit—VBI System 2	
		Reserved					X	X	X		Not used	
		SD_FIELD_CHNGD_CLR				0					Do not clear	
						1					Clears SD_FIELD_CHNGD_Q bit	
		CHX_MIN_MAX_INTRQ_CLR			0						Do not clear	
					1						Clears CHX_MIN_MAX_INTRQ bit	
		Reserved		X							Not used	
		MPU_STIM_INTRQ_CLR	0								Do not clear	
			1								Clears MPU_STIM_INTRQ_Q bit	

Interrupt/VDP Sub Map			Bits[1]									
Address	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x48	Interrupt Mask 2 (read/write)	$\overline{\text{CCAPD\_MSK}}$								0	Masks CCAPD_Q bit—VBI System 2	The interrupt in Register 0x46 for the CCAP, CGMS, and WSS data uses the Mode 1 data slicer
										1	Unmasks CCAPD_Q bit—VBI System 2	
		Reserved					0	0	0		Not used	
		$\overline{\text{SD\_FIELD\_CHNGD\_MSK}}$				0					Masks SD_FIELD_CHNGD_Q bit	
						1					Unmasks SD_FIELD_CHNGD_Q bit	
		$\overline{\text{CHX\_MIN\_MAX\_INTRQ\_MSKB}}$			0						Masks CHX_MIN_MAX_INTRQ bit	
					1						Unmasks CHX_MIN_MAX_INTRQ bit	
		Reserved		0							Not used	
		$\overline{\text{MPU\_STIM\_INTRQ\_MSK}}$	0								Masks MPU_STIM_INTRQ_Q bit	
			1								Unmasks MPU_STIM_INTRQ_Q bit	
0x49	Raw Status 3 (read only)	SD_OP_50Hz; SD 60 Hz/50 Hz frame rate at output								0	SD 60 Hz signal output	These bits are status bits only; they cannot be cleared or masked; use Register 0x4A
										1	SD 50 Hz signal output	
		SD_V_LOCK							0		SD vertical sync lock is not established	
									1		SD vertical sync lock established	
		SD_H_LOCK						0			SD horizontal sync lock is not established	
								1			SD horizontal sync lock established	
		Reserved					X				Not used	
		SCM_LOCK				0					SECAM lock is not established	
						1					SECAM lock established	
		Reserved	X	X	X						Not used	
0x4A	Interrupt Status 3 (read only)	SD_OP_CHNG_Q; SD 60 Hz/50 Hz frame rate at output								0	No change in SD signal standard detected at the output	These bits can be cleared and masked by Register 0x4B and Register 0x4C, respectively
										1	A change in SD signal standard is detected at the output	
		SD_V_LOCK_CHNG_Q							0		No change in SD VSYNC lock status	
									1		SD VSYNC lock status has changed	
		SD_H_LOCK_CHNG_Q						0			No change in HSYNC lock status	
								1			SD HSYNC lock status has changed	
		SD_AD_CHNG_Q; SD autodetect changed					0				No change in AD_RESULT[2:0] bits in Status 1 register	
							1				AD_RESULT[2:0] bits in Status 1 register have changed	
		SCM_LOCK_CHNG_Q; SECAM lock				0					No change in SECAM lock status	
						1					SECAM lock status has changed	

Interrupt/VDP Sub Map			Bits[1]									
Address	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
		PAL_SW_LK_CHNG_Q			0						No change in PAL swinging burst lock status	
					1						PAL swinging burst lock status has changed	
		Reserved	X	X							Not used	
0x4B	Interrupt Clear 3 (write only)	SD_OP_CHNG_CLR								0	Do not clear	
										1	Clears SD_OP_CHNG_Q bit	
		SD_V_LOCK_CHNG_CLR							0		Do not clear	
									1		Clears SD_V_LOCK_CHNG_Q bit	
		SD_H_LOCK_CHNG_CLR						0			Do not clear	
								1			Clears SD_H_LOCK_CHNG_Q bit	
		SD_AD_CHNG_CLR					0				Do not clear	
							1				Clears SD_AD_CHNG_Q bit	
		SCM_LOCK_CHNG_CLR				0					Do not clear	
						1					Clears SCM_LOCK_CHNG_Q bit	
		PAL_SW_LK_CHNG_CLR			0						Do not clear	
					1						Clears PAL_SW_LK_CHNG_Q bit	
		Reserved	X	X							Not used	
0x4C	Interrupt Mask 3 (read/write)	$\overline{\text{SD\_OP\_CHNG\_MSK}}$								0	Masks SD_OP_CHNG_Q bit	
										1	Unmasks SD_OP_CHNG_Q bit	
		$\overline{\text{SD\_V\_LOCK\_CHNG\_MSK}}$							0		Masks SD_V_LOCK_CHNG_Q bit	
									1		Unmasks SD_V_LOCK_CHNG_Q bit	
		$\overline{\text{SD\_H\_LOCK\_CHNG\_MSK}}$						0			Masks SD_H_LOCK_CHNG_Q bit	
								1			Unmasks SD_H_LOCK_CHNG_Q bit	
		$\overline{\text{SD\_AD\_CHNG\_MSK}}$					0				Masks SD_AD_CHNG_Q bit	
							1				Unmasks SD_AD_CHNG_Q bit	
		$\overline{\text{SCM\_LOCK\_CHNG\_MSK}}$				0					Masks SCM_LOCK_CHNG_Q bit	
						1					Unmasks SCM_LOCK_CHNG_Q bit	
		$\overline{\text{PAL\_SW\_LK\_CHNG\_MSK}}$			0						Masks PAL_SW_LK_CHNG_Q bit	
					1						Unmasks PAL_SW_LK_CHNG_Q bit	
		Reserved	X	X							Not used	
0x4E	Interrupt Status 4 (read only)	VDP_CCAPD_Q								0	Closed captioning not detected	These bits can be cleared and masked by Register 0x4F and Register 0x50, respectively; note that an interrupt in Register 0x4E for the CCAP, CGMS, and WSS data uses the VDP data slicer
										1	Closed captioning detected	
		Reserved							X			
		VDP_CGMS_WSS_CHNGD_Q; see Address 0x9C, Bit 4, of user sub map to determine whether interrupt is issued for a change in detected data or for when data is detected, regardless of content						0			CGMS/WSS data is not changed/not available	
								1			CGMS/WSS data is changed/available	
		Reserved					X					
		Reserved				X						
		Reserved			X							
		Reserved		X								
		Reserved	X									

Interrupt/VDP Sub Map			Bits[1]									
Address	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x4F	Interrupt Clear 4 (write only)	VDP_CCAPD_CLR								0	Do not clear	In Register 0x4E, CCAP/CGMS/WSS data uses VDP data slicer
										1	Clears VDP_CCAPD_Q	
		Reserved							0			
		VDP_CGMS_WSS_CHNGD_CLR						0			Do not clear	
								1			Clears VDP_CGMS_WSS_CHNGD_Q	
		Reserved					0					
		Reserved				0						
		Reserved			0							
		Reserved		0							Do not clear	
		Reserved	0									
		VDP_CCAPD_CLR								0	Do not clear	
0x50	Interrupt Mask 4	$\overline{\text{VDP\_CCAPD\_MSK}}$								0	Masks VDP_CCAPD_Q	Note that an interrupt in Register 0x4E for the CCAP, CGMS, and WSS data uses the VDP data slicer
										1	Unmasks VDP_CCAPD_Q	
		Reserved							0			
		$\overline{\text{VDP\_CGMS\_WSS\_CHNGD\_MSK}}$						0			Masks VDP_CGMS_WSS_CHNGD_Q	
								1			Unmasks VDP_CGMS_WSS_CHNGD_Q	
		Reserved					0					
		Reserved				0						
		Reserved			0							
		Reserved		0								
		Reserved	0									
0x51	Interrupt Latch 0 (read only)	CR_CHANNEL_MAX_VIOLATION								0	Cr value is below programmed maximum value	This register is cleared by CHX_MIN_MAX_INTRQ_CLR
										1	Cr value is above programmed maximum value	
		CR_CHANNEL_MIN_VIOLATION							0		Cr value is above programmed minimum value	
									1		Cr value is below programmed minimum value	
		CB_CHANNEL_MAX_VIOLATION						0			Cb value is below programmed maximum value	
								1			Cb value is above programmed maximum value	
		CB_CHANNEL_MIN_VIOLATION					0				Cb value is above programmed minimum value	
							1				Cb value is below programmed minimum value	
		Y_CHANNEL_MAX_VIOLATION				0					Y value is below programmed maximum value	
						1					Y value is above programmed maximum value	
		Y_CHANNEL_MIN_VIOLATION			0						Y value is above programmed minimum value	
					1						Y value is below programmed minimum value	
		Reserved	0	0								

Interrupt/VDP Sub Map			Bits[1]									
Address	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x53	Interrupt Status 5 (read only)	Reserved								X		
		DIAG_TRI1_L1							0		Voltage higher than DIAG1_SLICE_LEVEL not detected on DIAG1 pin	See DIAG1_SLICE_LEVEL (user sub map, Register 0x5D [4:2]) and DIAG2_SLICE_LEVEL (user sub map, Register 0x5E, Bits [4:2]). These bits can be cleared or masked in Register 0x54 and Register 0x55, respectively.
									1		Voltage higher than DIAG1_SLICE_LEVEL detected on DIAG1 pin	
		Reserved						X				
		DIAG_TRI2_L1					0				Voltage higher than DIAG2_SLICE_LEVEL not detected on DIAG2 pin	
							1				Voltage higher than DIAG2_SLICE_LEVEL detected on DIAG2 pin	
		Reserved	X	X	X	X						
0x54	Interrupt Clear 5 (write only)	Reserved								0		
		DIAG_TRI1_L1_CLR							0		Do not clear DIAG_TRI1_L1	
									1		Clear DIAG_TRI1_L1	
		Reserved						0				
		DIAG_TRI2_L1_CLR					0				Do not clear DIAG_TRI2_L1	
							1				Clear DIAG_TRI2_L1	
		Reserved	0	0	0	0						
0x55	Interrupt Mask 5	Reserved								0		
		DIAG_TRI1_L1_MSK							0		Masks DIAG_TRI1_L1	
									1		Unmasks DIAG_TRI1_L1	
		Reserved						0				
		DIAG_TRI2_L1_MSK					0				Masks DIAG_TRI2_L1	
							1				Unmasks DIAG_TRI2_L1	
		Reserved	0	0	0	0						
0x60	VDP_CONFIG_1	VDP_TTXT_TYPE_MAN[1:0]							0	0	PAL: Teletext-ITU-BT.653-625/ 50-A, NTSC: reserved	
									0	1	PAL: Teletext-ITU-BT.653-625/ 50-B (WST), NTSC: Teletext-ITU-BT.653-525/ 60-B	
									1	0	PAL: Teletext-ITU-BT.653-625/ 50-C, NTSC: Teletext-ITU-BT.653-525/60-C, orEIA516 (NABTS)	
									1	1	PAL: Teletext-ITU-BT.653-625/ 50-D, NTSC: Teletext-ITU-BT.653-525/60-D	
		VDP_TTXT_TYPE_MAN_ENABLE						0			User programming of teletext type disabled	
								1			User programming of teletext type enabled	
		WST_PKT_DECODE_DISABLE					0				Enables hamming decoding of WST packets	
							1				Disables hamming decoding of WST packets	
		Reserved	1	0	0	0						
0x62	VDP_ADF_ CONFIG_1	ADF_DID[4:0]				1	0	1	0	1	User-specified DID sent in the ancillary data stream with VDP decoded data	
		ADF_MODE[1:0]		0	0						Nibble mode	Sets whether ancillary data output mode in byte mode or nibble mode
				0	1						Byte mode, no code restrictions	
				1	0						Byte mode with 0x00 and 0xFF prevented	
				1	1						Reserved	
		ADF_ENABLE	0								Disables insertion of VBI decoded data into ancillary 656 stream	
			1								Enables insertion of VBI decoded data into ancillary 656 stream	

Interrupt/VDP Sub Map			Bits[1]									
Address	**Register Name**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Functionality**	**Comments**
0x63	VDP_ADF_ CONFIG_2	ADF_SDID[5:0]			1	0	1	0	1	0	User specified SDID sent in the ancillary data stream with VDP decoded data	
		Reserved		X								
		DUPLICATE_ADF	0								Ancillary data packet is spread across the Y and C data streams	
			1								Ancillary data packet is duplicated on the Y and C data streams	
0x64	VDP_LINE_00E	VBI_DATA_P318[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 318 (PAL), NTSC—not applicable	
		Reserved		0	0	0						
		MAN_LINE_PGM	0								Decode default VDP standards on the expected lines.	
			1								Manually program the VBI standard to be decoded on each line.	If set to 1, all VBI_DATA_Px_Ny bits can be set as desired
0x65	VDP_LINE_00F	VBI_DATA_P319_N286[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 319 (PAL), Line 286 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P6_N23[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 6 (PAL), Line 23 (NTSC)	
0x66	VDP_LINE_010	VBI_DATA_P320_N287[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 320 (PAL), Line 287 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P7_N24[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 7 (PAL), Line 24 (NTSC)	
0x67	VDP_LINE_011	VBI_DATA_P321_N288[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 321 (PAL), Line 288 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P8_N25[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 8 (PAL), Line 25 (NTSC)	
0x68	VDP_LINE_012	VBI_DATA_P322[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 322 (PAL), NTSC—not applicable	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P9[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 9 (PAL), NTSC—not applicable	
0x69	VDP_LINE_013	VBI_DATA_P323[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 323 (PAL), NTSC—not applicable	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P10[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 10 (PAL), NTSC—not applicable	
0x6A	VDP_LINE_014	VBI_DATA_P324_N272[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 324 (PAL), Line 272 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P11[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 11 (PAL); NTSC—not applicable	

Interrupt/VDP Sub Map			Bits[1]									
Address	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x6B	VDP_LINE_015	VBI_DATA_P325_N273[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 325 (PAL), Line 273 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P12_N10[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 12 (PAL), Line 10 (NTSC)	
0x6C	VDP_LINE_016	VBI_DATA_P326_N274[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 326 (PAL), Line 274 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P13_N11[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 13 (PAL), Line 11 (NTSC)	
0x6D	VDP_LINE_017	VBI_DATA_P327_N275[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 327 (PAL), Line 275 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P14_N12[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 14 (PAL), Line 12 (NTSC)	
0x6E	VDP_LINE_018	VBI_DATA_P328_N276[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 328 (PAL), Line 276 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P15_N13[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 15 (PAL), Line 13 (NTSC)	
0x6F	VDP_LINE_019	VBI_DATA_P329_N277[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 329 (PAL), Line 277 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P16_N14[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 16 (PAL), Line 14 (NTSC)	
0x70	VDP_LINE_01A	VBI_DATA_P330_N278[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 330 (PAL), Line 278 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P17_N15[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 17 (PAL), Line 15 (NTSC)	
0x71	VDP_LINE_01B	VBI_DATA_P331_N279[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 331 (PAL), Line 279 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P18_N16[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 18 (PAL), Line 16 (NTSC)	
0x72	VDP_LINE_01C	VBI_DATA_P332_N280[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 332 (PAL), Line 280 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P19_N17[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 19 (PAL), Line 17 (NTSC)	
0x73	VDP_LINE_01D	VBI_DATA_P333_N281[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 333 (PAL), Line 281 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P20_N18[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 20 (PAL), Line 18 (NTSC)	
0x74	VDP_LINE_01E	VBI_DATA_P334_N282[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 334 (PAL), Line 282 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective

Interrupt/VDP Sub Map			Bits[1]									
Address	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
		VBI_DATA_P21_N19[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 21 (PAL), Line 19 (NTSC)	
0x75	VDP_LINE_01F	VBI_DATA_P335_N283[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 335 (PAL), Line 283 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P22_N20[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 22 (PAL), Line 20 (NTSC)	
0x76	VDP_LINE_020	VBI_DATA_P336_N284[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 336 (PAL), Line 284 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P23_N21[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 23 (PAL), Line 21 (NTSC)	
0x77	VDP_LINE_021	VBI_DATA_P337_N285[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 337 (PAL), Line 285 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P24_N22[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 24 (PAL), Line 22 (NTSC)	
0x78	VDP_STATUS (read only)	CC_AVL								0	Closed captioning not detected	CC_CLEAR resets the CC_AVL bit
										1	Closed captioning is detected	
		CC_EVEN_FIELD							0		Closed captioning decoded from odd field	
									1		Closed captioning decoded from even field	
		CGMS_WSS_AVL						0			CGMS/WSS is not detected	CGMS_WSS_CLEAR resets the CGMS_WSS_AVL bit
								1			CGMS/WSS detected	
		Reserved		0	0	0	0					
		TTXT_AVL	0								Teletext not detected	
			1								Teletext detected	
	VDP_STATUS_ CLEAR (write only)	CC_CLEAR								0	Does not reinitialize the CCAP readback registers	This is a self clearing bit
										1	Reinitializes the CCAP readback registers	
		Reserved							0			
		CGMS_WSS_CLEAR						0			Does not reinitialize the CGMS/WSS readback registers	This is a self clearing bit
								1			Reinitializes the CGMS/WSS readback registers	
		Reserved	0	0	0	0	0					

Interrupt/VDP Sub Map			Bits[1]									
Address	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x79	VDP_CCAP_DATA_0 (read only)	CCAP_BYTE_1[7:0]	X	X	X	X	X	X	X	X	Decoded Byte 1 of CCAP	
0x7A	VDP_CCAP_DATA_1 (read only)	CCAP_BYTE_2[7:0]	X	X	X	X	X	X	X	X	Decoded Byte 2 of CCAP	
0x7D	VDP_CGMS_WSS_DATA_0 (read only)	CGMS_CRC[5:2]					X	X	X	X	Decoded CRC sequence for CGMS	
		Reserved	0	0	0	0						
0x7E	VDP_CGMS_WSS_DATA_1 (read only)	CGMS_WSS[13:8]			X	X	X	X	X	X	Decoded CGMS/WSS data	
		CGMS_CRC[1:0]	X	X							Decoded CRC sequence for CGMS	
0x7F	VDP_CGMS_WSS_DATA_2 (read only)	CGMS_WSS[7:0]	X	X	X	X	X	X	X	X	Decoded CGMS/WSS data	
0x9C	VDP_OUTPUT_SEL	Reserved					0	0	0	0		
		WSS_CGMS_CB_CHANGE				0					Disable content-based updating of CGMS and WSS data	The available bit shows the availability of data only when its content has changed
						1					Enable content-based updating of CGMS and WSS data	
		Reserved	0	0	0							

[1] X means don't care.

VPP MAP DESCRIPTION

To access the registers listed in Table 95, the user must set the VPP I²C device address by writing to VPP_SLAVE_ADDR[6:0]. VPP_SLAVE_ADDR[6:0] can be found in Register 0xFD, user sub map. Analog devices recommended scripts set the VPP I²C device address to 0x84. The default bits are indicated by the gray shading.

Table 95. VPP Map Register Descriptions

VPP Map			Bits									
Address	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x41	DEINT_RESET	DEINT_RESET								0		
										1	Reset the I²P core	
		Reserved	0	0	0	0	0	0	0		Reserved	
0x55	I2C_DEINT_ENABLE	Reserved		0	0	0	0	0	0	0	Reserved	
		I2C_DEINT_ENABLE	0								Disable I²P converter	For the I²P converter to operate correctly, the ADV_TIMING_MODE_EN bit must be set to 1. Also changes to the output timing video are needed. Refer to the Analog devices recommended scripts.
			1								Enable I²P converter	
0x5B	ADV_TIMING_MODE_EN	Reserved		0	0	0	0	0	0	0	Reserved	
		ADV_TIMING_MODE_EN	0								Enable advanced timing mode	
			1								Disable advanced timing mode	Advanced timing mode must be enabled for the I²P converter to work correctly

MIPI CSI-2 Tx MAP DESCRIPTION

To access the registers listed in Table 96, the user must set the CSI I²C device address by writing to CSI_TX_SLAVE_ADDR[6:0]. CSI_TX_SLAVE_ADDR[6:0] can be found in Register 0xFE, user sub map. Analog devices recommended scripts set the CSI I²C device address to 0x88. The gray shading is indicates the default.

Table 96. MIPI CSI-2 Tx Map Register Descriptions

MIPI CSI-2 Tx			Bit									
Address	**Register Name**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Functionality**	**Comments**
0x00	CSITX_PWRDN	Reserved		0	0	0	0	0	0	0	Reserved	
		CSITX_PWRDN	0								CSI Tx on	
			1								CSI Tx off	
0x01	TLPX	Reserved						0	0	0	Reserved	
		TLPX[4:0]	0	0	0	1	1				These bits set the duration of the T_{LPX} period of the D0P/D0N MIPI Tx data lanes	For normal operation: A 1 bit increase results in an increase of 37.04 ns TLPX[4:0]must be greater than or equal to 2 In I²P mode: A 1 bit increase results in an increase of 18.52 ns TLPX[4:0] must be greater than or equal to 3
0x02	THSPREP	Reserved						0	0	0	Reserved	
		THSPREP[4:0]	0	0	0	1	1				These bits set the duration of the $T_{HS-PREPARE}$ period of the D0P/D0N MIPI Tx data lanes	For normal operation: A 1 bit increase results in an increase of 37.04 ns THSPREP[4:0] must be greater than or equal to 2 In I²P mode: A 1 bit increase results in an increase of 18.52 ns THSPREP[4:0] must be greater than or equal to 3
0x03	THSZEROS	Reserved						0	0	0	Reserved	
		THSZEROS[4:0]	0	0	1	1	0				These bits set the duration of the HS-ZERO period of the D0P/D0N MIPI Tx data lanes	For normal operation: A 1 bit increase results in an increase of 37.04 ns THSZEROS[4:0]must be greater than or equal to 4 In I²P mode: A 1 bit increase results in an increase of 18.52 ns THSZEROS[4:0] must be greater than or equal to 7
0x04	THSTRAIL	Reserved						0	0	0	Reserved	

MIPI CSI-2 Tx			Bit									
Address	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
		THSTRAIL[4:0]	0	0	1	0	0				These bits set the duration of the HS-TRAILperiod of the D0P/D0N MIPI Tx data lanes	For normal operation: A 1 bit increase results in an increase of 37.04 ns THSTRAIL[4:0] must be greater than or equal to 3 In I²P mode: A 1 bit increase results in an increase of 18.52 ns THSTRAIL[4:0] must be greater than or equal to 4
0x05	THSEXIT	Reserved						0	0	0	Reserved	
		THSEXIT[4:0]	0	0	1	0	1				These bits set the duration of the HS-EXIT period of the D0P/D0N MIPI Tx data lanes	For normal operation: A 1 bit increase results in an increase of 37.04 ns THSEXIT[4:0]must be greater than or equal to 3 In I²P mode: A 1 bit increase results in an increase of 18.52 ns THSEXIT[4:0]must be greater than or equal to 6
0x06	TCLK_PREP	Reserved				0	0	0	0	0	Reserved	
		TCLK_PREP[4:0]	0	1	0						These bits set the duration of the HS-PREPARE period of the CLKP/CLKN MIPI Tx clock lanes.	For normal operation: A 1 bit increase results in an increase of 37.04 ns TCLK_PREP[4:0] must be greater than or equal to 2 In I²P mode: A 1 bit increase results in an increase of 18.52 ns TCLK_PREP[4:0] must be greater than or equal to 4
0x07	TCLK_ZEROS	Reserved						0	0	0		
		TCLK_ZEROS[4:0]	0	1	0	1	1				These bits set the duration of the HS-ZERO period of the CLKP/CLKN MIPI Tx clock lanes.	For normal operation: A 1 bit increase results in an increase of 37.04 ns TCLK_ZEROS[4:0] must be greater than or equal to 7 In I²P mode: A 1 bit increase results in an increase of 18.52 ns TCLK_ZEROS[4:0] must be greater than or equal to 14
0x08	TCLK_TRAIL	Reserved					0	0	0	0	Reserved	
		TCLK_TRAIL[3:0]	0	0	1	1					These bits set the duration of the HS-TRAIL period of the CLKP/CLKN MIPI Tx clock lanes.	For normal operation: A 1 bit increase results in an increase of 37.04 ns TCLK_TRAIL[3:0] must be greater than or equal to 3 In I²P mode: A 1 bit increase results in an increase of 18.52 ns TCLK_TRAIL[3:0] must be greater than or equal to 4
0x09	ANCILLARY_DI	Reserved							0	0	Reserved	
		ANCILLARY_DI	1	1	0	0	0	0			Data type for ancillary data packets.	Sets the 6 data type bits used in the data identifier byte. In this case the data identifier byte is for ancillary data packets.

MIPI CSI-2 Tx			Bit									
Address	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
0x0A	VBIVIDEO_DI	Reserved							0	0		
		VBIVIDEO_DI	1	1	0	0	0	1			Data type for VBI data packets.	Sets the 6 data type bits used in the data identifier byte. In this case the data identifier byte is for Vertical Blanking Interval data packets.
0x0B	LSPKT_DI	Reserved							0	0	Reserved	
		LSPKT_DI	0	0	0	0	1	0			Data type for line start packets.	Sets the 6 data type bits used in the data identifier byte. In this case the data identifier byte is for line start packets.
0x0C	LEPKT_DI	Reserved							0	0	Reserved	
		LEPKT_DI	0	0	0	0	1	1			Data type for line end packets.	Sets the 6 data type bits used in the data identifier byte. In this case the data identifier byte is for line end packets.
0x0D	VC_REF	Reserved			0	0	0	0	0	0	Reserved	
		VC_REF	0	0							Virtual channel identifier	Sets the virtual channel identifier bits used in Data Identifier bytes. Data identifier bytes are used in MIPI Tx data packets.
0x0E	CKSUM_EN	Reserved		0	0	0	0	0	0	0	Reserved	
		CKSUM_EN	0								High speed long packet checksum replaced with 0xFFFF	
			1								High speed long packet checksum appended to MIPI Tx CSI stream	
0x1F	CSI_FRAME_ NUM_CTL	Reserved			0	0	0	0	0	0	Reserved	
		FBIT_VAL_AT_ FIELD1START_ INTERLACED		0							The field number is set to 0 at the start of the first field output.	Sets frame number used in MIPI Tx frame start/end packets of first frame.
				1							The field number is set to 1 at the start of the first field output.	
		FRAMENUMBER_ INTERLACED	0								Frame number is 1 for odd fields and 2 for even fields.	Sets frame number in frame start/end packets
			1								Frame number is 2 for even fields and 1 for odd fields.	This I2C bit only applies for interlaced video.
0x20	CSI_ LINENUMBER_ INCR_ INTERLACED	Reserved		0	0	0	0	0	0	0	Reserved	
		LINENUMBER_INCR_ INTERLACED	0								Increment line numbers by 2 (default).	The line numbers in the line start (LS) and line end (LE) packets for interlaced video have to increment by more than 1. This bit gives the option of whether line numbers are incremented in steps of 2 or 3.
			1								Increment line numbers by 3.	This bit only applies for interlaced video.
0x26	ESC_MODE_CTL	Reserved					0	0	0	0	Reserved	

MIPI CSI-2 Tx			Bit									
Address	Register Name	Bit Description	7	6	5	4	3	2	1	0	Functionality	Comments
		ESC_XSHUTDOWN_CLK				0					These two bits force the MIPI Tx clock lanes (CLKP and CLKN) to enter and exit the Ultralow Power State	See MIPI CSI-2 Tx Output section for more information.
						1						
		ESC_MODE_EN_CLK			0							
					1							
		ESC_XSHUTDOWN_D0		0							These two bits force the MIPI Tx data lane (D0P and D0N) to enter and exit the Ultralow Power State	See MIPI CSI-2 Tx Output section for more information.
				1								
		ESC_MODE_EN_D0	0									
			1									
0xDE	DPHY_PWDN_CTL	DPHY_PWDN								0	MIPI Tx D-PHY Block is not powered-down	To use this bit, the DPHY_PWDN_OVERRIDE bit must be set to 1.
										1	MIPI Tx D-PHY Block is powered-down	
		DPHY_PWDN_OVERRIDE							0		Disable manual control of MIPI Tx D-PHY powerdown.	
									1		Enable manual control of MIPI Tx D-PHY powerdown.	The MIPI Tx D-PHY block can now be powered down by using the DPHY_PWDN bit.
		Reserved	0	0	0	0	0	0			Reserved	

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).