REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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TITLE

MICROCIRCUIT, DIGITAL-LINEAR, QUAD, 14-BIT, 125 MSPS SERIAL LVDS 1.8 V ANALOG-TO-DIGITAL CONVERTER, MONOLITHIC SILICON

SIZE	**CODE IDENT. NO.**
A	**16236**

DWG NO.
V62/13627

REV

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AMSC N/A

5962-V085-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quad, 14-bit, 125 MSPS serial LVDS 1.8 V analog-to-digital converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/13627	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD9253-EP	Quad, 14-bit, 125 MSPS serial LVDS 1.8 V analog-to-digital converter

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	JEDEC MO-220-WKKD	Lead Lead Frame Chip Scale Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

AVDD to AGND ..... -0.3 V to +2.0 V
DRVDD to AGND ..... -0.3 V to +2.0 V
Digital outputs (D0±x, D1±x, DCO+, DCO-, FCO+, FCO-) to AGND ..... -0.3 V to +2.0 V
CLK+, CLK- to AGND ..... -0.3 V to +2.0 V
VIN+x, VIN-x to AGND ..... -0.3 V to +2.0 V
SCLK/DTP, SDIO/OLM, CSB to AGND ..... -0.3 V to +2.0 V
SYNC, PDWN to AGND ..... -0.3 V to +2.0 V
RBIAS to AGND ..... -0.3 V to +2.0 V
VREF, SENSE to AGND ..... -0.3 V to +2.0 V
Operating temperature range (Ambient) ..... -55°C to +125°C
Maximum junction temperature ..... 150°C
Lead temperature (Soldering, 10 sec) ..... 300°C
Storage temperature range (Ambient) ..... -65°C to 150°C

1.5 Thermal characteristics.

Thermal resistance

Case outline	Air flow velocity (m/sec)	θ_{JA} 2/	ψ_{JT}	ψ_{JB}	θ_{JC} TOP	θ_{JC} BOTTOM	Unit
Case X	0.0	20.3	0.10	5.9	6.1	1.0	°C/W
	1.0	17.6	0.16	N/A 3/	N/A 3/	N/A 3/	°C/W
	2.5	16.5	0.20	N/A 3/	N/A 3/	N/A 3/	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

1/ Stresses above those listed under “Absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those beyond indicated in the operational section of this specifications is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ θ_{JA} for a 4-layer printed circuit board (PCB) with solid ground plane (simulated). Exposed pad soldered to PCB.
3/ N/A = not applicable.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function description. The Terminal function description shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test 2/	Test conditions 3/	Temp	Limits			Unit
			Min	Typ	Max	
DC SPECIFICATIONS						
Resolution			14			Bits
Accuracy						
No missing codes		Full	Guaranteed			
Offset error		Full	-0.8	-0.3	+0.1	% FSR
Offset matching		Full	-0.6	+0.2	+0.6	% FSR
Gain error		Full	-12	-3	+2	% FSR
Gain matching		Full		1.1	1.6	% FSR
Differential Nonlinearity (DNL)		Full 25°C	-0.8	 ±0.8	+1.9	LSB LSB
Integral Nonlinearity (INL)		Full 25°C	-4.5	 ±2.0	+4.5	LSB LSB
Temperature drift						
Offset error		Full		±2		ppm/°C
Gain error		Full		±50		ppm/°C
Internal voltage reference						
Output voltage (1 V Mode)		Full	0.98	1.0	1.02	V
Load regulation at 1.0 mA (V_{REF} = 1 V)		Full		2		mV
Input resistance		Full		7.5		kΩ
Input referred noise						
V_{REF} = 1.0 V		25°C		0.94		LSB rms
Analog inputs						
Differential input voltage (V_{REF} = 1 V)		Full		2		V p-p
Common mode voltage		Full		0.9		V
Differential input resistance				5.2		kΩ
Differential input capacitance		Full		3.5		pF
Power supply						
AVDD		Full	1.7	1.8	1.9	V
DRVDD		Full	1.7	1.8	1.9	V
I_{AVDD} 4/		Full		183	205	mA
I_{DRVDD}(ANSI-644 mode) 4/		Full		61	63	mA
I_{DRVDD}(Reduce range mode) 4/		25°C		53		mA
Total power consumption						
DC input		Full		403		mW
Sine wave input (Four channels including output drivers ANSI 644 mode)		Full		440	480	mW
Sine wave input (Four channels including output drivers reduced range mode)		25°C		425		mW
Power down mode		Full		2		mW
Standby mode 5/		Full		235		mW

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test 2/	Test conditions 3/	Temp	Limits			Unit
			Min	Typ	Max	
AC SPECIFICATIONS						
Signal to Noise Ratio (SNR)						
f_{IN} = 9.7 MHz		25°C		75.3		dBFS
f_{IN} = 30.5 MHz		25°C		75.2		
f_{IN} = 70 MHz		Full	72	74.1		
f_{IN} = 140 MHz		25°C		72.2		
f_{IN} = 200 MHz		25°C		70.7		
Signal to Noise And Distortion ratio (SINAD)						
f_{IN} = 9.7 MHz		25°C		75.2		dBFS
f_{IN} = 30.5 MHz		25°C		75.1		
f_{IN} = 70 MHz		Full	71.7	74.0		
f_{IN} = 140 MHz		25°C		71.9		
f_{IN} = 200 MHz		25°C		70.4		
Effective Number Of Bits (ENOB)						
f_{IN} = 9.7 MHz		25°C		12.2		Bits
f_{IN} = 30.5 MHz		25°C		12.2		
f_{IN} = 70 MHz		Full		12.0		
f_{IN} = 140 MHz		25°C		11.7		
f_{IN} = 200 MHz		25°C		11.4		
Spurious Free Dynamic Range (SFDR)						
f_{IN} = 9.7 MHz		25°C		98		dBc
f_{IN} = 30.5 MHz		25°C		92		
f_{IN} = 70 MHz		Full	76	90		
f_{IN} = 140 MHz		25°C		85		
f_{IN} = 200 MHz		25°C		83		
Worst Harmonic (Second or Third)						
f_{IN} = 9.7 MHz		25°C		-98		dBc
f_{IN} = 30.5 MHz		25°C		-92		
f_{IN} = 70 MHz		Full		-90	-76	
f_{IN} = 140 MHz		25°C		-85		
f_{IN} = 200 MHz		25°C		-83		
Worst other Harmonic (Excluding Second or Third)						
f_{IN} = 9.7 MHz		25°C		-101		dBFS
f_{IN} = 30.5 MHz		25°C		-100		
f_{IN} = 70 MHz		Full		-95	-83	
f_{IN} = 140 MHz		25°C		-96		
f_{IN} = 200 MHz		25°C		-92		
Two tone Intermodulation Distortion (IMD) –AN1 and AND2 = -7.0 dBFS						
f_{IN1} = 70.5 MHz, f_{IN2} = 72.5 MHz		25°C		86		dBc
Crosstalk 6/		Full		-95		dB
Crosstalk (Overrange condition) 7/		25°C		-89		dB
Power Supply Rejection Ratio (SPRR) 8/						
AVDD		25°C		48		dB
DRVDD		25°C		75		dB
Analog input bandwidth, Full power		25°C		650		MHz

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test 2/	Test conditions 3/	Temp	Limits			Unit
			Min	Typ	Max	
DIGITAL SPECIFICATIONS						
Clock inputs (CLK+, CLK-)						
Logic compliance			CMOS/LVDS/LVPECL			
Differential input voltage 9/		Full	0.2		3.6	V p-p
Input voltage range		Full	AGND – 0.2		AGND + 0.2	V
Input common mode voltage		Full		0.9		V
Input resistance (Differential)		25°C		15		kΩ
Input capacitance		25°C		4		pF
Logic inputs (PDWN, SYNC, SCLK)						
Logic 1 voltage		Full	1.2		AVDD + 0.2	V
Logic 0 voltage		Full	0		0.8	V
Input resistance		25°C		30		kΩ
Input capacitance		25°C		2		pF
Logic input (CSB)						
Logic 1 voltage		Full	1.2		AVDD + 0.2	V
Logic 0 voltage		Full	0		0.8	V
Input resistance		25°C		26		kΩ
Input capacitance		25°C		2		pF
Logic input (SDIO/OLM)						
Logic 1 voltage		Full	1.2		AVDD + 0.2	V
Logic 0 voltage		Full	0		0.8	V
Input resistance		25°C		26		kΩ
Input capacitance		25°C		5		pF
Logic output (SDIO/OLM) 10/						
Logic 1 voltage (I_{OH} = 800 µA)		Full		1.79		V
Logic 0 voltage (I_{OL} = 50 µA)		Full			0.05	V
Digital outputs (D0±x, D1±x), ANSI-644						
Logic compliance			LVDS			
Differential output voltage (V_{OD})		Full	290	345	400	mV
Output offset voltage (V_{OS})		Full	1.15	1.25	1.35	V
Output coding (Default)			Twos complement			
Digital outputs (D0±x, D1±x), low power, reduced signal option						
Logic compliance			LVDS			
Differential output voltage (V_{OD})		Full	160	200	230	mV
Output offset voltage (V_{OS})		Full	1.15	1.25	1.35	V
Output coding (Default)			Twos complement			

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test 2/ 11/	Test conditions 3/	Temp	Limits			Unit
			Min	Typ	Max	
SWITCHING SPECIFICATIONS						
Clock						
Input clock rate		Full	10		1000	MHz
Conversion rate		Full	10		125	MSPS
Clock Pulse Width High (t_{EH})		Full		4.00		ns
Clock Pulse Width Low (t_{EL})		Full		4.00		ns
Output parameters 12/						
Propagation Delay (t_{PD})		Full		2.3		ns
Rise Time (t_R) (20% to 80%)		Full		300		ps
Fall Time (t_F) (20% to 80%)		Full		300		ps
FCO Propagation Delay (t_{FCO})		Full	1.5	2.3	3.1	ns
DCO Propagation Delay (t_{CPD}) 13/		Full		t_{FCO} + (t_{SAMPLE}/16)		ns
DCO-to-Data Delay (t_{DATA}) 13/		Full	(t_{SAMPLE}/16) - 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	ops
DCO-to-FCO Delay (t_{FRAME}) 13/		Full	(t_{SAMPLE}/16) - 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	ps
Lane Delay (t_{LD})				90		ps
Data to Data Skew ($t_{DATA-MAX} - t_{DATA-MIN}$)		Full		±50	±200	ps
Wake-Up Time (Standby)		25°C		250		ns
Wake-Up Time (Power-Down) 14/		25°C		375		µs
Pipeline Latency		Full		16		Clock cycles
Aperture						
Aperture Delay (t_A)		25°C		1		ns
Aperture Uncertainty (Jitter, t_J)		25°C		135		fs ms
Out-of-Range Recovery Time		25°C		1		Clock cycles

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ See the AN-835 manufacturer's application note. Understanding high speed ADC testing and evaluation, for definitions and for details on how these tests were completed.

3/ AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -1.0 dBFS, unless otherwise noted.

4/ Measured with a low input frequency, full scale sine wave of all four channels.

5/ It can be controlled via the SPI.

6/ Crosstalk is measured at 70 MHz with an −1.0 dBFS analog input on one channel and no input on the adjacent channel.

7/ The over range condition is specified with 3 dB of the full-scale input range.

8/ PSRR is measured by injecting a sinusoidal signal at 10 MHz to the power supply pin and measuring the output spur on the FFT. PSRR is calculated as the ratio of the amplitudes of the spur voltage over the pin voltage, expressed in decibels.

9/ This is specified for LVDS and LVPECL only.

10/ This is specified for 13 SDIO/OLM pins sharing the same connection.

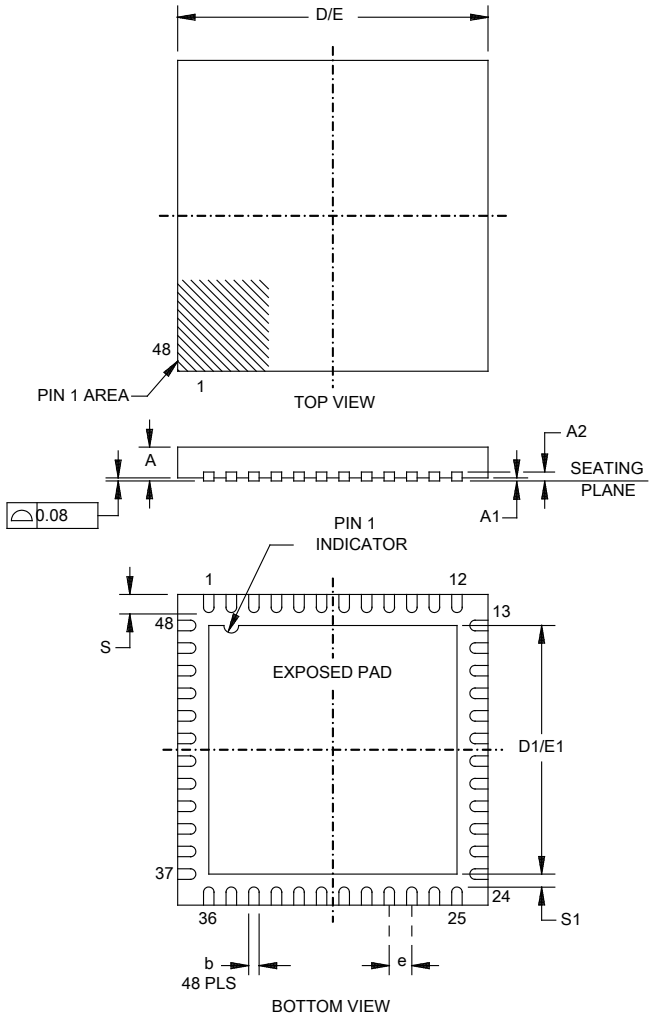
11/ Measured on standard FR-4 material.

12/ Can be adjusted via the SPI. The conversion rate is the clock rate after the divider.

13/ $t_{SAMPLE}/16$ is based on the number of bits in two LVDS data lanes. $t_{SAMPLE} = 1/f_S$.

14/ Wake-up time is defined as the time required to return to normal operation from power-down mode.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.70	0.80	D1/E1	5.55	5.65
A1		0.05	e	0.50 BSC	
A2	0.20 REF		S	0.35	0.45
b	0.18	0.30	S1	0.20	
D/E	6.90	7.10			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC STANDARDS MO-220-WKKD.

FIGURE 1. Case outline.

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	VIN+D	48	VIN+C
2	VIN-D	47	VIN-C
3	AVDD	46	AVDD
4	AVDD	45	AVDD
5	CLK-	44	SYNC
6	CLK+	43	VCM
7	AVDD	42	VREF
8	DRVDD	41	SENSE
9	D1-D	40	RBIAS
10	D1+D	39	AVDD
11	D0-D	38	VIN-B
12	D0+D	37	VIN+B
13	D1-C	36	VIN+A
14	D1+C	35	VIN-A
15	D0-C	34	AVDD
16	D0+C	33	PDWN
17	DCO-	32	CSB
18	DCO+	31	SDIO/OLM
19	FCO-	30	SCLK/DTP
20	FCO+	29	DRVDD
21	D1-B	28	D0+A
22	D1+B	27	D0-A
23	D0-B	26	D1+A
24	D0+B	25	D1-A

NOTE:
1. The exposed thermal PAD on the bottom of the package provides the analog ground for the part, this exposed PAD must be connected to ground for proper operation.

FIGURE 2. Terminal connections

Case outline X

Pin No.	Mnemonic	Description
0	AGND, Exposed Pad	Analog Ground, Exposed Pad. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
1	VIN+D	ADC D Analog Input True.
2	VIN−D	ADC D Analog Input Complement.
3, 4, 7, 34, 39, 45, 46	AVDD	1.8 V Analog Supply Pins.
5, 6	CLK−, CLK+	Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs.
8, 29	DRVDD	Digital Output Driver Supply.
9	D1−D	Channel D Digital Output 1 Complement.
10	D1+D	Channel D Digital Output 1 True.
11	D0−D	Channel D Digital Output 0 Complement.
12	D0+D	Channel D Digital Output 0 True.
13	D1−C	Channel C Digital Output 1 Complement.
14	D1+C	Channel C Digital Output 1 True.
15	D0−C	Channel C Digital Output 0 Complement.
16	D0+C	Channel C Digital Output 0 True.
17	DCO−	Data Clock Output Complement.
18	DCO+	Data Clock Output True.
19	FCO−	Frame Clock Output Complement.
20	FCO+	Frame Clock Output True.
21	D1−B	Channel B Digital Output 1 Complement.
22	D1+B	Channel B Digital Output 1 True.
23	D0−B	Channel B Digital Output 0 Complement.
24	D0+B	Channel B Digital Output 0 True.
25	D1−A	Channel A Digital Output 1 Complement.
26	D1+A	Channel A Digital Output 1 True.
27	D0−A	Channel A Digital Output 0 Complement.
28	D0+A	Channel A Digital Output 0 True.
30	SCLK/DTP	SPI Clock Input/Digital Test Pattern.
31	SDIO/OLM	SPI Data Input and Output Bidirectional SPI Data/Output Lane Mode.
32	CSB	SPI Chip Select Bar. Active low enable; 30 kΩ internal pull-up.
33	PDWN	Digital Input, 30 kΩ Internal Pull-Down. PDWN high = power-down device. PDWN low = run device, normal operation.
35	VIN−A	ADC A Analog Input Complement.
36	VIN+A	ADC A Analog Input True.
37	VIN+B	ADC B Analog Input True.
38	VIN−B	ADC B Analog Input Complement.
40	RBIAS	Sets Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground.
41	SENSE	Reference Mode Selection.
42	VREF	Voltage Reference Input and Output.
43	VCM	Analog Input Common-Mode Voltage.
44	SYNC	Digital Input. SYNC input to clock divider.
47	VIN−C	ADC C Analog Input Complement.
48	VIN+C	ADC C Analog Input True.

FIGURE 3. Terminal function description.

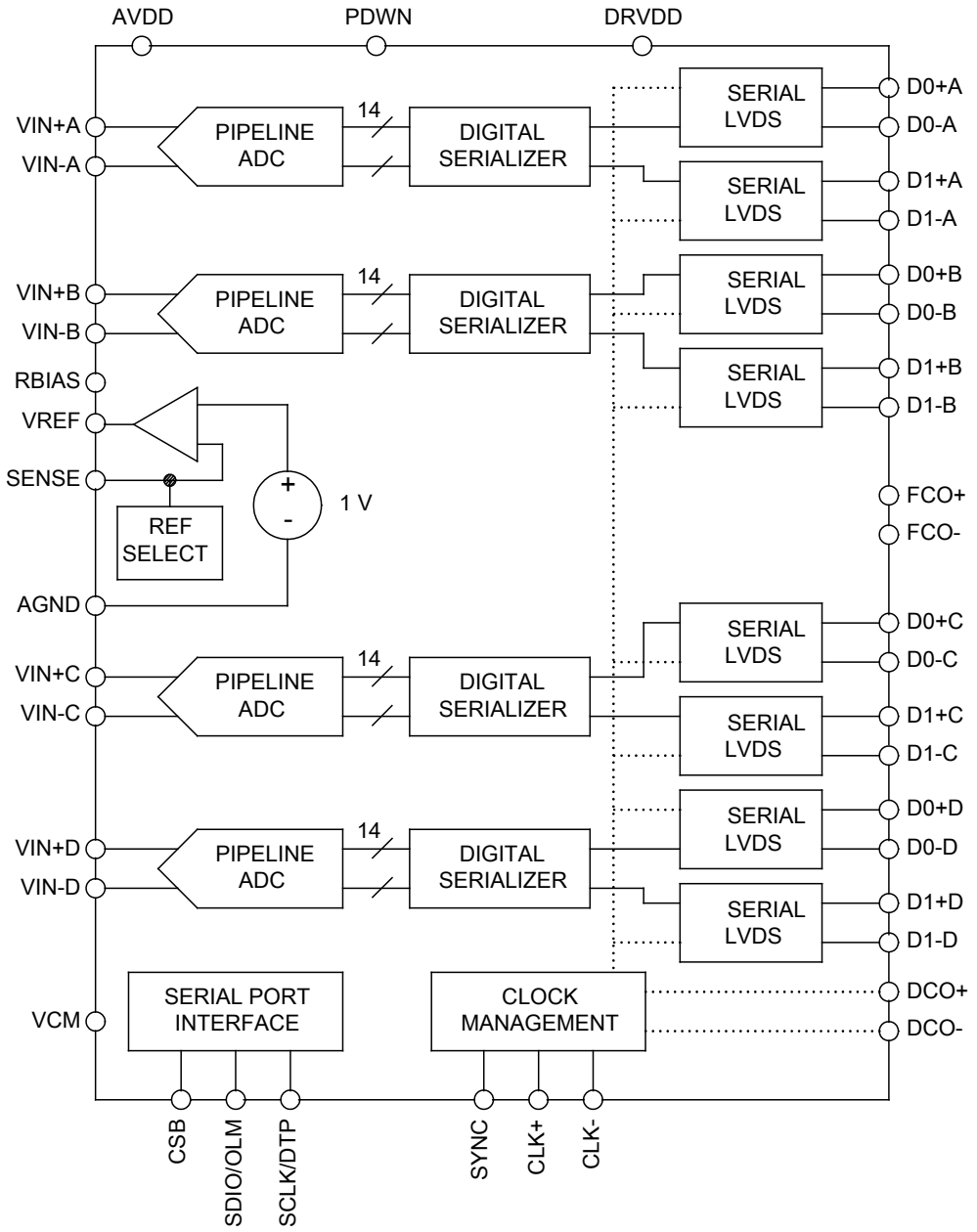


FIGURE 4. Functional block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Transport media	Vendor part number
V62/13627-01XE	24355	Tray, 260	AD9253TCPZ-125EP
		Tape and reel	AD9253TCPZR7-125EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106