REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. -rrp	02-07-18	R. Monnin
B	Redrawn. Paragraphs updated to MIL-PRF-38535 requirements. - drw	14-11-21	Charles F. Saffle

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																			
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REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B				
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13					

PMIC N/A

PREPARED BY
Rick C. Officer

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles E. Besore

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
91-10-02

REVISION LEVEL
B

MICROCIRCUIT, LINEAR, CMOS, 8-BIT, A/D CONVERTER WITH TRACK/HOLD, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89518**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89518	01	R	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function	Total unadjusted error
01	AD7821	CMOS 8-bit ADC with track/hold	±1.0 LSB

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage to ground (V_{SS})	0 V dc to –7.0 V dc
Supply voltage to ground (V_{DD})	0 V dc to +7.0 V dc
Digital input voltage	-0.3 V dc to V_{DD}
Digital output voltage	-0.3 V dc to V_{DD}
Positive reference voltage (V_{REF+})	V_{SS} – 0.3 V dc, V_{DD} + 0.3 V dc
Negative reference voltage (V_{REF-})	V_{SS} – 0.3 V dc, V_{DD} + 0.3 V dc
Input voltage (V_{IN})	V_{SS} – 0.3 V dc, V_{DD} + 0.3 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation (P_D)	450 mW 2/
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage to ground (V_{SS})	-4.75 V dc to –5.25 V dc
Supply voltage to ground (V_{DD})	+4.75 V dc to +5.25 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C
Positive reference voltage (V_{REF+})	V_{REF-} to V_{DD}
Negative reference voltage (V_{REF-})	V_{SS} to V_{REF+}

1/ All voltages are with respect to ground.
2/ Derate above T_A = +75°C at 6.0 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	Res	This is the minimum resolution for which no missing codes are guaranteed.	1, 2, 3	01	8.0		Bits
Total unadjusted error	TUE	3/	1, 2, 3	01		±1.0	LSB
Analog input leakage current	I_{IN}		1, 2, 3	01		±3.0	µA
Reference input resistance	R_{IN}		1, 2, 3	01	1.0	4.0	kΩ
Digital input high current	I_{IH}	$\overline{CS}$ and $\overline{RD}$ inputs, V_{IH} = 5.25 V, V_{IL} = 0 V	1, 2, 3	01		±1.0	µA
		$\overline{WR}$ input, V_{IH} = 5.25 V, V_{IL} = 0 V				±3.0	
		Mode input, V_{IH} = 5.25 V, V_{IL} = 0 V				±200	
Digital input low current	I_{IL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ and mode inputs	1, 2, 3	01		-1.0	µA
Digital output high level voltage	V_{OH}	DB_0-DB_7, $\overline{OFL}$, and $\overline{INT}$ outputs, I_{SOURCE} = -360 µA	1, 2, 3	01	4.0		V
Digital output low level voltage	V_{OL}	DB_0-DB_7, $\overline{OFL}$, and $\overline{INT}$ outputs, I_{SINK} = 1.6 mA	1, 2, 3	01		0.4	V
Floating state leakage current	I_{OUT}	DB_0-DB_7, V_{OUT} = 5.25 V, then V_{OUT} = 0 V	1, 2, 3	01		±3.0	µA
Supply current from V_{DD}	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = 0 V	1, 2, 3	01		20.0	mA
Digital input low level voltage	V_{IL}	$\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ inputs	1,2,3	01		0.8	V
		Mode input				1.5	
Digital input high level voltage	V_{IH}	$\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ inputs	1, 2, 3	01	2.4		V
		Mode input			3.5		
Power supply sensitivity	PSS	V_{DD} = 5.0 V ± 5%, V_{REF} = 4.75 V maximum	1, 2, 3	01		±0.25	LSB
Signal to noise ratio	SNR	4/, 5/	1, 2, 3	01	45		dB
Total harmonic distortion	THD	4/, 5/	1, 2, 3	01		-50	dB
Peak harmonic or spurious noise		4/, 5/	1, 2, 3	01		-50	dB
Intermodulation distortion	IMD	Second order terms 5/, 6/	1, 2, 3	01		-50	dB
		Third order terms 5/, 6/				-50	
Supply current from V_{SS}	I_{SS}	$\overline{CS}$ = $\overline{RD}$ = 0 V	1, 2, 3	01		100	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/, 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital input capacitance	C_{ID}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ and mode inputs, See 4.3.1c, $T_A = +25°C$	4	01		8.0	pF
Analog input capacitance	C_{IA}	See 4.3.1c	4	01		55	pF
Digital output capacitance	C_{OUT}	See 4.3.1c, $T_A = +25°C$	4	01		8.0	pF
Slew rate, tracking	SR	4/, 5/	7, 8	01		1.6	V/μs
$\overline{RD}$ pulse width	t_{READ1}	Determined by t_{ACC1} 7/, 8/	9	01	160		ns
			10, 11		240		
$\overline{RD}$ pulse width	t_{READ2}	Determined by t_{ACC2} 7/, 8/	9	01	65		ns
			10, 11		85		
$\overline{CS}$ to $\overline{RD}$ / $\overline{WR}$ setup time	t_{CSS}	7/, 8/	9, 10, 11	01	0		ns
$\overline{CS}$ to $\overline{RD}$ / $\overline{WR}$ hold time	t_{CSH}	7/, 8/	9, 10, 11	01	0		ns
$\overline{CS}$ to RDY delay	t_{RDY}	C_L = 50 pF, 8/ pull-up resistor = 4.7 kΩ	9	01		70	ns
			10,11			100	
Conversion time ($\overline{RD}$ mode)	t_{CRD}	8/	9	01		700	ns
			10, 11			975	
Data access time ($\overline{RD}$ mode)	t_{ACCO}	8/, 9/	9	01		750	ns
			10, 11			1050	
$\overline{RD}$ to $\overline{INT}$ delay ($\overline{RD}$ mode)	t_{INTH}	C_L = 50 pF 8/	9	01		80	ns
			10, 11			90	
Data hold time	t_{DH}	8/, 10/	9	01		60	ns
			10, 11			80	
Delay time between conversion	t_P	7/, 8/	9	01	350		ns
			10, 11		500		
Write pulse width	t_{WR}	7/, 8/	9	01	0.25	10	μs
			10, 11		0.4	10	
Delay time between $\overline{WR}$ and $\overline{RD}$ pulses	t_{RD}	7/, 8/	9	01	250		ns
			10, 11		450		
Data access time ($\overline{WR}$ / $\overline{RD}$ mode)	t_{ACC1}	8/, 9/	9	01		185	ns
			10, 11			275	
$\overline{RD}$ to $\overline{INT}$ delay	t_{R1}	8/	9	01		150	ns
			10, 11			220	
$\overline{WR}$ to $\overline{INT}$ delay	t_{INTL}	C_L = 50 pF, see figure 3 11/	9	01		500	ns
			10, 11			700	
Data access time ($\overline{WR}$ / $\overline{RD}$ mode)	t_{ACC2}	8/, 9/	9	01		90	ns
			10, 11			130	
$\overline{WR}$ to $\overline{INT}$ delay (stand alone operation)	t_{IHWR}	C_L = 50 pF 8/	9	01		80	ns
			10, 11			120	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data access time after $\overline{INT}$ (stand alone operation)	t_{ID}	8/ 9/	9	01		45	ns
			10,11			70	

1/ Unless otherwise specified, V_{DD} = +5.0 V; V_{REF+} = +5.0 V; V_{REF-} = GND = 0 V and V_{SS} = 0 V.

2/ All input control signals are specified with $t_R = t_F$ = 20 ns (10% to 90% of +5.0 V) and timed from a voltage level of 1.6 V.

3/ Includes gain error, offset error and linearity error.

4/ V_{IN} = 99.85 kHz full scale sine wave at 5.0 V peak to peak with f sampling = 500 kHz.

5/ V_{SS} = -5.0 V; V_{DD} = +5.0 V; V_{REF+} = +2.5 V; V_{REF-} = -2.5 V.

6/ fa (84.72 kHz) and fb (94.97 kHz) combine to produce a full scale sine wave at the analog input with f sampling = 500 kHz.

7/ Pass/fail tested only with tested parameter used as a test condition.

8/ Refer to timing diagram of figure 3. These parameters are tested to subgroup 9 under group A test requirements.

9/ Measured with load circuits of figure 2 and defined as the time required for an output to cross 0.8 V to 2.4 V.

10/ Defined as the time required for the data lines to change 0.5 V when loaded with the circuits of figure 2 and is measured only for initial test and after process or design changes which may affect t_{DH}.

11/ If not tested, shall be guaranteed to the limits specified in table I herein.

Device type	01
Case outlines	R and 2
Terminal number	Terminal symbol
1	V_{IN}
2	DB_0(LSB)
3	DB_1
4	DB_2
5	DB_3
6	$\overline{WR}$ /RDY
7	Mode
8	$\overline{RD}$
9	$\overline{INT}$
10	GND
11	V_{REF-}
12	V_{REF+}
13	$\overline{CS}$
14	DB_4
15	DB_5
16	DB_6
17	DB_7(MSB)
18	$\overline{OFL}$
19	V_{SS}
20	V_{DD}

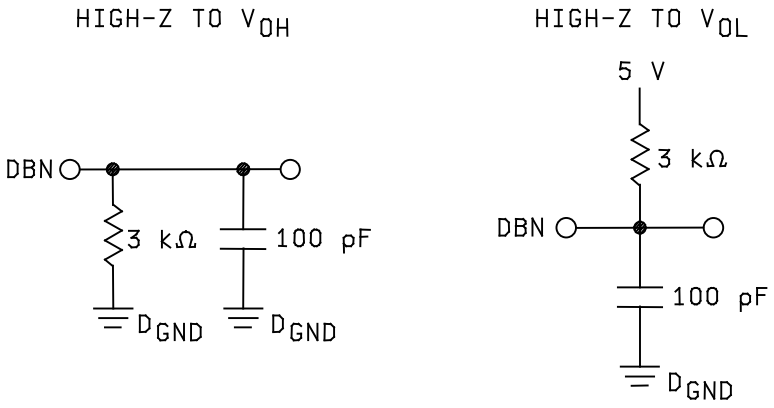
FIGURE 1. Terminal connections.

Pin Function Description

Pin	Symbol	Description
1	V_{IN}	Analog input. Range: $V_{REF-} \le V_{IN} \le V_{REF+}$
2	DB_0	Three-State Data Output (LSB)
3-5	DB_1 - DB_3	Three-State Data Outputs.
6	$\overline{WR}$ /RDY	WRITE control input/READY status output.
7	MODE	Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. This input is internally pulled low through a 50 μA current source.
8	$\overline{RD}$	READ input. $\overline{RD}$ must be low to access data from the part.
9	$\overline{INT}$	INTERRUPT Output. $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.
10	GND	Ground
11	V_{REF-}	Lower limit of reference span. Range: $V_{SS} \le V_{REF-} < V_{REF+}$
12	V_{REF+}	Upper limit of reference span. Range: $V_{REF-} < V_{REF+} \le V_{DD}$
13	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
14-16	DB_4 – DB_6	Three-State Data Outputs.
17	DB_7	Three-State Data Output (MSB)
18	$\overline{OFL}$	Overflow Output. If the analog input is higher than (V_{REF+} - ½ LSB), $\overline{OFL}$ will be low at the end of conversion. It is a non-three-state output which can be used to cascade 2 or more devices to increase resolution.
19	V_{SS}	Negative supply voltage. V_{SS} = 0 V; Unipolar Operation. V_{SS} = -5 V; Bipolar Operation.
20	V_{DD}	Positive supply voltage, +5 V.

FIGURE 1. Terminal connections - continued.

Load circuits for data access time



Load circuits for data hold time

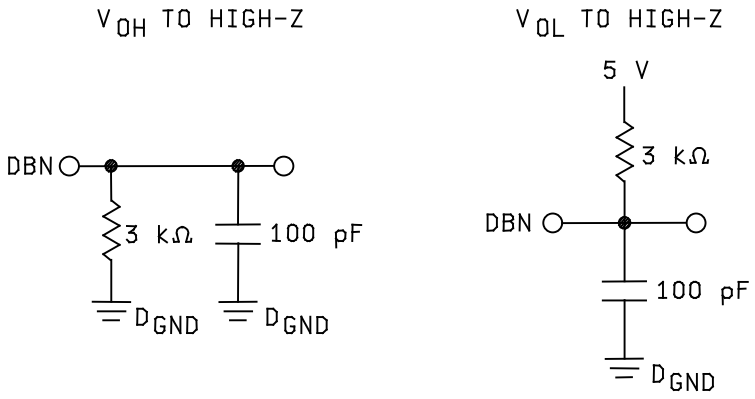
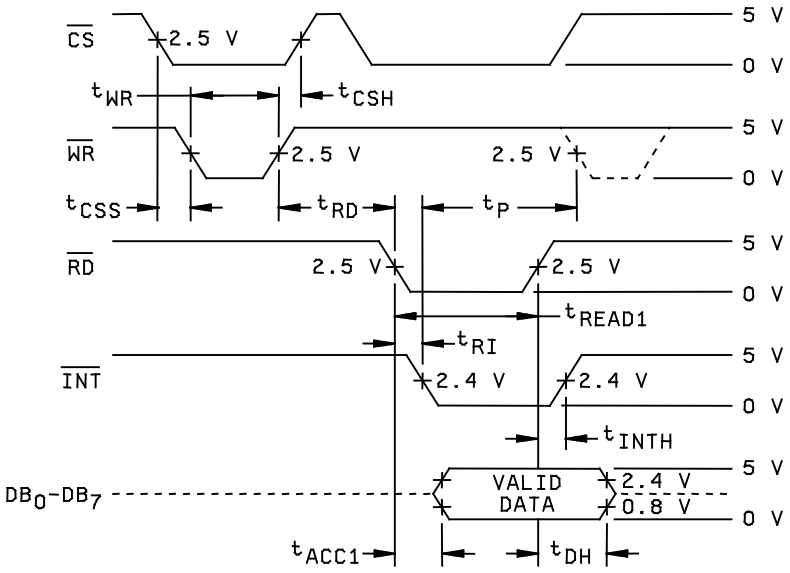


FIGURE 2. Output load circuits.

WR-RD mode ($t_{RD} < t_{INTL}$)



WR-RD mode ($t_{RD} > t_{INTL}$)

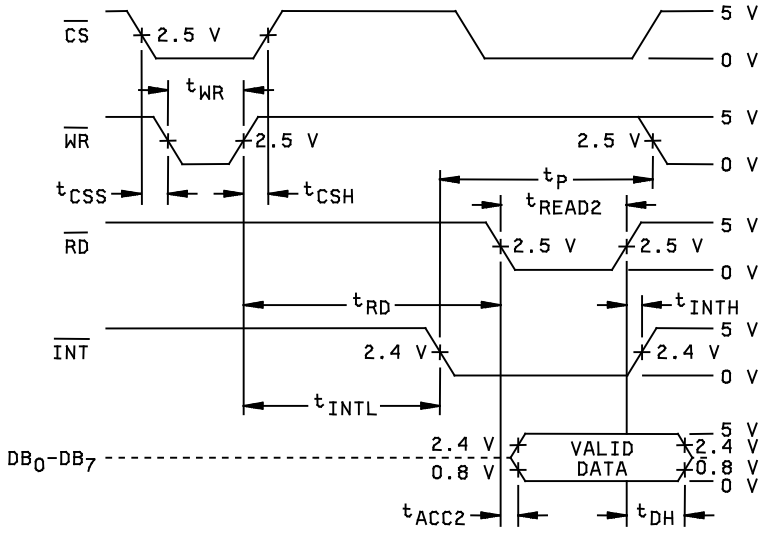
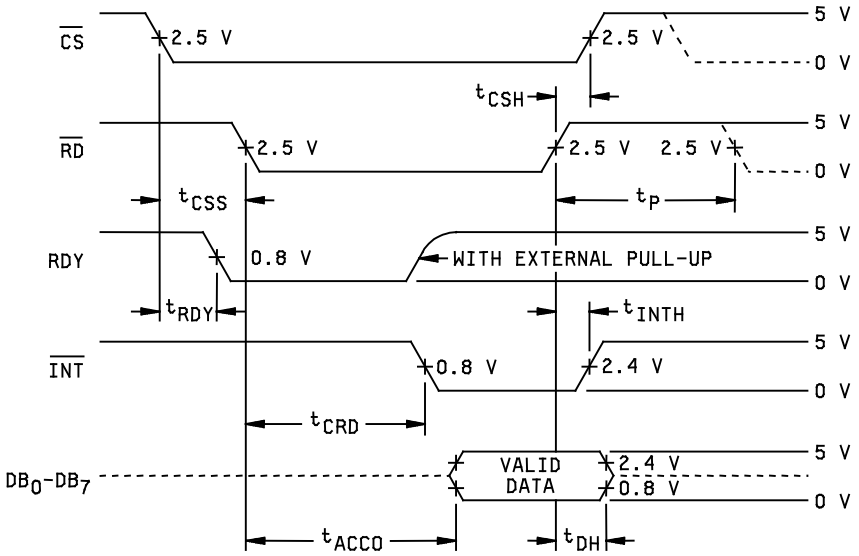


FIGURE 3. Mode timing waveforms.

RD mode



WR-RD mode stand-alone operation, $\overline{CS}$ = $\overline{RD}$ = 0

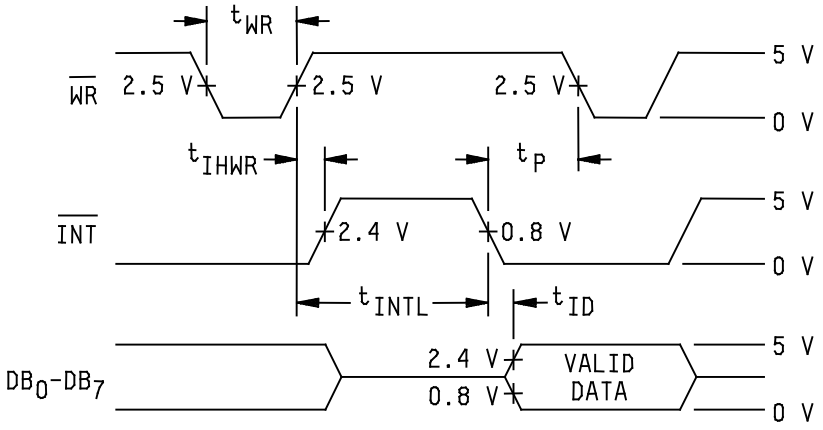


FIGURE 3. Mode timing waveforms – continued.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IA}, C_{ID}, and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-11-21

Approved sources of supply for SMD 5962-89518 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8951801RA	24355	AD7821TQ/883B
5962-89518012A	24355	AD7821TE/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland