REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15					

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 14-12-16	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR-DIGITAL, 500 kSPS, 8-CHANNEL, SOFTWARE-SELECTABLE, TRUE BIPOLAR INPUT, 12-BIT PLUS SIGN ADC, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/14636**
	REV	**PAGE** 1 **OF** 15

AMSC N/A

5962-V024-15

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 500 kSPS, 8-channel, software-selectable, true bipolar input, 12- bit plus sign ADC microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/14636	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD7327-EP	500 kSPS, 8-channel, software-selectable, true bipolar input, 12- bit plus sign ADC

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	JEDEC MO-153-AC	Thin Shrink Small Outline Package (TSSOP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to AGND, DGND	-0.3 V to +16.5 V
V_{SS} to AGND, DGND	+0.3 V to -16.5 V
V_{DD} to V_{CC}	V_{CC} – 0.3 V to 16.5 V
V_{CC} to AGND, DGND	-0.3 V to +7 V
V_{DRIVE} to AGND, DGND	-0.3 V to +7 V
AGND to DGND	-0.3 V to +0.3 V
Analog input voltage to AGND	V_{SS} – 0.3 V to V_{DD} + 0.3 V
Digital input voltage to DGND	-0.3 V to +7 V
Digital output voltage to GND	-0.3 V to V_{DRIVE} + 0.3 V
REFIN to AGND	-0.3 V to V_{CC} + 0.3 V
Input current to any pin except supplies	±10 mA 2/
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature	150°C
Case outline X:	
Thermal impedance, θ_{JA}	143°C/W
Thermal impedance, θ_{JC}	45°C/W
Pb-free temperature, soldering reflow	260(0) °C
ESD	2.5 kV

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ Transient currents of up to 100 mA do not cause SCR latch-up.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Serial interface timing diagram. The serial interface timing diagram shall be as shown in figure 5.

3.5.6 Channel to channel isolation. The channel to channel isolation shall be as shown in figure 6.

3.5.7 CMRR vs Common Mode Ripple frequency. The CMRR vs Common Mode Ripple frequency shall be as shown in figure 7.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions $-55°C \le T_A \le +125°C$ 2/	Limits			Unit
			Min	Typ	Max	
Dynamic Performance (f_{IN} = 50 kHz sine wave)						
Signal-to-Noise Ratio	SNR 3/	Differential mode, V_{CC} = 4.75 V to 5.25 V	76			dB
		Differential mode, V_{CC} < 4.75 V	75.5			
		Single-ended/pseudo differential mode; ±10 V, ±2.5 V and ±5 V ranges, V_{CC} = 4.75 V to 5.25 V	72			
		Single-ended/pseudo differential mode; 0 V to 10 V V_{CC} = 4.75 V to 5.25 V and all ranges at V_{CC} < 4.75 V	71.7			
Signal-to-Noise + Distortion	SINAD 3/	Differential mode; ±2.5 V and ±5 V ranges	75			
		Differential mode; 0 V to 10 V	74			
		Differential mode; ±10 V range		76		
		Single-ended/pseudo differential mode; ±2.5 V and ±5 V ranges	70.7			
		Single-ended/pseudo differential mode; 0 V to +10 V and ±10 V ranges		72.5		
Total Harmonic Distortion	THD 3/	Differential mode; ±2.5 V and ±5 V ranges			-79.3	
		Differential mode; 0 V to 10 V ranges			-78.8	
		Differential mode; ±10 V range		-82		
		Single-ended/pseudo differential mode; ±5 V range			-76	
		Single-ended/pseudo differential mode; ±2.5 V range			-77.3	
		Single-ended/pseudo differential mode; 0 V to +10 V and ±10 V ranges		-80		
Peak Harmonic or Spurious Noise	SFDR 3/	Differential mode; ±2.5 V and ±5 V ranges			-80	
		Differential mode; 0 V to 10 V ranges			-80	
		Differential mode; ±10 V ranges		-82		
		Single-ended/pseudo differential mode; ±5 V range			-77.2	
		Single-ended/pseudo differential mode; ±2.5 V range			-78.9	
		Single-ended/pseudo differential mode; 0 V to +10 V and ±10 V ranges		-79		
Intermodulation Distortion	MD 3	f_A = 50 kHz, f_B = 30 kHz				
Second-Order Terms				-88		
Third-Order Terms				-90		
Aperture Delay 4/				7		ns
Aperture Jitter 4/				50		ps
Common-Mode Rejection	CMRR 3/	Up to 100 kHz ripple frequency; see FIURE 7		-79		dB
Channel-to-Channel Isolation 3/		f_{IN} on unselected channels up to 100 kHz; see FIGURE 6		-72		
Full Power Bandwidth		At 3 dB		22		MHz
		At 0.1 dB		5		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions $-55°C \le T_A \le +125°C$ 2/	Limits			Unit
			Min	Typ	Max	
DC Accuracy 5/ 6/						
Resolution			13			Bits
No Missing Codes		Differential mode	12 bit plus sign (13 bits)			
			11 bit plus sign (12 bits)			
Integral Nonlinearity 3/		Differential mode; V_{CC} = 3 V to 5.25 V, typical for V_{CC} = 2.7 V			±1.25	LSB
		Single-ended/pseudo differential mode, V_{CC} = 3 V to 5.25 V, typical for V_{CC} = 2.7 V			±1.2	
		Single-ended/pseudo differential mode (LSB = FSR/8192)		-0.7/+1.2		
Differential Nonlinearity 3/		Differential mode; guaranteed no missing codes to 13 bits			-0.99/+1.2	
		Single-ended mode; guaranteed no missing codes to 12 bits			±0.99	
		Single-ended/pseudo differential mode (LSB = FSR/8192)		-0.7/+1		
Offset Error 3/ 7/		Single-ended/pseudo differential mode			-6/+10	
		Differential mode			-7/+11	
Offset Error Match 3/ 7/		Single-ended/pseudo differential mode			±0.8	
		Differential mode			±0.5	
Gain Error 3/ 7/		Single-ended/pseudo differential mode			±8	
		Differential mode			±15	
Gain Error Match 3/ 7/		Single-ended/pseudo differential mode			±0.5	
		Differential mode			±0.5	
Positive Full Scale Error 3/ 8/		Single-ended/pseudo differential mode			±4	
		Differential mode			±8	
Positive Full Scale Error Match 3/ 8/		Single-ended/pseudo differential mode			±0.5	
		Differential mode			±0.5	
Bipolar Zero Error 3/ 8/		Single-ended/pseudo differential mode			±9	
		Differential mode			±8	
Bipolar Zero Error Match 3/ 8/		Single-ended/pseudo differential mode			±0.5	
		Differential mode			±0.5	
Negative Full Scale Error 3/ 8/		Single-ended/pseudo differential mode			±4	
		Differential mode			±7	
Negative Full Scale Error Match 3/ 8/		Single-ended/pseudo differential mode			±0.5	
		Differential mode			±0.5	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions $-55°C \le T_A \le +125°C$ 2/	Limits			Unit
			Min	Typ	Max	
Analog input						
Input Voltage Ranges 3/ (Programmed via Range Registers)		Reference = 2.5 V				V
		V_{DD} = +10 V min, V_{SS} = −10 V min, V_{CC} = +2.7 V to +5.25 V		±10		
		V_{DD} = +5 V min, V_{SS} = −5 V min, V_{CC} = +2.7 V to +5.25 V		±5		
		V_{DD} = +5 V min, V_{SS} = −5 V min, V_{CC} = +2.7 V to +5.25 V		±2.5		
		V_{DD} = +10 V min, V_{SS} = AGND min, V_{CC} = +2.7 V to +5.25 V		0 to 10		
Pseudo Differential V_{IN}(−)		V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = +5 V				
Input Range 3/		Reference = 2.5 V; range = ±10 V		±3.5		V
		Reference = 2.5 V; range = ±5 V		±6		
		Reference = 2.5 V; range = ±2.5 V		±5		
		Reference = 2.5 V; range = 0 V to +10 V v		±3/-5		
DC Leakage Current		V_{IN} = V_{DD} or V_{SS}			±80	nA
		Per input channel, V_{IN} = V_{DD} or V_{SS}		3		
Input Capacitance 4/		When in track, ±10 V range		13.5		pF
		When in track, ±5 V and 0 V to +10 V ranges		16.5		
		When in track, ±2.5 V range		21.5		
		When in hold, all ranges		3		
Reference Input/Output						
Input Voltage Range			2.5		3	V
Input DC Leakage Current					±1	µA
Input Capacitance				10		pF
Reference Output Voltage				2.5		V
Reference Output Voltage Error at 25°C					±5	mV
Reference Output Voltage T_{MIN} to T_{MAX}					±10	
Reference Temperature Coefficient					25	ppm/°C
				3		
Reference Output Impedance				7		Ω
Logic Inputs						
Input High Voltage	V_{IN}		2.4			V
Input Low Voltage	V_{IL}	V_{CC} = 4.75 V to 5.25 V			0.8	
		V_{CC} = 2.7 to 3.6 V			0.4	
Input Current	I_{IN}	V_{IN} = 0 V or V_{DRIVE}			±1	µA
Input Capacitance	C_{IN}			10		pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions $-55°C \le T_A \le +125°C$ 2/	Limits			Unit
			Min	Typ	Max	
Logic Outputs						
Output High Voltage	V_{OH}	I_{SOURCE} = 200 µA	V_{DRIVE} – 0.2 V			V
Output Low Voltage	V_{OL}	I_{SINK} = 200 µA			0.4	
Floating-State Leakage Current					±1	µA
Floating-State Output Capacitance				5		pF
Output Coding		Coding bit set to 1 in control register	(Straight natural binary Twos complement)			
		Coding bit set to 0 in control register				
Conversion rate						
Conversion Time		16 SCLK cycles with SCLK = 10 MHz			1.6	µs
Track-and-Hold Acquisition Time 3/ 4/		Full-scale step input			305	ns
Throughput Rate					500	kSPS
Power requirements (Digital inputs = 0 V or V_{DRIVE})						
V_{DD} 3/			12		16.5	V
V_{SS} 3/			-12		-16.5	
V_{CC} 3/			2.7		5.25	
V_{DRIVE}			2.7		5.25	
Normal Mode (Static)		V_{DD}/V_{SS} = ±16.5 V, V_{CC}/V_{DRIVE} = 5.25 V		0.9		mA
Normal Mode (Operational)		f_{SAMPLE} = 500 kSPS				
I_{DD}		V_{DD} = 16.5 V			195	µA
I_{SS}		V_{SS} = −16.5 V			215	µA
I_{CC} and I_{DRIVE}		V_{CC}/V_{DRIVE} = 5.25 V			2.3	mA
Autostandby Mode (Dynamic)		f_{SAMPLE} = 250 kSPS				
I_{DD}		V_{DD} = 16.5 V			100	µA
I_{SS}		V_{SS} = −16.5 V			110	µA
I_{CC} and I_{DRIVE}		V_{CC}/V_{DRIVE} = 5.25 V			0.87	mA
Autoshutdown Mode (Static)		SCLK on or off				
I_{DD}		V_{DD} = 16.5 V			1	µA
I_{SS}		V_{SS} = −16.5 V			1	µA
I_{CC} and I_{DRIVE}		V_{CC}/V_{DRIVE} = 5.25 V			1	µA
Fullshutdown Mode		SCLK on or off				
I_{DD}		V_{DD} = 16.5 V			1	µA
I_{SS}		V_{SS} = −16.5 V			1	µA
I_{CC} and I_{DRIVE}		V_{CC}/V_{DRIVE} = 5.25 V			1	µA
Power dissipation						
Normal Mode (Operational)		V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = +5.25 V			19	mW
Full Shutdown Mode		V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = +5.25 V			38.25	µW

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions -55°C ≤ T_A ≤ +125°C 9/	V_{CC} < 4.75 V			V_{CC} = 4.75 V to 5.25 V			Unit
			Min	Typ	Max	Min	Typ	Max	
Timing specifications									
	f_{SCLK}		5o			50			kHz
					10			10	MHz
	$t_{CONVERT}$	$t_{SCLK} = 1/f_{SCLK}$			16 x t_{SCLK}			16 x t_{SCLK}	ns
	t_{QUIET}	Minimum time between end of serial read and next falling edge of $\overline{CS}$	75			60			
	t_1	Minimum $\overline{CS}$pulse width	12			5			
	t_2	$\overline{CS}$ to SCLK set-up time; bipolar input ranges (±10 V, ±5 V, ±2.5 V)	25			20			
	10/	Unipolar input range (0 V to 10 V)	45			35			
	t_3	Delay from $\overline{CS}$ until DOUT three-state disabled			26			14	
	t_4	Data access time after SCLK falling edge			57			43	
	t_5	SCLK low pulse width	0.4 x t_{SCLK}			0.4 x t_{SCLK}			
	t_6	SCLK high pulse width	0.4 x t_{SCLK}			0.4 x t_{SCLK}			
	t_7	SCLK to data valid hold time	13			8			
	t_8	SCLK falling edge to DOUT high impedance			40			22	
		SCLK falling edge to DOUT high impedance	10			9			
	t_9	DIN set-up time prior to SCLK falling edge	4			4			
	t_{10}	DIN hold time after SCLK falling edge	2			2			
	$t_{POWER-UP}$	Power-up from autostandby			750			750	
		Power-up from full shutdown/autoshutdown mode, internal reference			500			500	µs
		Power-up from full shutdown/autoshutdown mode, external reference		25			25		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 12 V to 16.5 V, V_{SS} = - 12 V to -16.5 V, V_{CC} = 2.7 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, V_{REF} = 2.5 V to 3.0 V internal/external, f_{SCLK} = 10 MHz, fs = 500 kSPS, $T_A = T_{MAX}$ to T_{MIN}, unless otherwise noted.

3/ See the terminology section of the AD7327 from manufacturer data sheet.

4/ Sample tested during initial release to ensure compliance.

5/ For dc accuracy specifications, the LSB size for differential mode is FSR/8192. For single-ended mode/pseudo differential mode, the LSB size is FSR/4096, unless otherwise noted.

6/ Single-ended/pseudo differential mode 1 LSB = FSR/4096, unless otherwise noted; differential mode 1 LSB = FSR/8192, unless otherwise noted.

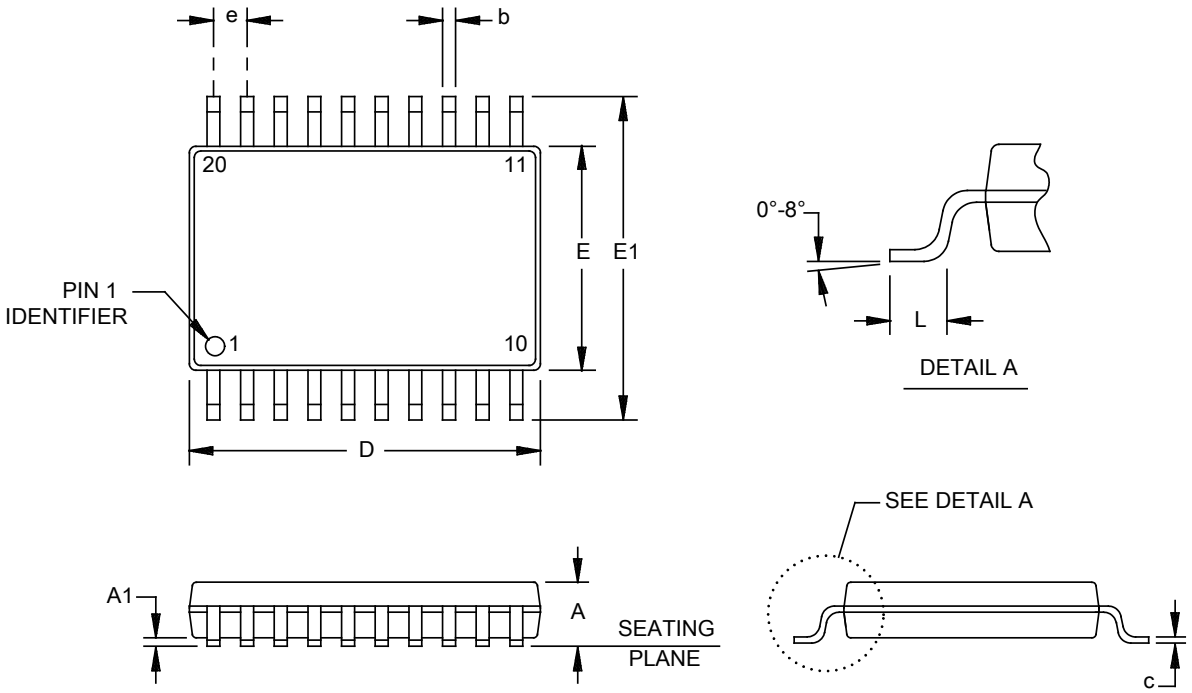
7/ Unipolar 0 V to 10 V range with straight binary output coding.

8/ Bipolar range with twos complement output coding.

9/ V_{DD} = 12 V to 16.5 V, V_{SS} = - 12 V to -16.5 V, V_{CC} = 2.7 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, V_{REF} = 2.5 V to 3.0 V internal/external, $T_A = T_{MAX}$ to T_{MIN}. Timing specifications apply with a 32 pF load, unless otherwise noted. Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V.

10/ When using the 0 V to 10 V unipolar range, running at 500 kSPS throughput rate with t_2 at 20 ns, the mark space ratio needs to be limited to 50:50.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.40 BSC	
b	0.19	0.30	e	0.65 BSC	
c	0.09	0.20	L	0.45	0.75
D	6.40	6.60			

NOTES:
1. All linear dimensions are in millimeters.
2. Compliant to JEDEC standard MO-153-AC.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{CS}$	20	SCLK
2	DIN	19	DGND
3	DGND	18	DOUT
4	AGND	17	VDRIVE
5	REFIN/OUT	16	V_{CC}
6	V_{SS}	15	V_{DD}
7	$V_{IN}0$	14	$V_{IN}2$
8	$V_{IN}1$	13	$V_{IN}3$
9	$V_{IN}4$	12	$V_{IN}6$
10	$V_{IN}5$	11	$V_{IN}7$

FIGURE 2. Terminal connections.

Terminal number	Terminal symbol	Description
1	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7327-EP and frames the serial data transfer.
2	DIN	Data In. Data to be written to the on-chip registers is provided on this input and is clocked into the AD7327-EP on the falling edge of SCLK (see the Registers section of AD7327 data sheet).
3, 19	DGND	Digital Ground. Ground reference point for all digital circuitry on the AD7327-EP. The DGND and AGND voltages, ideally, share the same potential and must not be more than 0.3 V apart, even on a transient basis.
4	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7327-EP. Refer all analog input signals and any external reference signal to this AGND voltage. The AGND and DGND voltages, ideally, share the same potential and must not be more than 0.3 V apart, even on a transient basis.
5	REFIN/OUT	Reference Input/Reference Output. The on-chip reference is available on this pin for external use to the AD7327-EP. The nominal internal reference voltage is 2.5 V, which appears at this pin. Place a 680 nF capacitor on the reference pin (see the Reference section of the AD7327 data sheet). Alternatively, the internal reference can be disabled and an external reference applied to this input. On power-up, the external reference mode is the default condition.
6	V_{SS}	Negative Power Supply Voltage. This is the negative supply voltage for the analog input section.
7, 8, 9, 10, 11, 12, 13, 14	$V_{IN}0$ to $V_{IN}7$	Analog Input 0 to Analog Input 7. The analog inputs are multiplexed into the on-chip track-and-hold. The analog input channel for conversion is selected by programming the channel address Bit ADD2 through Bit ADD0 in the control register. The inputs can be configured as eight single-ended inputs, four true differential input pairs, four pseudo differential inputs, or seven pseudo differential inputs. The configuration of the analog inputs is selected by programming the mode bits, Bit Mode 1 and Bit Mode 0, in the control register. The input range on each input channel is controlled by program-ming the range registers. Input ranges of ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V can be selected on each analog input channel when a +2.5 V reference voltage is used (see the Registers section of AD7327 data sheet).
15	VDD	Positive Power Supply Voltage. This is the positive supply voltage for the analog input section.

FIGURE 3. Terminal function.

Terminal number	Terminal symbol	Description
16	VCC	Analog Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for the ADC core on the AD7327-EP. Decouple this supply to AGND.
17	VDRIVE	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Decouple this pin to DGND. The voltage at this pin may be different to that at V_{CC}, but it must not exceed V_{CC} by more than 0.3 V.
18	DOUT	Serial Data Output. The conversion output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input, and 16 SCLKs are required to access the data. The data stream consists of three channel identification bits, the sign bit, and 12 bits of conversion data. The data is provided MSB first (see the Serial Interface section of AD7327 data sheet).
20	SCLK	Serial Clock, Logic Input. A serial clock input provides the SCLK used for accessing the data from the AD7327-EP. This clock is also used as the clock source for the conversion process.

FIGURE 3. Terminal function - Continued.

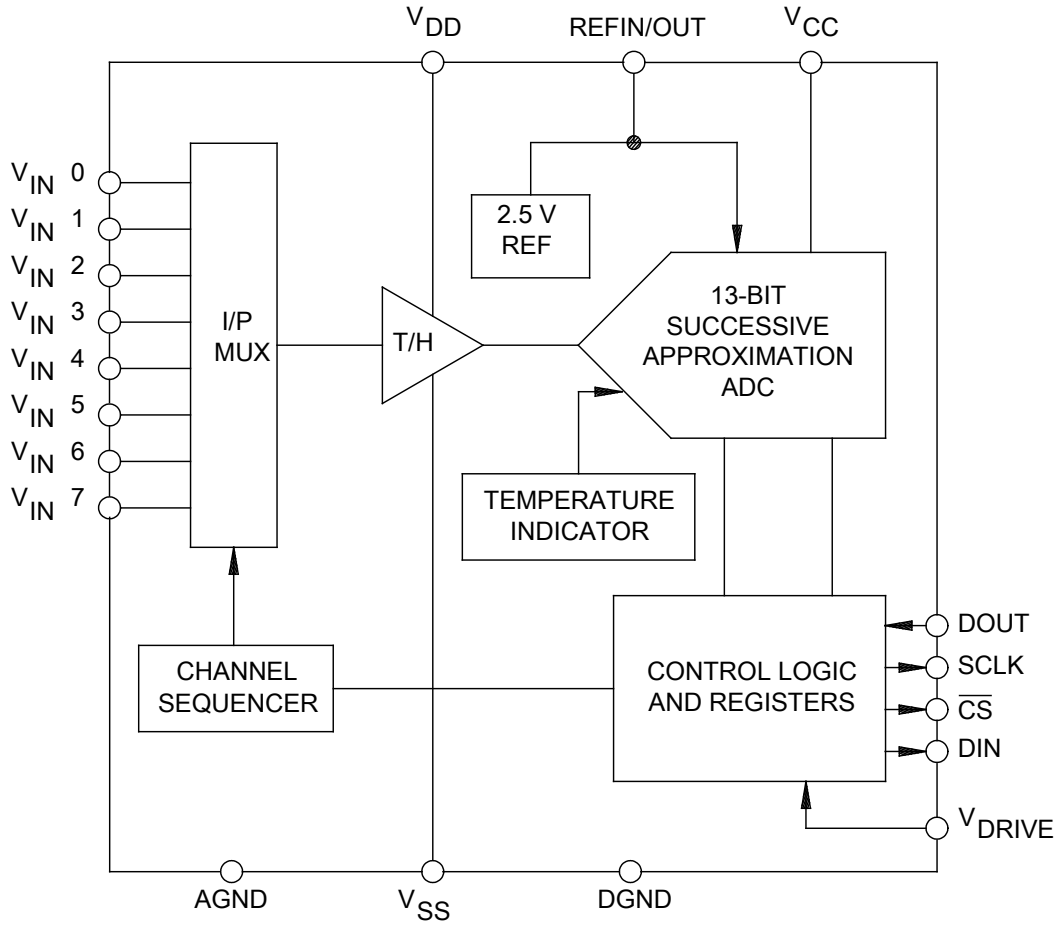


FIGURE 4. Functional block diagram.

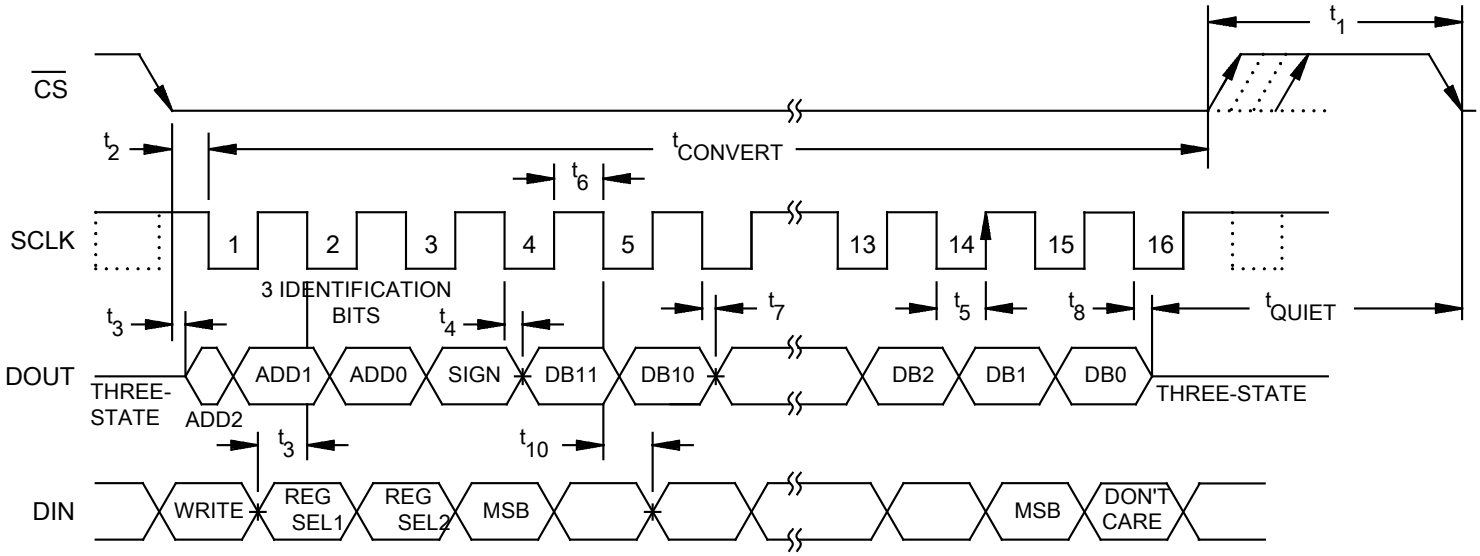


FIGURE 5. Serial interface timing diagram.

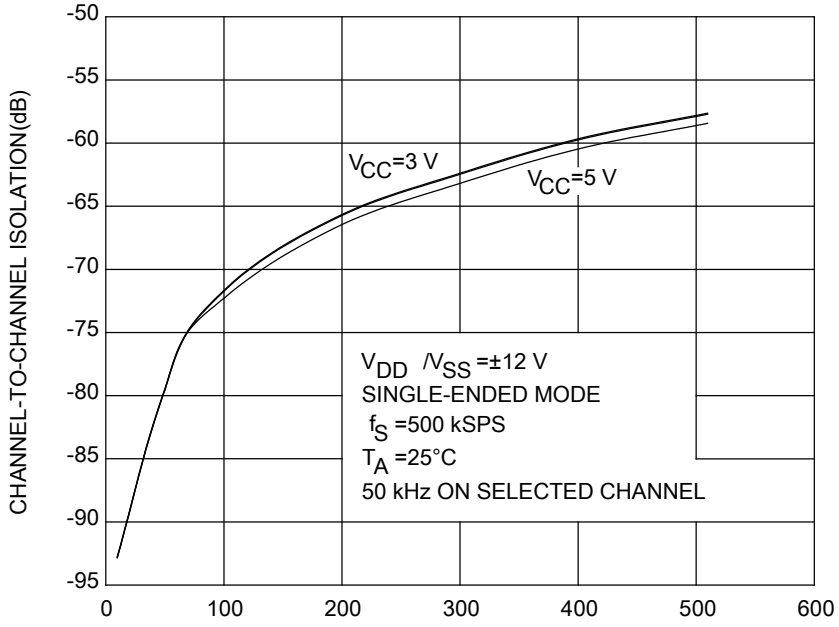


FIGURE 6. Channel to channel isolation.

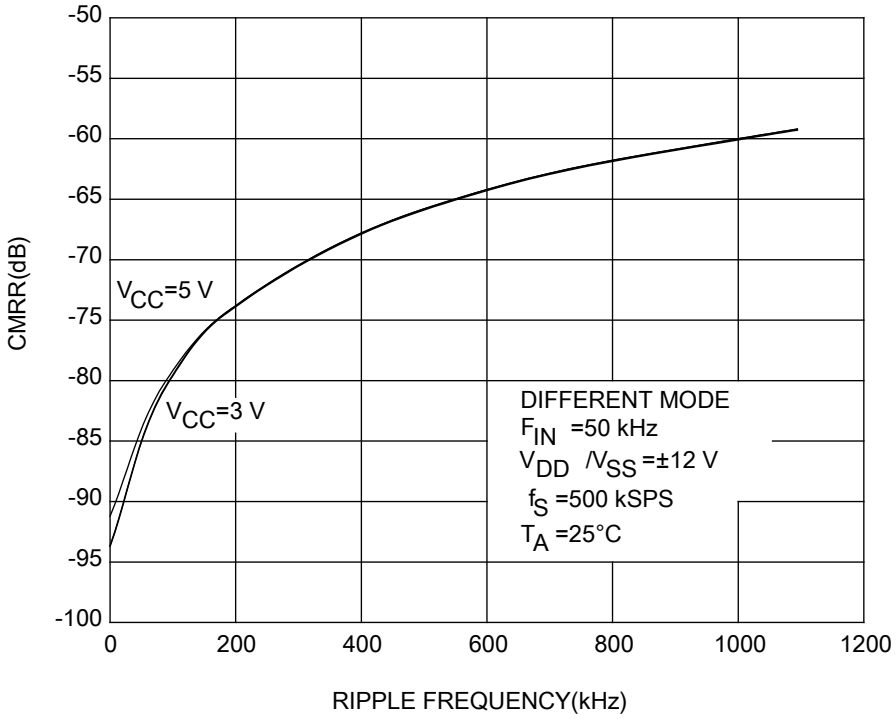


FIGURE 7. CMRR vs Common Mode Ripple frequency.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/14636-01XB	24355	AD7327TRU-EP
		AD7327TRU-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106