

Evaluating the **SSM3515** 25 W, Filterless, Class-D, Digital Input Audio Amplifier

FEATURES

- Filterless digital input, mono Class-D amplifier
- Operates from a single 4.5 V to 17 V supply
- 25 W output power, 16 V supply and 4 Ω load at 1% THD + N
- 107 dB A-weighted signal-to-noise ratio
- 93.3% efficiency into 8 Ω load at 12 V
- I²C control with up to 4 pin-selectable slots/addresses
- Digital interface supports sample rates from 8 kHz to 192 kHz
- Flexible digital and analog gain adjustment
- Flexible supply monitoring AGC function
- Short-circuit and thermal protection, thermal warning

EVALUATION KIT CONTENTS

- [EVAL-SSM3515Z](#) evaluation board
- [EVAL-ADUSB2EBZ](#) USB interface board (USBi)
- User GUI with [SigmaStudio](#) software (download from [product page](#))

DOCUMENTS NEEDED

- [SSM3515](#) data sheet
- [EVAL-SSM3515Z](#) user guide

GENERAL DESCRIPTION

The [EVAL-SSM3515Z](#) is an evaluation board for quick evaluation of the [SSM3515](#). The board uses a single supply from 4.5 V to 17 V. The board includes 3.3 V and 1.8 V regulators. The on-board digital SPDIF optical input generates the serial digital signal to the [SSM3515](#). The board provides register control using USBi with [SigmaStudio](#)™-based GUI or the Total Phase Aardvark™ I²C/SPI Host Adapter. The application circuit requires a minimum of external components and can operate from a single 4.5 V to 17 V supply. It is capable of delivering 8 W of continuous output power into an 8 Ω load, and 15 W into a 4 Ω load from a 12 V power supply. The board can deliver 25 W into a 4 Ω load from a 16 V power supply, all with <1% total harmonic distortion + noise (THD + N); however, output powers above 20 W are not continuous due to the thermal limit.

This user guide describes how to configure and use the [EVAL-SSM3515Z](#) evaluation board. When using the evaluation board, consult this user guide in conjunction with the [SSM3515](#) data sheet, which provides specifications, internal block diagrams, and application guidance for the amplifier IC.

The [EVAL-SSM3515Z](#) evaluation board includes a complete circuit for driving a loudspeaker. Figure 1 shows the top view of the evaluation board, and Figure 2 shows the bottom view of the evaluation board.

EVALUATION BOARD TOP VIEW AND BOTTOM VIEW

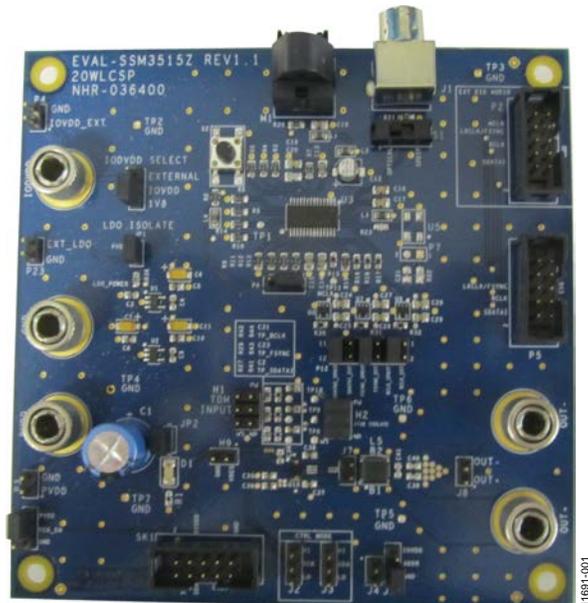


Figure 1. [EVAL-SSM3515Z](#) Evaluation Board Top View

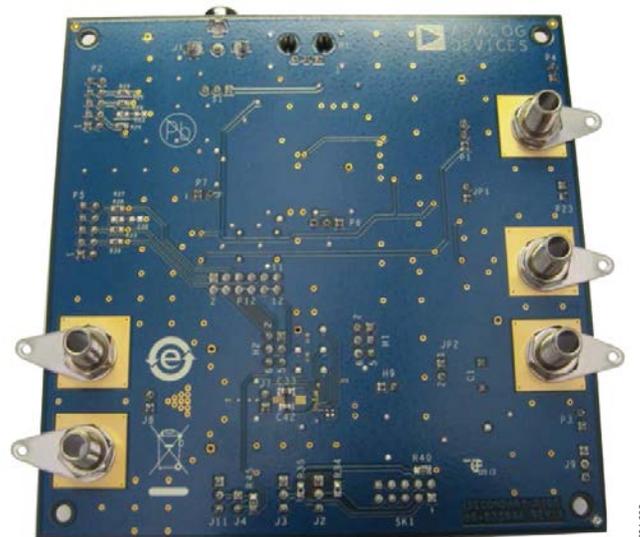


Figure 2. [EVAL-SSM3515Z](#) Evaluation Board Bottom View

TABLE OF CONTENTS

Features	1	I ² C Control Port.....	4
Evaluation Kit Contents.....	1	Output Configuration.....	5
Documents Needed.....	1	Edge Mode.....	5
General Description	1	Component Selection	5
Evaluation Board Top View and Bottom View.....	1	Getting Started.....	6
Revision History	2	USBi and SigmaStudio Install.....	6
Evaluation Board Hardware Overview.....	3	Evaluation Board Startup	6
Setting Up the Hardware	4	I ² C Writes for Board Startup.....	10
Power Supply Configuration.....	4	Evaluation Board Schematics and Artwork.....	11
Regulator Enable.....	4	Ordering Information.....	18
Digital Audio Input	4	Bill of Materials.....	18
Input Configuration	4		

REVISION HISTORY

9/15—Rev. 0 to Rev. A

Change to Figure 1	1
Change to Figure 12	13
Change to Figure 13	14
Change to Figure 19	17

6/15—Revision 0: Initial Version

EVALUATION BOARD HARDWARE OVERVIEW

The evaluation board includes all the hardware required for quick evaluation of the [SSM3515](#). The board needs an external, high current, low noise power supply with 4.5 V to 17 V and 5 A current capability. The board needs either an optical SPDIF or serial I²S/TDM-compatible audio source. The board provides

the 10-pin header for connecting an external I²C control device, such as the USBi (included with the kit) or Aardvark I²C/SPI controller via USB to control the internal registers. The loudspeaker with 4 Ω to 8 Ω impedance can be connected directly for listening.

SETTING UP THE HARDWARE

POWER SUPPLY CONFIGURATION

The PVDD and GND binding posts are used to power the board. Take care to connect the dc power with correct polarity and voltage. Reverse polarity or overvoltage can damage the board permanently. The supply voltages range is from 4.5 V to 17 V; higher voltages can damage the amplifier. Alternately, the P3 2-pin, 0.1 inch header can be used to connect the external supply. When inserted, JP2 turns on the power-on LED.

U1 is a 3.3 V regulator included to power up the on-board SPDIF receiver. JP1 provides the input to the 3.3 V regulator. If the on-board SPDIF receiver is used, JP1 must be inserted.

The U2 regulator is included as an option to provide the 1.8 V (DVDD) power to the [SSM3515](#) and other on-board supporting circuits. Alternately, the external 1.8 V source can be connected via the IOVDD binding post. Use P1 to select the external vs. internal 1.8 V source.

REGULATOR ENABLE

In addition to the 4.5 V to 17 V power supply, a voltage must be present to activate the integrated voltage regulators on the [SSM3515](#). The [SSM3515](#) amplifier has an internal regulator to provide a clean internal 5 V (AVDD) rail, as well as an internally generated 1.8 V (DVDD) rail.

When the REGEN pin is pulled high, by connecting the top two pins of J9 (REG_EN to PVDD), the internal DVDD regulator is enabled. If the REGEN pin is pulled low, the regulators are disabled and the 1.8 V DVDD must be present for the [SSM3515](#) to function.

DIGITAL AUDIO INPUT

M1 and J1 on the evaluation board provide the SPDIF optical or coaxial input connectors. The S1 switch selects the desired source. The U3 IC receives the SPDIF signal and generates the serial digital output suitable for the [SSM3515](#). The default format is set as I²S, 2-channel with 32 bits/channel. The serial outputs are level shifted to 1.8 V using U6, U7, and U8 before feeding to the [SSM3515](#). Alternatively, a suitable I²S/TDM-compatible source such as a DSP serial port or Audio Precision digital serial port can be connected at P2. The P12 header selects either the SPDIF or external source.

INPUT CONFIGURATION

There are several ways to source audio to the [SSM3515](#) on the evaluation board. The evaluation board can accept direct I²S/TDM data or it can convert from 2-channel SPDIF/optical digital audio data to I²S using an on-board digital audio receiver (CS8416-CZZ).

To make a connection from either the on-board audio receiver circuitry or the P2 external digital audio header to the [SSM3515](#) device pins, jumpers must be inserted across all three rows of H2. In some use cases, such as high speed clocking of data, remove the jumpers across H2 to reduce stub length and

minimize parasitics. In this case, source digital audio data on the H1 header block.

When using an I²S or TDM source, such as from Audio Precision, it is recommended to source the input audio signals directly to the FSYNC, BCLK, and SDATAI pins of the P2 header block. When connecting multiple [SSM3515](#) evaluation boards on the same digital audio bus in a daisy-chain configuration, note that the P5 header port has the same direct connections to the [SSM3515](#) pins.

To route the externally sourced I²S or TDM data to the [SSM3515](#) pins, insert jumpers across SDATAI_EXT, FSYNC_EXT, and BCLK_EXT on the P12 header block.

If the user does not have a direct I²S or TDM source, the on-board digital audio receiver can accept SPDIF data from a digital audio source, such as the digital audio output of a compact disk player. In this case, select either optical or SPDIF on the S1 switch to properly connect the desired input to the digital audio receiver.

To route the on-board converted SPDIF-to-I²S data to the [SSM3515](#) pins, insert jumpers across SDATAI_INT, FSYNC_INT, and BCLK_INT on the P12 header block. Note that the audio performance is limited to that of the on-board digital audio receiver (CS8416-CZZ).

I²C CONTROL PORT

The [SSM3515](#) supports I²C control with the state of the ADDR pin (J11 and J4) determining the I²C device address. Inserting a jumper across J4 shorts across a 47 k Ω resistor. Removing the jumper across J4 inserts the resistor in the signal path for pull-up or pull-down operation. A jumper inserted across the top two pins of J11 pulls the ADDR pin to a high state (IOVDD), whereas inserting a jumper across the bottom two pins of J11 pulls the ADDR pin to a low state (GND). To set the ADDR pin to open condition, insert a jumper across J4 and do not insert jumpers on J11.

Table 1. ADDR Pin Configuration

I ² C Address	TDM Slot	J11 (ADDR)	J4	Configuration
0x14	1	GND	Open	ADDR pin connected through 47 k Ω to GND
0x15	2	Open	Short	ADDR pin unconnected
0x16	3	IOVDD	Open	ADDR pin connected through 47 k Ω to IOVDD
0x17	4	IOVDD	IOVDD	ADDR pin directly connected to IOVDD
N/A ¹	N/A ¹	GND	Short	Not an option

¹ N/A means not applicable.

The SK1 10-pin header connects the USBi (provided with the kit) for I²C control of the device.

OUTPUT CONFIGURATION

The OUT– and OUT+ output terminals connectors provide convenient attachment points for speakers or other load devices with standard banana connectors. In addition, 2-pin, 0.100 inch headers are provided. J7 is inserted before the EMI filtering portion, and J8 is inserted after the EMI filtering portion. Because the SSM3515 does not typically require any external audio band LC output filtering due to a low noise modulation scheme, a low cost, high performance common-mode, choke-based filter can optionally be inserted on the evaluation board for EMI suppression.

For optimal performance measurement, remove this filtering by inserting 0 Ω links or a thick wire short across B1 and B2. In this case, leave the C39 to C41 filter capacitors unpopulated.

To safeguard against system radiated emission failure, especially if the speaker cable length exceeds 20 cm, it may be necessary to include an output filter. The recommended filter uses a common-mode choke, L5 in the output path, plus capacitors, C39 to C41, to couple the output terminals to ground. A schematic of this configuration is shown in Figure 10, with recommended values for the filter components given. The recommended common-mode chokes are listed in Table 2.

Alternatively, a carefully selected pair of ferrite beads can be used in place of the common-mode choke to save space. Take care with the component selection to avoid degradation of THD + N or signal-to-noise ratio (SNR) as a result of the nonlinear performance of the ferrite beads. A summary of the recommended ferrite beads is shown in Table 3.

For the best THD and SNR performance as specified in the SSM3515 data sheet, remove the output filters and insert a short across L1 and L2.

EDGE MODE

To reduce the radiated emissions from the SSM3515 amplifier, an edge rate control mode is available. To enable the reduced EMI mode, send an I²C control register write to activate Bit D4 of Register 0x01. The efficiency is slightly reduced when low EMI mode is enabled. To return to the ordinary (fast edge) operating mode, write a 0 to Bit D4 of Register 0x01.

COMPONENT SELECTION

Selecting the proper components is the key to achieving the performance required at the cost budgeted.

Common-Mode Choke Coil—L5

The L5 common-mode choke coil is a necessary component for filtering out the EMI caused at the switching output nodes when the length of the speaker wire is greater than 20 cm. Recommended components are shown in Table 2.

Output Shunt Capacitors

There are three output shunt capacitors, C39 to C41, that work with the L1 common-mode chokes coil. Use small size (0603 or 0402), multilayer ceramic capacitors made of X7R or C0G (NP0) materials. The recommended value is 220 pF.

Output Ferrite Beads

If ferrite beads are preferred for EMI filtering at the output nodes, choose only the selected ferrite beads in Table 3 to avoid excessive noise induced by the nonlinear behavior of ferrite beads.

Table 2. Recommended Common-Mode Chokes

Part No. ¹	Manufacturer	Z (Ω at 100 MHz)	I _{MAX} (mA)	DCR (Ω)	Size (mm)
DLW5BTN251SQ2	Murata Manufacturing Co.	250	5000	0.014	5.0 × 5.0 × 2.35
DLW5BTN101SQ2	Murata Manufacturing Co.	100	6000	0.009	5.0 × 5.0 × 2.35

¹ Contact Murata Manufacturing Co. for further options.

Table 3. Recommended Output Ferrite Beads

Part No.	Manufacturer	Z (Ω at 100 MHz)	I _{MAX} (mA)	DCR (Ω)	Size (mm)
NFZ2MSM101SN10	Murata Manufacturing Co.	100	4000	0.014	2.0 × 1.6 × 0.9
NFZ2MSM181SN10	Murata Manufacturing Co.	180	3400	0.020	2.0 × 1.6 × 0.9
NFZ2MSM301SN10	Murata Manufacturing Co.	300	3100	0.024	2.0 × 1.6 × 0.9

GETTING STARTED

USBi AND SigmaStudio INSTALL

To use USBi and SigmaStudio-based GUI, follow these steps:

1. Download the SigmaStudio software suitable for your PC from the SigmaStudio page at www.analog.com/SigmaStudio.
2. Open the downloaded .zip file.
3. For 64-bit operating systems, double click **SigmaStudio-Rel3.11-x64.exe**. For 32-bit operating systems, double-click **SigmaStudio-Rel3.11-x86.exe**.
4. Follow the installation steps as prompted and install the USBi driver as the final step.
5. The **SStudio.exe** file is installed by default to the folder **Program Files\Analog Devices\SigmaStudio3.11**.
6. Double click **SStudio.exe**. If the window shown in Figure 3 appears, the SigmaStudio software has been installed. Proceed to evaluation board startup.

EVALUATION BOARD STARTUP

To start up the evaluation board using single supply, follow these steps:

1. Ensure that the output filter is installed or 0 Ω links are in place to connect the output terminals to the IC.
2. Place a jumper between the upper two pins of J9 (REG_EN to PVDD) to enable the on-chip 1.8 V regulator.
 - a. In the bottom right corner, place a jumper across the bottom pins of J11, and open J4 (ADDR pull-down to GND) to select the device I²C address of 0x28, or 0x14 if using the Aardvark adapter.
3. Select the digital audio source for the SDATAI, FSYNC, and BCLK pins of the SSM3515. If using the SPDIF source,

select the _INT signal paths on P12. If sourcing via the Audio Precision I²S/TDM output, select the _EXT signal paths on P12 and connect digital audio signals via the Audio Precision connection to P2. Note that P5 allows multiple evaluation boards to be daisy-chained to the same signal bus.

4. Insert jumpers across all three rows of H2 to establish direct connection of the digital audio signal lines to the inputs of the SSM3515. For special use cases, to minimize stub length, remove the jumpers across H2 and source digital audio signals directly to the ports of H1.
5. If using the on-board SPDIF-to-I²S converter instead of the external digital audio port for Audio Precision, insert jumpers across JP1 and the bottom two terminals of P1 (IOVDD to 1V8) to power the level translators for digital audio signals.
6. Connect a USBi or Total Phase Aardvark USB-to-I²C adapter to SK1.
7. Connect a suitable 4 Ω to 8 Ω speaker to the left and right banana jacks.
8. Connect a power supply to the PVDD and GND binding posts. Turn on the power supply.
9. If using the Total Phase Aardvark USB-to-I²C adapter, use Device Address 0x14 and write the appropriate I²C commands to activate the SSM3515. Setting SPWDN (Bit D0 of Register 0x00) to 0 activates the device.
10. If using SigmaStudio, ensure that the USBi is connected to the USB port on the PC and that the 10-pin header is connected at SK1.

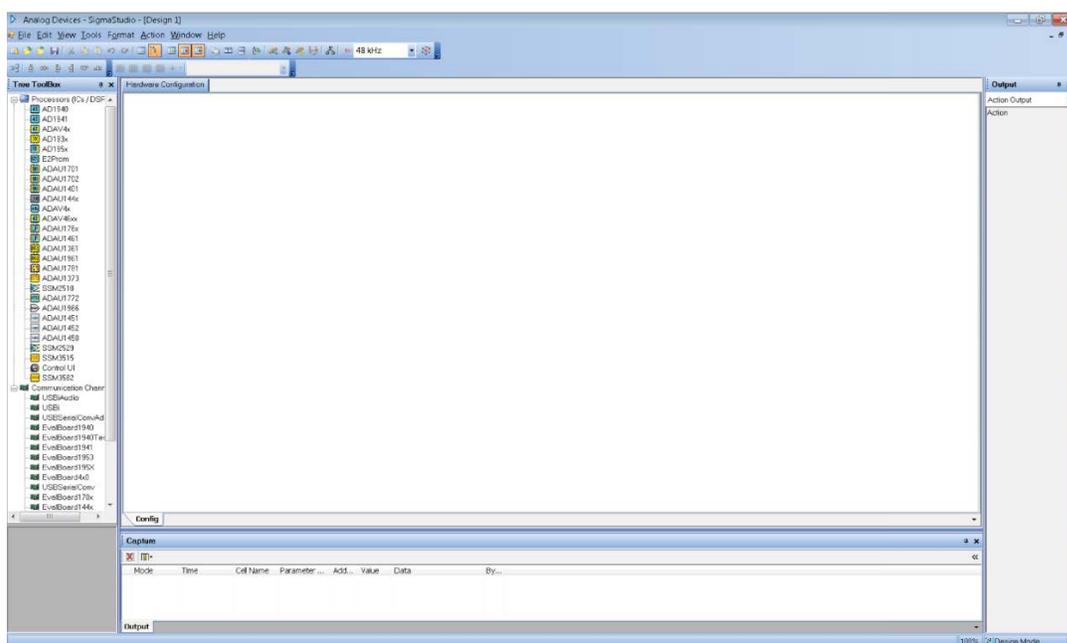


Figure 3. SigmaStudio GUI Start Window

11. In the SigmaStudio window, under the **File** menu, click **New Project** (see Figure 3).
12. From the **Tree Toolbox**, under **Processors (ICs/DSPs)**, drag the **SSM3515** block to the schematic page; and from under **Communication Channel**, drag the **USBi** block onto the schematic page. Using the mouse, connect the two as shown in Figure 5.
13. If the I²C communication failure message appears, as shown in Figure 4, the board is not set up correctly.
 - a. If the yellow light on USBi flickers, disconnect and try reconnecting the USB connector from the USBi board.
 - b. Check if the SCL/SDA signal lines at J2-2 and J3-2 are pulled to high.
 - c. Check the 1.8 V IOVDD on P1-2.

If the error persists, further debug for I²C is required before proceeding further.

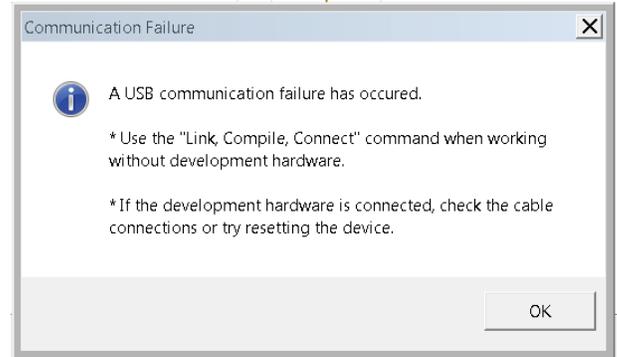


Figure 4. PC Communication Failure Message

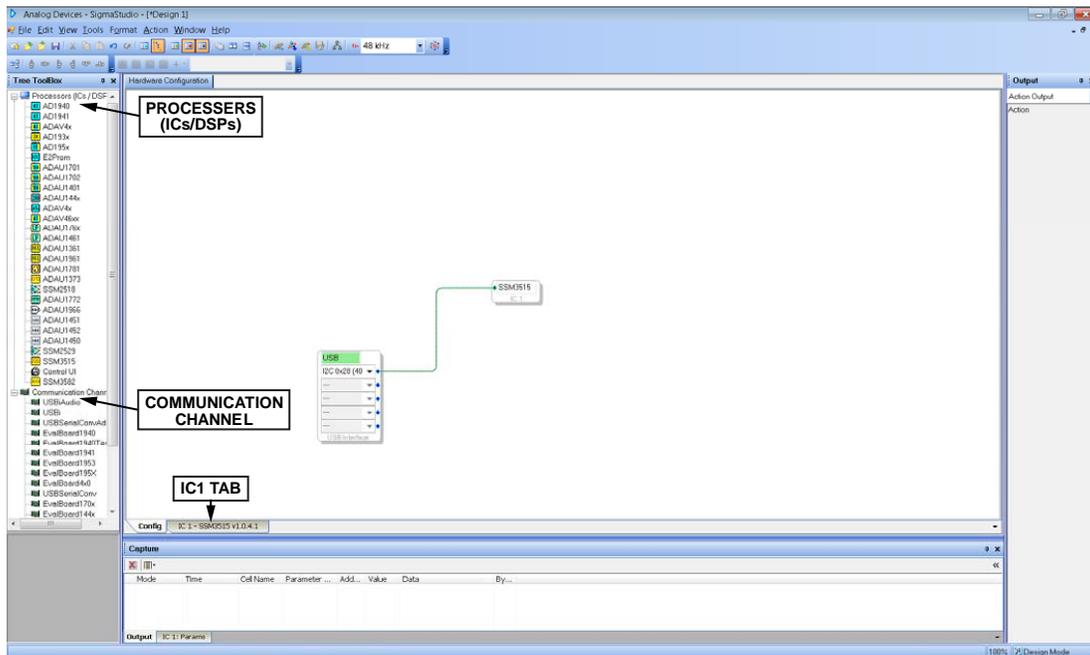


Figure 5. New Project Setup

14. Click the **IC 1** tab to bring up the register control screen for the [SSM3515](#) (see Figure 5).
15. Under **Master Software Powerdown**, select **Normal Operation** (see Figure 6).
16. If using the on-board SPDIF-to-I²S circuitry, press the **S2** button to reset the SPDIF receiver. After reset, the BCLK, FSYNC, and SDATAI signals are available at Header H2.
17. If using the Audio Precision PSIA, the digital serial signals must be made available at Header P2.
18. Click the **Chip/DAC Control** tab in the GUI (see Figure 6). This tab provides the power-up, mute, volume control, and gain settings.
19. Next, select the desired analog gain under **Amp Analog Gain Selection**.

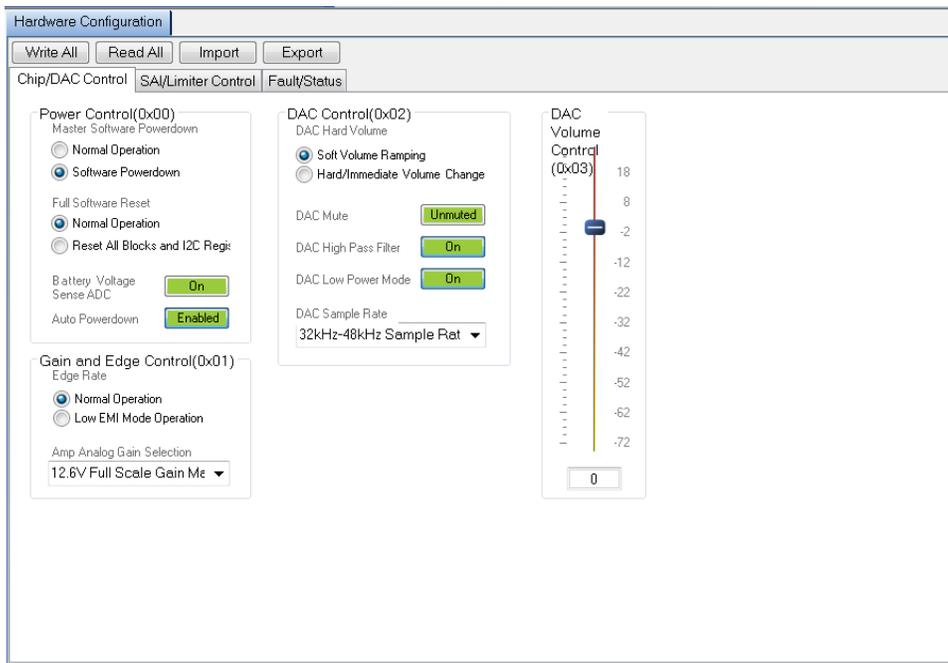


Figure 6. Chip/DAC Control Tab

11681-106

20. In the **SAI/Limiter Control** tab, under **SAI Control 1**, select **Stereo Mode** (see Figure 7). If clock and data signals are present, the **SSM3515** switching outputs are available at Connector J8 and audio can be heard from the connected speaker.

21. Click the **Chip/DAC Control** tab in the GUI (see Figure 6). Under **Master Software Powerdown**, select **Normal Operation** to power up the chip.
22. The **Fault/Status** tab provides the settings for faults and status (see Figure 8). Click **Read Status**. If no faults exist, all indicators are green.

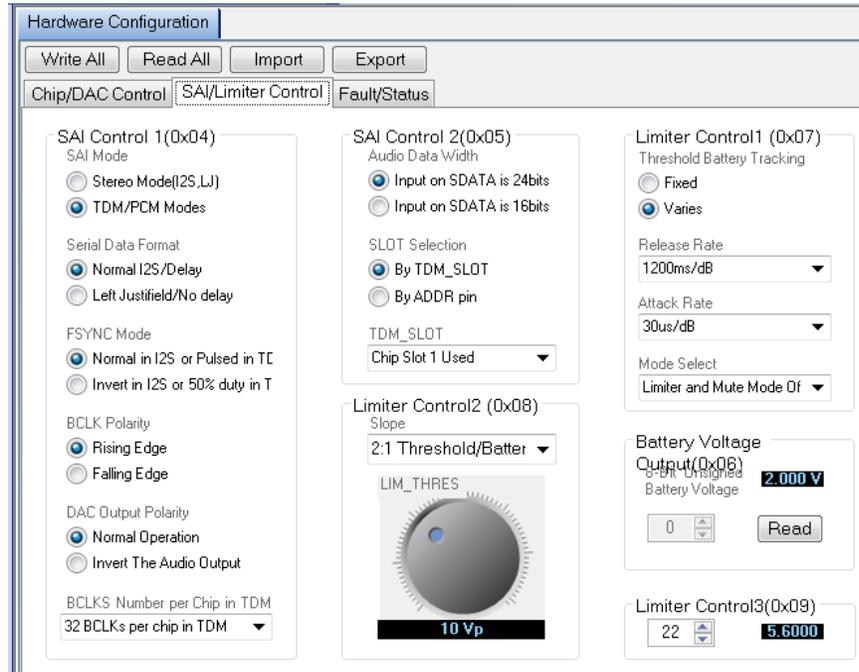


Figure 7. Serial Audio Interface and Limiter Control Tab

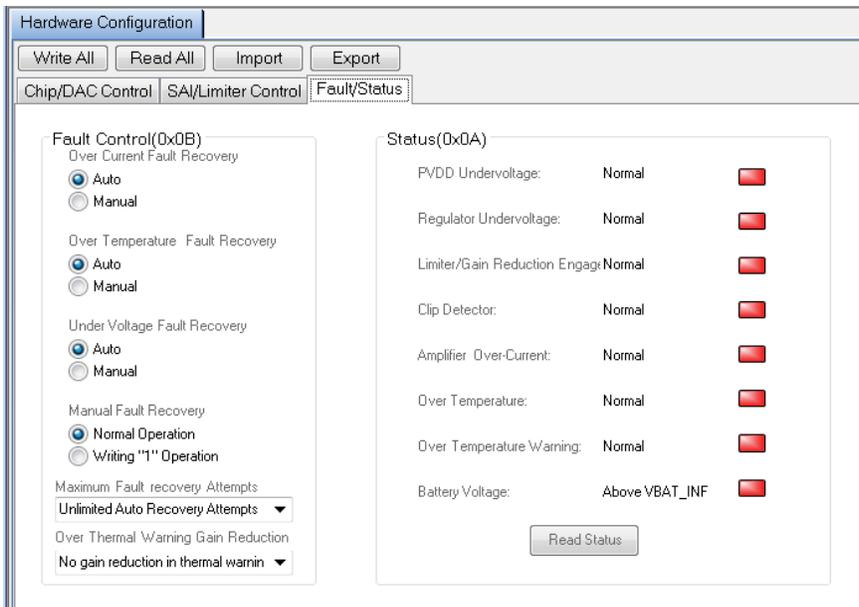
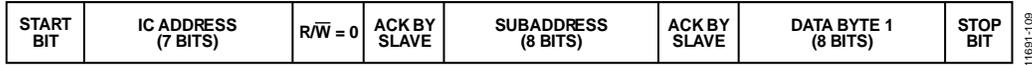


Figure 8. Fault/Status Tab

I²C WRITES FOR BOARD STARTUP

To start up the board, only Register 0x00 needs to be written. Set the SPWDN bit to 0 (that is, set Register 0x00 to 0x80). If the BCLK, FSYNC, and SDATA are present with required supply voltages, writing to this register wakes up the board from power-down. For I²C details, see the [SSM3515](#) data sheet. Typical I²C writes are 3 bytes, with the first byte containing the

device address, followed by the register address, followed by register data. Figure 9 shows a typical I²C single-word write sequence. The default 7-bit device address set on the board is 0x14. If set differently from the default value, use that address for the IC address bits. Set the subaddress as 0x00 and Data Byte 1 as 0x80. Following the I²C write, the device pulls the SDA line low during the acknowledge bit period.



11691-109

Figure 9. Single-Word I²C Write Format

EVALUATION BOARD SCHEMATICS AND ARTWORK

POWER SUPPLY

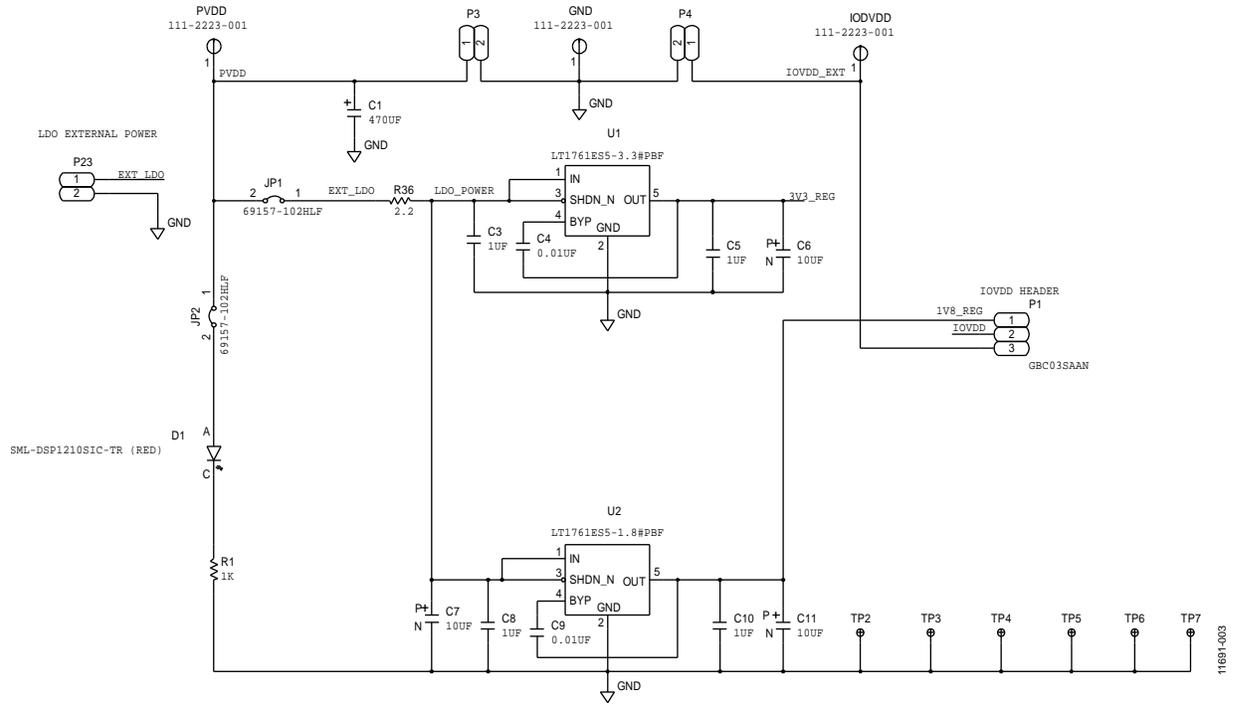


Figure 10. Evaluation Board Power Supply Section

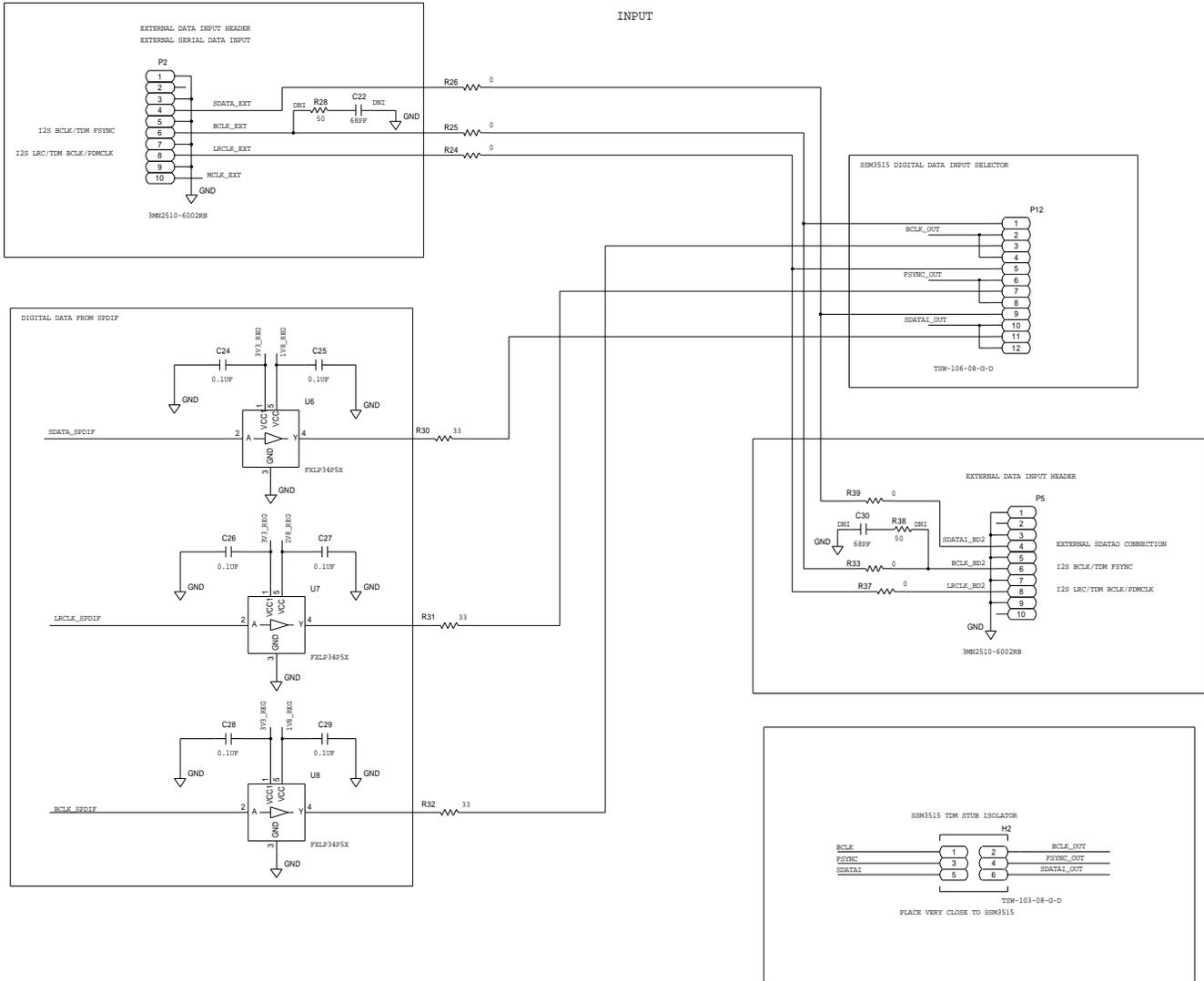
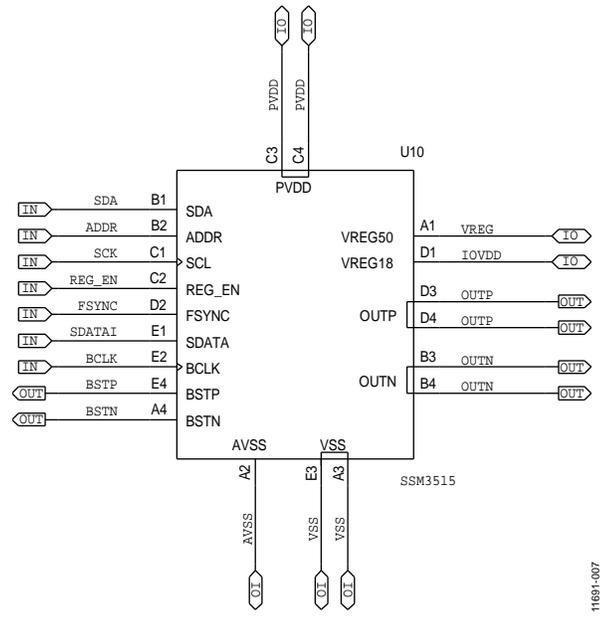


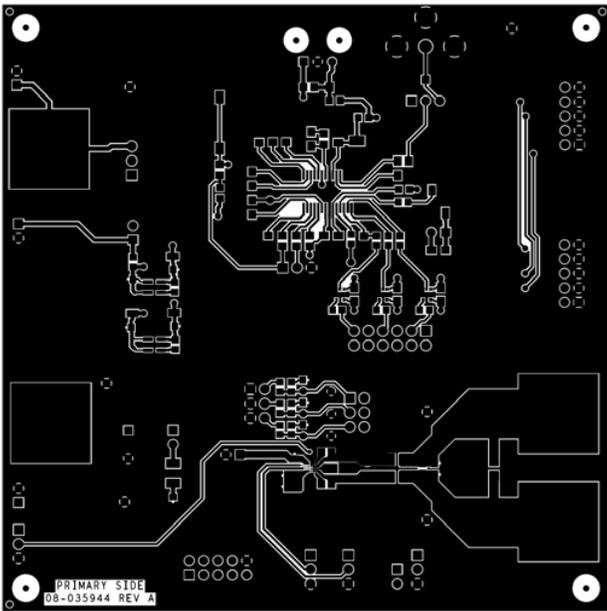
Figure 12. Evaluation Board Digital Input Routing/Level Shifting Section

11691-005



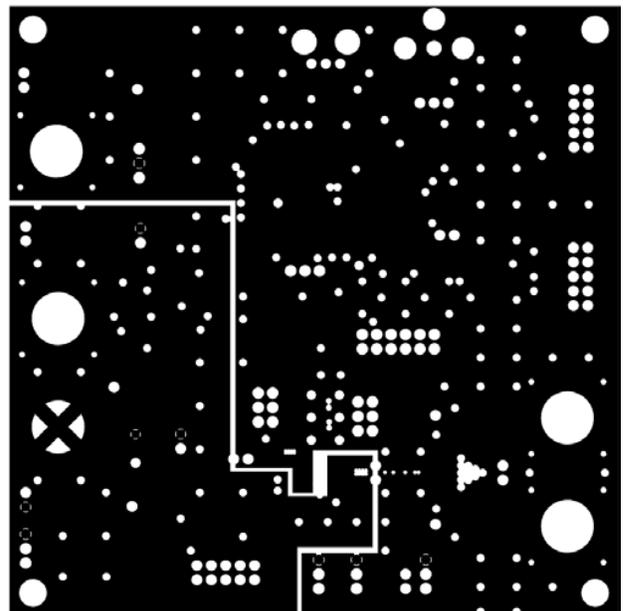
11891-007

Figure 14. Evaluation Board Device Pinout



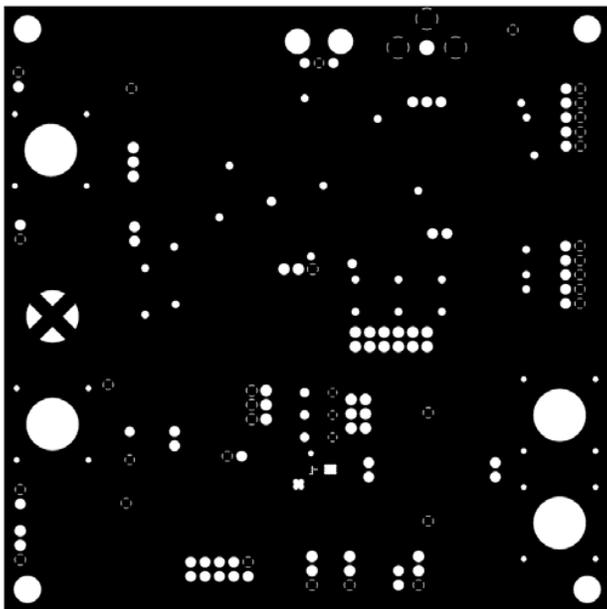
11691-008

Figure 15. Evaluation Board Top Layer Copper



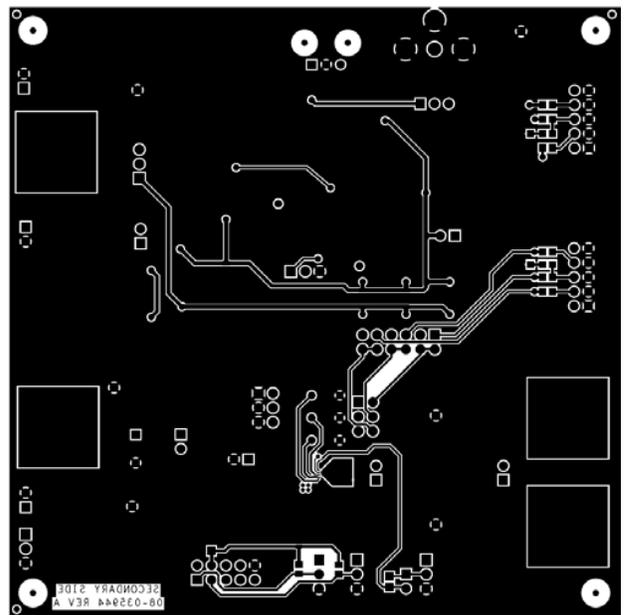
11691-010

Figure 17. Evaluation Board Third Layer Copper



11691-009

Figure 16. Evaluation Board Second Layer Copper



11691-011

Figure 18. Evaluation Board Bottom Layer Copper

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Qty	Reference Designator	Description	Supplier	Part No.
1	C1	Capacitor, electrolytic, 470 μ F, 35 V	Nichicon	UKA1V471MPD1TD
5	C3, C5, C8, C10, C36	Capacitor, ceramic, X5R, 0603, 1 μ F, 16 V	Murata	GRM188R61C105KA93D
3	C6, C7, C11	Capacitor, tantalum, 10 μ F, 10 V	AVX	TAJA106K010RNJ
1	C12	Capacitor, electrolytic, 10 μ F, 16 V	United Chemi-Con	MV16VC10RMD55TP
11	C13 to C15, C18, C21, C24 to C29	Capacitor, ceramic, X7R, 0805, 0.1 μ F, 50 V	Murata	GRM21BR71H104KA01L
2	C16, C17	Capacitor, ceramic, X7R, 0805, 1000 pF, 250 V	AVX	0805PC103KAT1A
1	C19	Capacitor, ceramic, X7R, 0805, 0.022 μ F, 50 V	Murata	GRM216R71H223KA01D
3	C2, C23, C31	Capacitor, ceramic, NPO, 0603, 33 pF, 50 V	Phycomp (Yageo)	CC0603JRNPO9BN330
1	C20	Capacitor, ceramic, COG, 0805, 1000 pF, 50 V	Murata	GRM2165C1H102JA01D
1	C33	Capacitor, ceramic, 0805, 10 μ F, 16 V	Murata	GRM21BR61C106KE15L
1	C34	Capacitor, ceramic, X7R, 0603, 2.2 μ F, 10 V	Murata	GRM188R71A225KE15D
2	C35, C42	Capacitor, ceramic, X8R, 0603, 0.1 μ F, 25 V	TDK	C1608X8R1E104K
2	C37, C38	Capacitor, ceramic, X7R, 0603, 0.22 μ F, 50 V	Murata	GCM188R71H224KA64D
2	C4, C9	Capacitor, ceramic, X7R, 0603, 0.01 μ F, 50 V	Phycomp (Yageo)	2238 586 15636
1	D1	LED, wtr clr, 1210, SMD (red)	Lumex	SML-DSP1210SIC-TR
5	GND, OUT+, OUT-, PVDD, IODVDD	Connector, PCB, banana jack uninsulated STD (Version 2 footprint)	Johnson	108-0740-001
2	H1, H2	Connector, PCB, berg header double STR male 6P	SAMTEC	TSW-103-08-G-D
7	H9, J4, J7, J8, P3, P4, P23	Connector, PCB, header, assy, breakaway st	Tyco Electronics	9-146285-0-02
1	J1	Connector, PCB, jack mt, right angle, yellow	Connect-Tech	CTP-021-A-S-Y
6	J2, J3, J9, P1, P6, J11	Connector, PCB, wire to board, header	Molex	22-03-2031
3	P7, JP1, JP2	Connector, PCB, berg jumper st male 2P, 1X M000385	FCI	69157-102HLF
1	M1	MOD photolink fiber optic receiver	Everlight	PLR135/T9
1	P12	Connector, PCB, berg header, st male 12P	SAMTEC	TSW-106-08-G-D
3	P2, P5, SK1	Connector, PCB, low profile straight thru hole, 2500 series	3M	N2510-6002RB
1	R1	Resistor, precision thick film chip, R0603	Panasonic	ERJ-3EKF1001V
14	R2 to R6, R8 to R14, R19, R45	Resistor, film, SMD, 0805, 47 k Ω	Yageo-Phycomp	9C08052A4702FKHFT
8	R15 to R18, R23, R30 to R32	Resistor, film, SMD, 0603, 33 Ω	Multicomp	MC 0.063W 0603 1% 33R.
2	R20, R22	Resistor, precision thick film chip, R0805, 10 k Ω	Panasonic	ERJ-6ENF1002V
1	R21	Resistor, precision thick film chip, R0805, 750 Ω	Panasonic	ERJ-6ENF7500V
9	R24 to R27, R29, R33, R37, R39, R42	Resistor, film, SMD, 0603, 0 Ω	Multicomp	MC0603WG00000T5E-TC
2	R34, R35	Resistor, precision thick film chip, R0603, 2.2 k Ω	Panasonic	ERJ-3EKF2201V
1	R36	Resistor, thick film chip, R0603, 2.2 Ω	Panasonic	ERJ-3RQF2R2V
1	R40	Resistor, precision thick film chip, R0805, 100 k Ω	Panasonic	ERJ-6ENF1003V
3	R41, R43, R44	Resistor, precision thick film chip, R0603, 53.6 Ω	Panasonic	ERJ-3EKF53R6V
1	R7	Resistor, precision thick film chip, R0805, 3.01 k Ω	Panasonic	ERJ-6ENF3011V
1	S1	Switch slide SPDT	E-Switch	EG1218
1	S2	Switch tact 6 mm gullwing SMD	Tyco Electronics	FSM6JSMA
1	U1	IC, low noise, LDO micropower regulator, 3.3 V	Linear Technology	LT1761ES5-3.3#PBF
1	U2	IC, linear low noise, LDO micropower regulator, 1.8 V	Linear Technology	LT1761ES5-1.8#PBF
1	U3	IC, CMOS, 192 kHz, digital audio receiver, CS8416-C22	Cirrus Logic	CS8416-CZZ
1	U5	Crystal, SMD, 12.288 MHz	Abracon	ABM3B-12.288MHZ-10-1-U-T
3	U6 to U8	IC, 1-bit translator, FXLP34P5X	Fairchild	FXLP34P5X

Qty	Reference Designator	Description	Supplier	Part No.
NF ¹	C22, C30	Capacitor, ceramic, NP0, R0603	Phycomp (Yageo)	2238 867 15689
NF ¹	R28, R38	Resistor, high frequency, SMD, chip, 0603	Vishay	FC0603E50R0BST1
NF ¹	L5	Inductor, common-mode choke, DLW5BTN251SQ2L	Murata	DLW5BTN251SQ2L
NF ¹	C39 to C41	Capacitor, ceramic, X7R, 0603	AVX	06032C102JAT2A
2	B1, B2	Ferrite bead, low noise	Murata	NFZ2MSM181
4	L1 to L4	Ferrite bead, 500 mA, 600 Ω	Steward	HZ0805E601R-00

¹ NF means not fitted.

¹C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

©2015 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
UG11691-0-9/15(A)



www.analog.com