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ADL5304 Evaluation Board User Guide

FEATURES

4-layer printed circuit board (PCB), 53 mm × 72 mm form factor
Resistor programmable log slope and intercept
Single-or dual-supply operation
Full two argument logarithmic computation
On-board precision 100 nA reference
Optimized for very fast response at all input currents
  Overall bandwidth of >4 MHz for inputs >1 µA
  Bandwidth: 25 kHz at input of 1 nA and 350 kHz at 10 nA
10 decades of input range: 1 pA to 10 mA
Law conformance: ±0.25 dB from 100 pA to 100 µA
Log ratio or fixed-intercept operation
On-board precision 1.5 V and 2.0 V voltage references
Adaptive photodiode (PD) bias for low dark current
Default log slope of 10 mV/dB at VLOG pin

GENERAL DESCRIPTION

This user guide refers to the ADL5304 evaluation board, which allows users to connect the ADL5304 precision log amplifier to current sources with simple SMA connections or, with modification of the default configuration, to mount a photodiode to the INUM input for optical power level applications.

The ADL5304 evaluation board is laid out to minimize errors due to leakage into the sensitive INUM and IDEN nodes through driven guards.

Slope and logarithmic intercept are programmable through on-chip resistors and can be further optimized for specific applications using external resistors. Additional components can be added to optimize filtering for specific applications.

Adaptive photodiode bias is available using the IMON output to optimize photodiode response and dark current.

Full details about the part are available in the ADL5304 data sheet, which should be consulted when using the ADL5304-EVALZ.

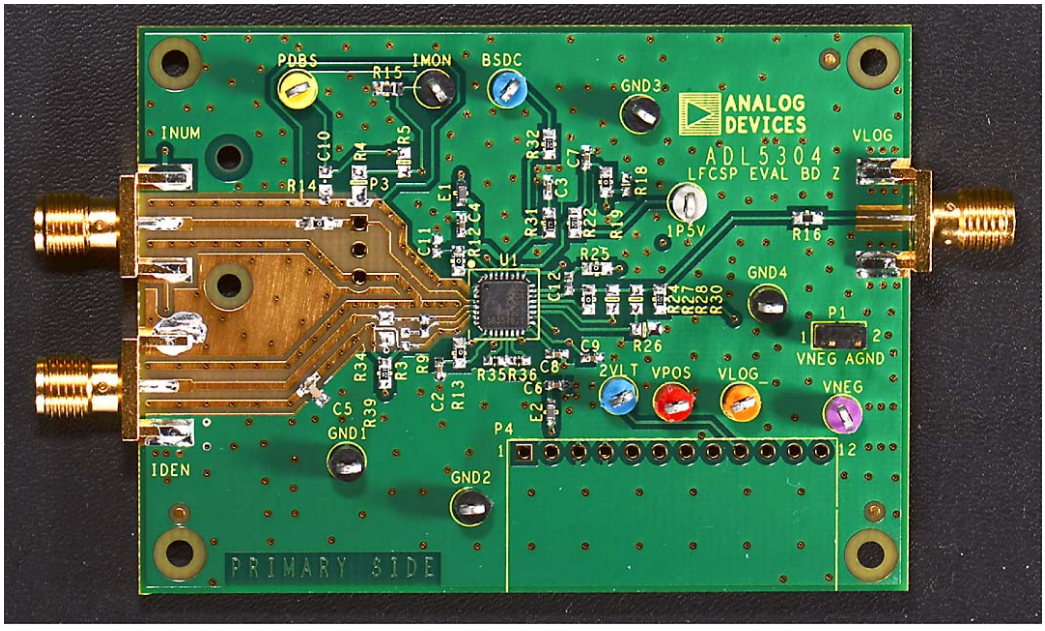

Figure 1. Top View of ADL5304 Evaluation Board

TABLE OF CONTENTS

REVISION HISTORY

11/11—Revision 0: Initial Version

EVALUATION BOARD FEATURES

POWER SUPPLY

The ADL5304 evaluation board can be powered from a single 5 V supply for specified inputs from 1 pA to 3 mA. In single-supply configuration, the VNEG bus is connected to ground using Jumper P1. This is the default configuration of the board. In single-supply operation, the V_{SUM} reference voltage is 1.5 V and the range of the VLOG output swing is 0.5 V to 2.5 V. Ground referenced V_{SUM} operation is not allowed in single-supply configuration. With Jumper P1 removed, the ADL5304 evaluation board can be used in dual-supply mode. In dual-supply mode operation, the VNEG supply is connected to a −2 V to −5 V source. This increases the specified input range from 1 pA to 10 mA. The ADL5304 evaluation board can be configured to operate with V_{SUM} at ground and a V_{LOG} output swing from −1 V to +1 V when VNEG is less than −2 V.

PROGRAMMING SLOPE AND INTERCEPT

The ADL5304 provides precision trimmed internal resistors to allow programming options for slope and intercept without the need for external components. The internal resistors connected to Pin SCL1 to Pin SCL3 are accessed by Resistors R24 to R28. Table 1 shows the values for slope, intercept, and offset available through programming using 0 Ω resistors in the R24 to R28 positions. Additional slope, intercept, and offset values can be configured by using nonzero resistors; however, performance may be affected by drift and tolerance of the external components. The intercept can also be adjusted by using both the INUM and IDEN inputs.

PHOTODIODE CONNECTIONS

The ADL5304 evaluation board has a provision to connect a p-intrinsic-n (PIN) photodiode to the INUM input at Connector P3 (see Table 4). The monitor current output (I_{MON}) provides easy configuration of an adaptive photodiode bias scheme. Input current, I_{NUM}, is multiplied to give an effective output current at the IMON pin of 1.1 × I_{NUM}. Because the photodiode produces I_{NUM}, the additional current must flow in an external resistor, R4, equal to 10 × R_S, where R_S is the value of the internal parasitic series resistance of the photodiode. This ensures that the actual junction of the photodiode is biased as close as possible to 0 V to minimize dark current. Capacitor C10 provides potential filtering and dynamic currents during fast transients. The value for best bias response depends on the photodiode used and should be determined experimentally.

If the adaptive bias is not used, the IMON pin must be connected to ground by populating R5 with a 0 Ω resistor.

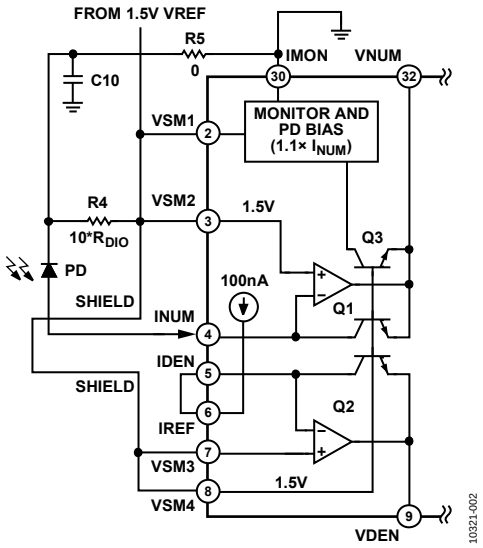

Figure 2. Adaptive Photodiode Bias

1.5 V AND 2.0 V REFERENCES

Accurate 1.5 V (Pin 1P5V) and 2.0 V (Pin 2VLT) reference outputs allow precise repositioning of the intercept using external resistors. These voltages are available on test points and on the P4 connector (see Table 2). The 2.0 V reference can be used in adaptive photodiode mode to set up a precise 0.5 V bias across the photodiode. See the ADL5304 data sheet for more information. The 2.0 V reference can also be used to set a different current reference for the IDEN input by removing R9 and populating R3 and R34. The value of R34 is calculated based on the V_{SUM} voltage, R34 = (2.0 −V_{SUM})/I_{DEN}. For example, with V_{SUM} = 1.5 V to generate an I_{DEN} current of 1 µA, R34 = 500 kΩ.

IREF FIXED CURRENT REFERENCE

The ADL5304 provides a fixed 100 nA reference (I_{REF}), which, in the default configuration, is connected to the IDEN input for single input log calculation. For applications requiring both inputs to the logarithmic argument, IREF can be disconnected from IDEN by removing Resistor R9 and applying current directly to the IDEN input. When IREF is not used, it must be connected to V_{SUM} through Resistor R3 to dump the generated 100 nA current.

SHIELDS AND GUARDS

Reducing errors from external sources in a current sensing circuit requires a different approach from the voltage sensing input of the typical high impedance op amp circuit. Leakage can be a significant source of error for highly sensitive log amps, especially at the low end of their range. For example, a 1 GΩ leakage path to ground from the INUM input with V_{SUM} set to the default 1.5 V generates a 1.5 nA offset. The ADL5304 evaluation board makes extensive use of guards to reduce the effects of leakage at low input levels; however, it is still important to carefully handle and clean the ADL5304 evaluation board to prevent contaminants from handling or leakage currents from improper washing of the PCB. A common mistake for those unfamiliar with low level current sensing is to attach a high impedance scope probe or meter to measure the input for debugging. This can cause significant error, because the typical 1 M ~ 100 MΩ impedance of these probes sources/sinks current from the input depending on their bias.

In instrumentation applications where measurements <1 nA are required, the use of triaxial cables and connectors is common to reduce leakage through the insulating dielectric by carrying a continuous guard from current source to sensing circuit on the intermediate conductor. This type of guarding circuit is different from a conventional electrostatic shield used in voltage sensing applications. An electrostatic shield relies on low impedance and the ability to flow current freely to minimize voltage induced on the shield that can capacitively couple into a high impedance input. A guard is actively driven to the same voltage as the current-carrying center conductor, eliminating leakage through the dielectric between the center conductor and the guard. The guard does not flow current other than the leakage from the guard to the outer shield and is usually only connected to a single end of the cable, because any significant current flow through the guard can couple inductively to the center conductor. Using the ADL5304 evaluation board, the guard can be driven either from the current source (see Figure 5) or from the ADL5304 (see Figure 6).

The ADL5304 evaluation board can bias the shield of a coaxial cable that is connected to the INUM input to the nominal V_{SUM} voltage by removing Resistor R41 and populating Resistor R40, but this requires careful consideration of the environment on the other side of the cable. For example, if the ADL5304 evaluation board is configured for V_{SUM} = 1.5 V, connecting the other end of the INUM coaxial cable to an instrument with a ground referenced shield pulls V_{SUM} to ground and collapses the input stage of the ADL5304. Floating the current source end of the shield provides a low leakage guard, but a separate return path for the signal current must then be provided (see Figure 7). If cable dielectric leakage is not a concern, the INUM input can be connected directly to a coaxial cable with the shield, providing signal ground (see Figure 8).

STRAY MAGNETIC FIELDS

Current input devices such as the ADL5304 are sensitive to their environments in ways that are not typically a problem with high impedance input devices like voltage input op amps, particularly in high bandwidth applications where filtering is not an option. Because of its excellent sensitivity and low noise, the ADL5304 is capable of operation at currents easily influenced by stray magnetic fields. This can lead to unwanted signals coupling into the ADL5304 in unexpected ways. An example of this is shown in Figure 3. In a typical circuit testing environment, eddy currents from instrument power supplies are contained in the steel of the test cart. The low impedance of the cart prevents the eddy currents from generating a sufficient voltage for electrostatic coupling into the typical voltage sensing circuit. In a current sensing application using the ADL5304, the loop currents in the metal cart can inductively couple into the traces and cable used to build the test circuit and into the INUM and IDEN inputs. In this instance, shielding and guarding are ineffective at decoupling the interferer and receiver circuits. The best ways to prevent this type of coupling are careful design to minimize stray magnetic fields, increasing the distance between the interferer and receiver circuits, removing the coupling mechanism, in this example the steel work surface, or using Mu-Metal or similar high magnetic permeability material to provide a magnetic shield.

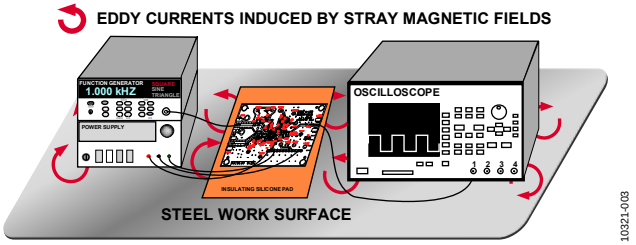

Figure 3. Inductive Coupling of Poorly Shielded Instrument Power Supplies

LOGARITHMIC RATIO OPERATION

Log ratio operation of the ADL5304 is possible using both the INUM and IDEN inputs. For log ratio operation, IREF must be disconnected from IDEN by removing R9.

The value of V_{LOG} depends on the log of the ratio of I_{NUM} and I_{DEN} and the programmed slope (R24/R28), offset by the INPS voltage (R18, R19) according to the following formula:

$$V_{LOG} = V_Y \times \log_{10}\left(\frac{I_{NUM}}{I_{DEN}}\right) + V_{OFS}$$

where:
V_Y denotes slope.
V_{OFS} denotes the voltage offset applied at the INPS pin (1.5 V in the default configuration).

Because the ratio of I_{NUM}/I_{DEN} can be either greater or less than unity, V_{LOG} can be of either polarity, requiring a negative supply in some cases. For example, if the ratio varies from 1:1000 to 1000:1 and a slope of 20 mV/dB is required, the peak swing is ±1.2 V around V_{OFS}.

Option 5 in Table 1 provides this with an intercept, I_Z, of 17.8 pA (V_{OFS} = 1.5 V) with V_{LOG} = ±1.2 V around V_{OFS} = 1.5 V, which results in 0.3 V ≤ V_{LOG} ≤ 2.7 V.

The electrical characteristics of I_{NUM} and I_{DEN} are identical, with the exception of the I_{MON} current, which is derived from the I_{NUM} signal and allows adaptive photodiode bias at the INUM input only.

VOLTAGE SOURCE OPERATION

In test situations where a precision current source is not available or a dynamic signal is required, a voltage source or function generator can be used to supply I_{NUM} current through a resistor in series with the INUM input. In the default configuration, R14 is a 0 Ω, 0603 resistor. Due to the large input range of the ADL5304, it is very difficult to find a voltage source with sufficient range to fully exercise the ADL5304. This limitation can be mitigated by using different resistor values to access different segments of the ADL5304's range.

The INUM and IDEN inputs cannot source current. When using a voltage source and series resistor to provide INUM or IDEN current, the source voltage must always be positive relative to the V_{SUM} voltage. If the voltage source drops below V_{SUM}, the translinear device that performs the logarithmic function saturates and the feedback amplifier rails as it attempts to balance the loop around the translinear device. This will not damage the ADL5304, but the recovery time of the input is directly related to the input current and the capacitance seen by the input. At low input currents, the input can take significantly longer to recover from momentary transients that attempt to source current.

SPEED AND FILTERING

Filtering to Improve Noise and Dynamic Behavior

The noise at the output of a log amp, particularly at low current levels, leads to uncertainty in the measurement. Noise amplitude is limited by the finite bandwidth. If measurement speed is not of primary concern, additional filtering can reduce noise. Figure 4 shows the locations provided on the ADL5304 evaluation board for additional external filtering.

Typically, capacitors are not used on the numerator side (I_{NUM}) to keep the speed of the device as high as possible. On the denominator side (I_{DEN}), additional filtering is useful to reduce noise. In applications where I_{NUM} is used as the reference to the logarithmic equation and I_{DEN} is a variable, for example, where a reverse logarithmic slope is desired, filtering can be performed on the numerator side (I_{NUM}).

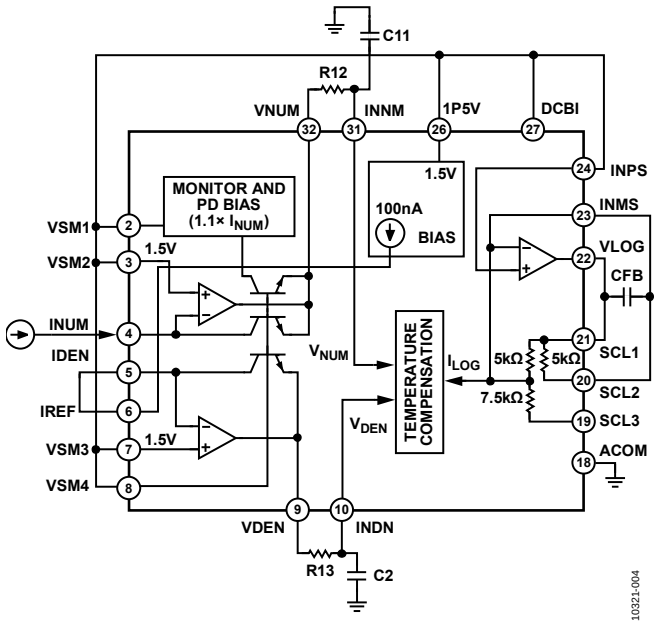

Figure 4. Evaluation Board Filtering Locations

A capacitor placed on the INUM and IDEN inputs effectively reduces the bandwidth of the input stages. A few picofarads of capacitance (<5 pF) reduce the bandwidth significantly for currents below approximately 1 µA, and 1 nF to 10 nF are normally enough to reduce the bandwidth up to the maximum 10 mA of input current. When measurement speed is of primary importance, it is better to add filtering after the FET amp outputs, in which case, C2 and R13 for the INDN inputs and C11 and R12 for the INNM inputs are the best locations. A bias current of approximately 35 µA flows from the INNM and INDN pins through Resistors R12 and R13, raising the voltage at the INNM and INDN pins. To prevent this voltage rise from limiting headroom in the temperature compensation block, the value of R12 and R13 should not be much larger than 1 kΩ.

Adding a capacitor, C12, adds additional filtering at the buffer output. This capacitor also helps to optimize the pulse response by placing a zero across the feedback resistor (2.5 kΩ in the default configuration). A good value to start with is 22 pF; this introduces a zero at 2.9 MHz that can improve the pulse response for input currents greater than 100 µA.

GUARD CONFIGURATIONS

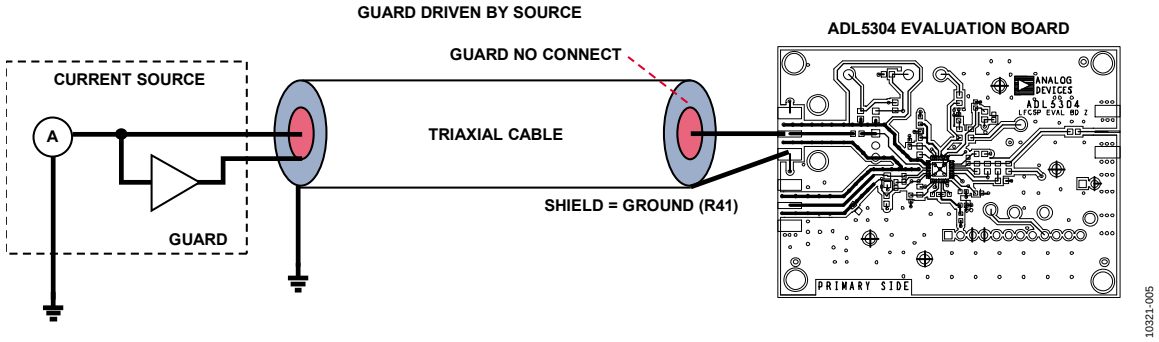

Figure 5. ADL5304 INUM Configuration, Triaxial Cable, Guard from Current Source

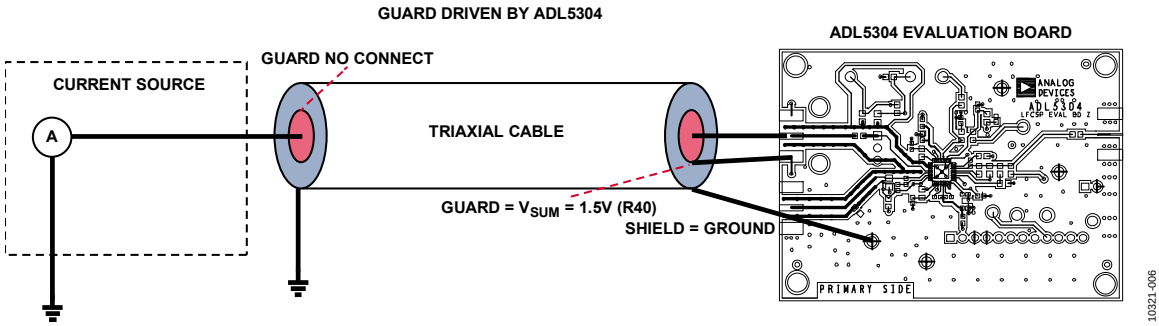

Figure 6. ADL5304 INUM Configuration, Triaxial Cable, Guard from ADL5304

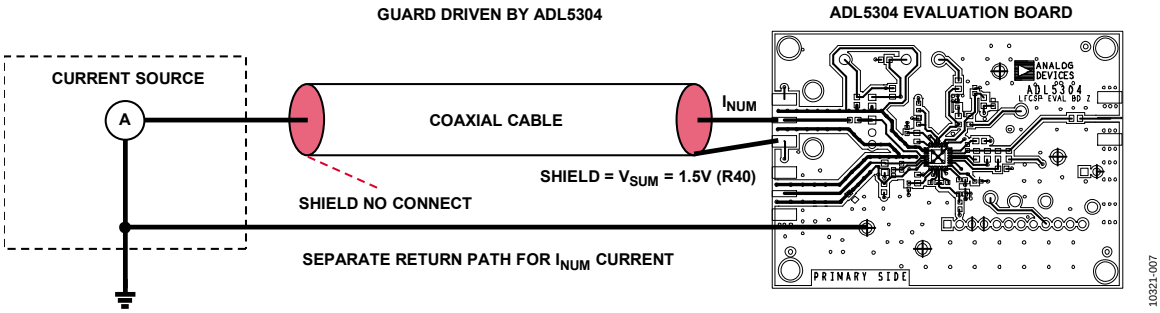

Figure 7. ADL5304 INUM Configuration, Coaxial Cable, Guard = V_{SUM}

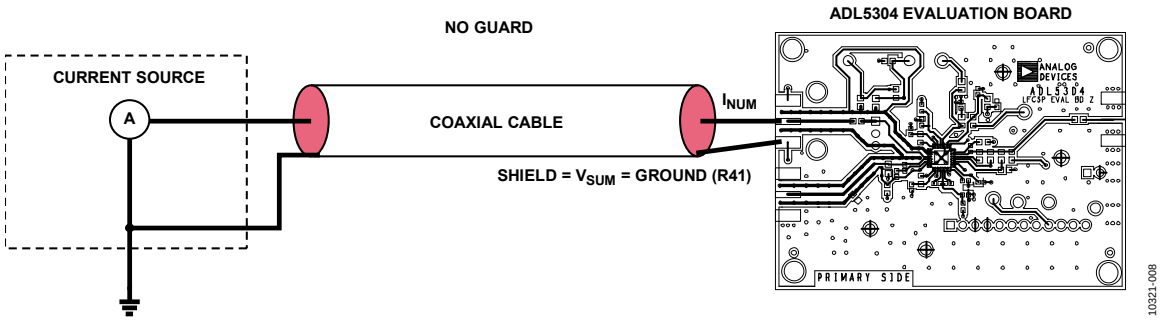

Figure 8. ADL5304 INUM Configuration, Coaxial Cable, No Guard

SLOPE/INTERCEPT OPTIONS

Table 1. VLOG Scaling Options

Option	Pin SCL1	Pin SCL2	Pin SCL3	Pin INPS	Pin INMS	V_Y (V/dec)	I_Z (A)	V_{OFS} (V)
Single-Supply Operation (VNEG = 0 V; VSMx = DCBI = INPS = 1P5V)								
1[1]	R24	R25	Open	R19	R25	0.2	3.16 f	1.5
2	R24	R25	R28	R19	R25	0.15	0.01 f	1.5
3	R24	R25	R26	R19	R25	0.2	0.01 f	2.0
4	R24	Open	R26	R19	Open	0.4	56.2 f	2.5
5	R24	Open	Open	R19	Open	0.4	17.8 p	1.5
6	Open	Open	R28	R19	Open	0.6	316 p	1.5
7	Open	R27	Open	R19	Open	0.8	1.33 n	1.5
8	R24	R25	2VLT	R19	R25	0.2	21.6 f	1.333
Dual-Supply Operation (VNEG < −2 V; VSMx = DCBI = INPS = Ground)								
9[2]	R24	R25	Open	R18	R25	0.2	100 n	0
10	R24	R25	R28	R18	R25	0.15	100 n	0
11	R24	Open	Open	R18	Open	0.4	100 n	0
12	Open	Open	R28	R18	Open	0.6	100 n	0
13	Open	R27	Open	R18	Open	0.8	100 n	0

[1] Default setup for single-supply operation and VSMx = 1.5 V.
[2] Default setup for dual-supply operation and VSMx = ground.

EXTERNAL CONNECTORS

ANALOG I/O CONNECTOR, P4

The analog I/O connector, P4, provides external connections for power supplies, references, and outputs. The pinout of the connector is shown in Table 2.

Table 2. Pin Functions for Analog I/O Connector, P4

Pin Number	Pin Function
P4-1	VPOS
P4-2	VPOS
P4-3	AGND
P4-4	AGND
P4-5	1P5V
P4-6	VLOG
P4-7	VSUM
P4-8	BSDC
P4-9	2VLT
P4-10	VNEG
P4-11	VNEG
P4-12	NC

INUM, IDEN, AND VLOG SMA CONNECTORS

INUM, IDEN, and VLOG are connected through standard SMA end launch connectors. The outer shell of the INUM connector can be connected to ground (R41) or the VSUM bus (R40) when the ADL5304 provides the guard for low leakage applications. IDEN and VLOG connector outer shells are permanently connected to ground.

OUTPUT LOADING

The ADL5304 is specified into a >2 kΩ load. To maintain stability of the VLOG output when presented with a capacitive load, a 453 Ω resistor, R16, is placed in series with the VLOG output to isolate the ADL5304 from the loading effects of long cables and instrumentation. R16 can be replaced with a 0 Ω resistor if the output load is known to be greater than 2 kΩ and not significantly reactive.

SINGLE-/DUAL-SUPPLY JUMPER, P1

This jumper connects the VNEG rail to ground to facilitate single-supply operation. Remove the jumper on P1 to configure for dual-supply operation.

Table 3. Test Points

Color	Function
Black	AGND ground
Violet	VNEG negative supply
Orange	VLOG output
Red	VPOS positive supply
Blue	BSCD bias generator filter
Yellow	PDBS photodiode bias
Black	IMON photodiode monitor output
Blue	2VLT
Grey	1P5V

Table 4. Photodiode Connector, P3

Pin Number	Pin Function
P3-1	Cathode
P3-2	Anode
P3-3	Case

EVALUATION BOARD SCHEMATICS AND ARTWORK

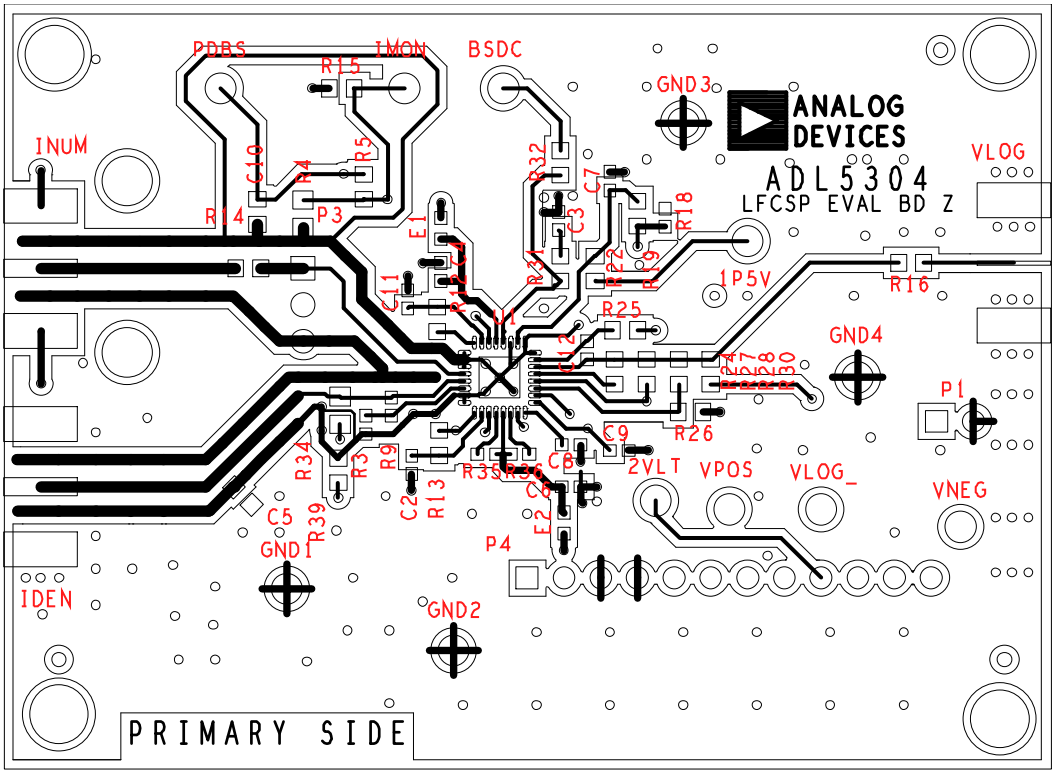

Figure 9. ADL5304-EVALZ, 32-Lead LFCSP Evaluation Board Artwork, Primary Side

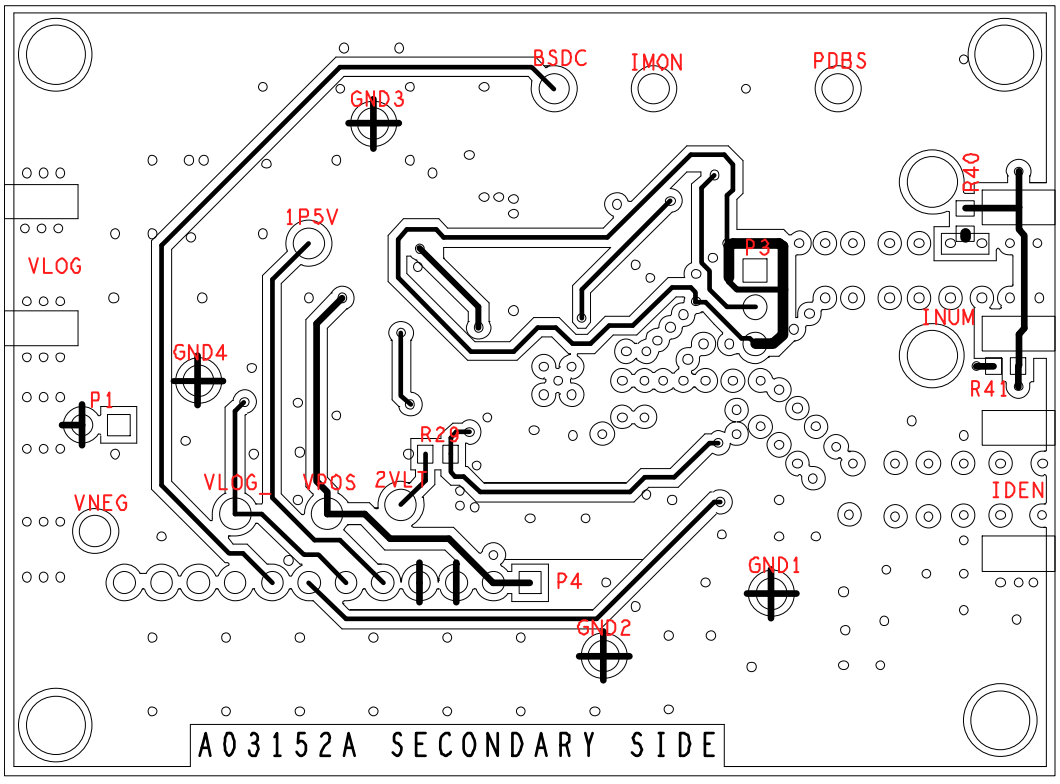

Figure 10. ADL5304-EVALZ, 32-Lead LFCSP Evaluation Board Artwork, Secondary Side

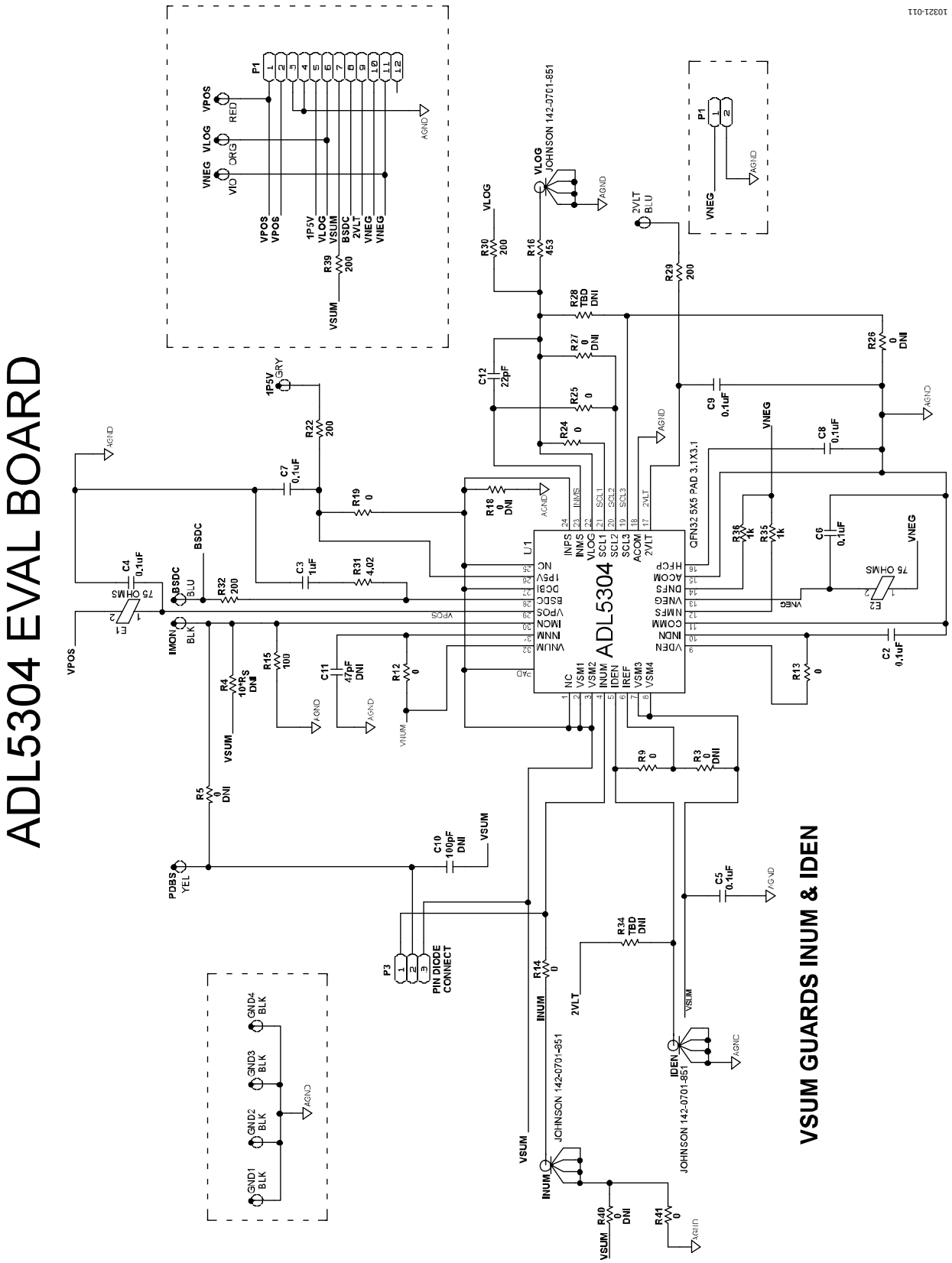

Figure 11. ADL5304-EVALZ, 32-Lead LFCSP Evaluation Board Schematic

EVALUATION BOARD OPTIONAL COMPONENTS

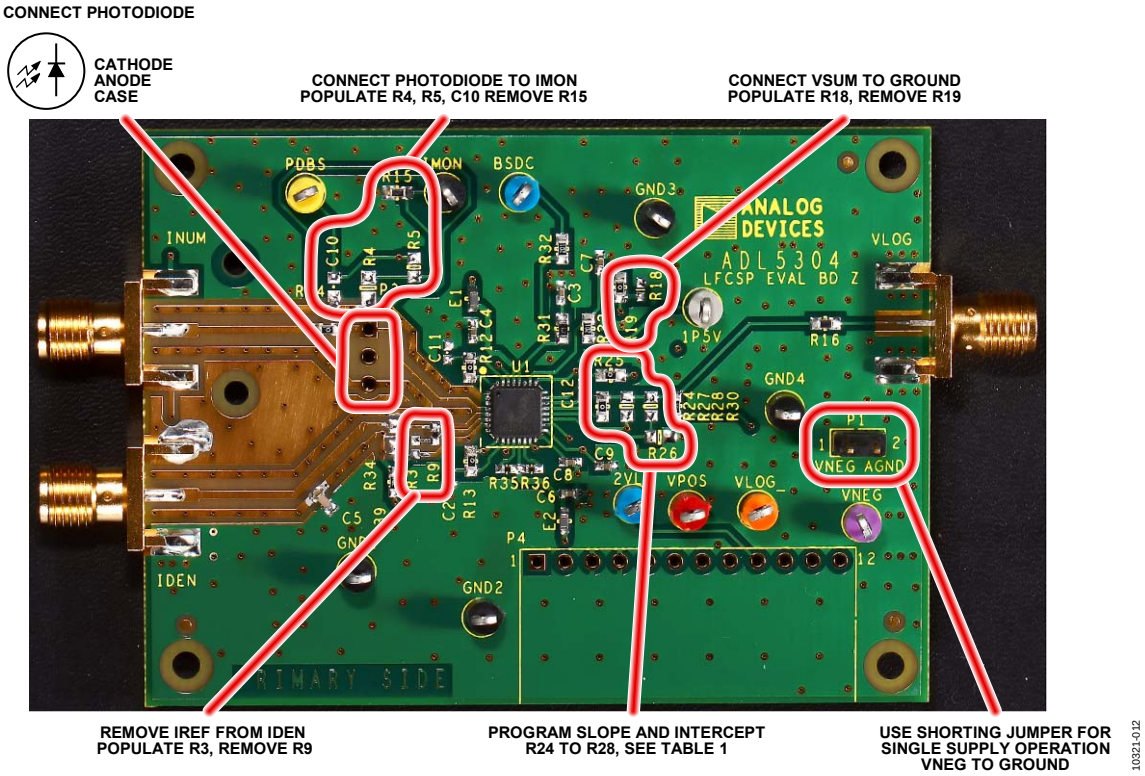

Figure 12. ADL5304-EVALZ, 32-Lead LFCSP Evaluation Board Top Optional Configurations

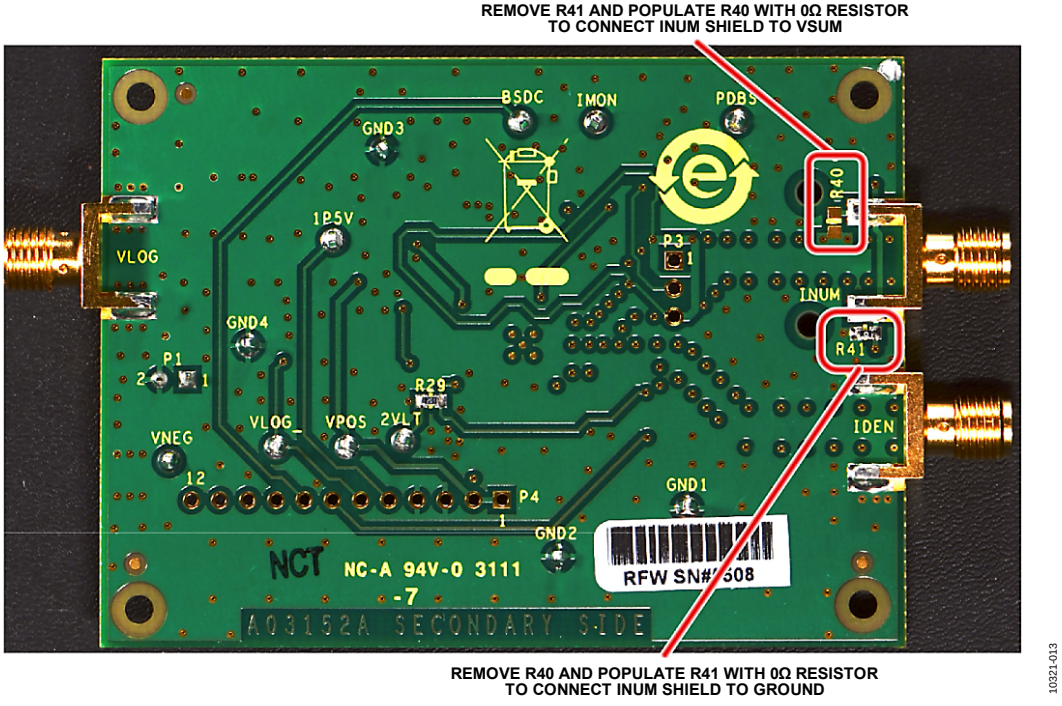

Figure 13. ADL5304-EVALZ, 32-Lead LFCSP Evaluation Board Bottom Optional Configurations

ORDERING INFORMATION

BILL OF MATERIALS

Table 5.

Reference Designator	Value	Part Description	Manufacturer	Part No.
C12	22 pF, 5%	Capacitor ceramic 0402	Phycomp (Yageo)	0402CG220J9B200
C2, C4, C6 to C9	0.1 µF, 10%	Capacitor ceramic X7R 0402	Murata	GRM155R71C104KA88D
C5	0.1 µF, 10%	Capacitor ceramic X7R 0603 50V	AVX	06035C104KAT2A
C3	1 µF, 10%	Capacitor ceramic mono 0402	Murata	GRM155R60J105KE19D
IDEN, INUM, VLOG		CONN PCB coaxial SMA end launch	Johnson	142-0701-851
E1, E2	75 Ω, 25%	Ferrite BEAD 0603	Murata	BLM18BA750SN1D
R9	0 Ω, 5%	Resistor film SMD 0402 1/16 W	Panasonic	ERJ-2GE0R00X
R12 to R14, R19, R24, R25, R41	0 Ω, 5%	Resistor film SMD 0603 1/10 W	Panasonic	ERJ-3GEY0R00V
R22, R29, R30, R32, R39	200 Ω, 0.1%	Resistor film SMD 0603 1/10 W	Panasonic	ERA-3YEB201V
R31	4.02 Ω, 1%	Resistor chip 0603 1/10 W	Yageo Phycomp	RC0603FR-074R02L
R15	100 Ω, 1%	Resistor film chip R0603 1/10 W	Panasonic	ERJ-3EKF1000V
R16	453 Ω, 1%	Resistor film chip 0603 75 V 1/10 W	Vishay	CRCW0603453RFKEA
R35, R36	1 kΩ, 0.1%	Resistor metal film 1/16 W	SUSUMU	RG1005P-102-B-T5
1P5V		Grey test point	Components Corporation	TP104-01-08
2VLT, BSDC		Blue test point	Components Corporation	TP104-01-06
GND1 to GND4, IMON		Black test point	Components Corporation	TP-104-01-00
PDBS		Yellow test point	Components Corporation	TP-104-01-04
VLOG		Orange test point	Components Corporation	TP-105-40-03
VNEG		Violet test point	Components Corporation	TP104-01-07
VPOS		Red test point	Components Corporation	TP-104-01-02
P1		CONN CNBERG69157-102	Tyco Electronics	826936-2
C11[1]	47 pF, 5%	Capacitor ceramic C0G 0402 50 V	Murata	GCM1555C1H470JZ13D
C10[1]	100 pF, 5%	Capacitor ceramic NP0 0603 50 V	PHYCOMP (YAGEO)	2238 867 15101
P3[1]		CONN-PCB BERG HDR ST male 3P	Samtec	TSW-103-08-G-S
P4[1]		CONN-PCB HDR 12P R/A	Molex	22-12-2124
R28[1]	TBD[2]	Resistor film chip 0603 1/10 W	TBD	TBD
R3, R18[1]	0 Ω, 5%	Resistor film SMD 0402 1/16 W	Panasonic	ERJ-2GE0R00X
R5, R26, R27, R40[1]	0 Ω, 5%	Resistor film SMD 0603 1/10 W	Panasonic	ERJ-3GEY0R00V
R34[1]	TBD[2]	Resistor film chip 0805 1/8 W	TBD	TBD
R4[1]	10 × R_S	Resistor film chip 0805 1/8 W	Panasonic	N/A

[1] Not populated on standard evaluation board.
[2] To be determined by the user.

RELATED LINKS

Resource	Description
ADL5304ACPZ	Product Page, High Speed, 200 dB Range, Logarithmic Converter
ADL5304-EVALZ	ADL5304 Evaluation Board

NOTES

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ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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