

Programming the AD5932 for Frequency Sweep and Single Frequency Outputs

by Liam Riordan

INTRODUCTION

This application note details how to program the output of the [AD5932](#) to sweep frequency from 1 MHz to 10 MHz. Then, when the user has discovered the strongest frequency point on the spectrum, the part can be selected to only transmit a sine wave at that particular frequency.

POWERING UP THE AD5932

The AD5932 is powered up in an undefined state. The registers (control and frequency) contain invalid data and must be set to a known value by the user. The control register should be the first register to be programmed because this sets up the part. Note that a write to the control register automatically resets the internal state machines and provides an analog output of midscale

because it performs the same function as the INTERRUPT pin. Typically, this is followed by a serial loading of all the required scan parameters. The DAC output remains at midscale until a frequency scan is started using the CTRL pin.

To set up the part in sweep mode, the following registers must be written to:

- Control register $\times 1$
- Start frequency registers (F_{START}) $\times 2$
- Frequency increment (or delta frequency) register (Δf) $\times 1$
- Number of increments register (N_{INCR}) $\times 1$

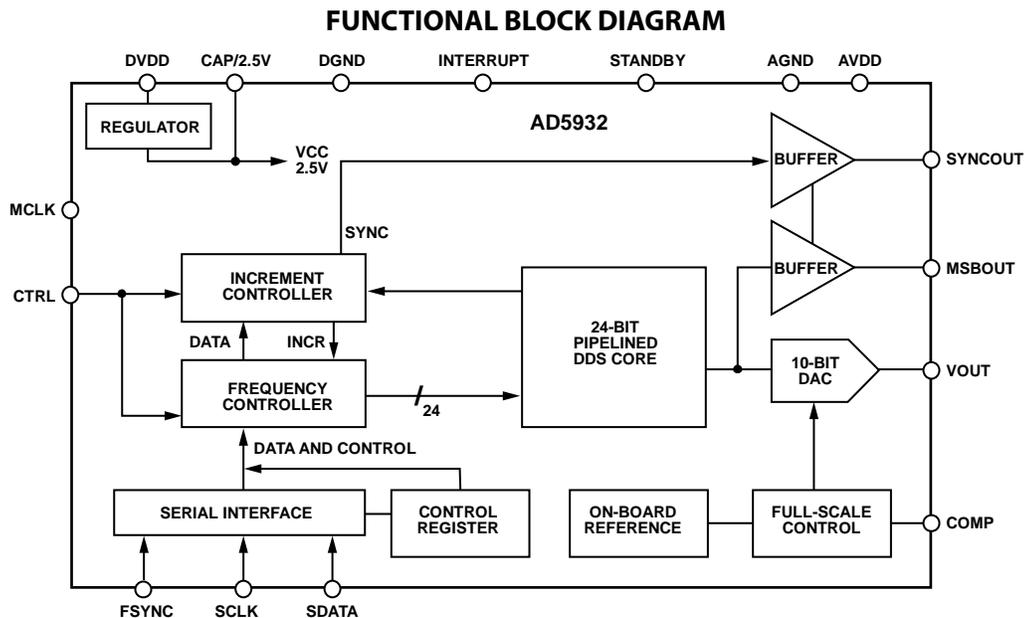


Figure 1.

08425-0101

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REVISION HISTORY

11/10—Rev. 0 to Rev. A

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| Changes to Table 1, Start Frequency Section, and Frequency Increment Section..... | 3 |
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8/09—Revision 0: Initial Version

PROGRAMMING THE AD5932 IN SWEEP MODE

Control Register

The first register to write to after powering up the AD5932 is the 16-bit control register.

Writing the following code (Frame I) to the control register sets the part to sweep mode (see Table 1):

0000 1111 1111 1111

Table 1. Description of Bits in the Control Register

| Bit | Value | Function |
|------------|-------|---|
| D15 to D12 | 0 | Address bits |
| D11 | 1 | F _{START} becomes a two-write operation, both MSB and LSB loaded |
| D10 | 1 | DAC enabled |
| D9 | 1 | Sine wave selected |
| D8 | 1 | MSBOUT pin enabled |
| D7 | 1 | Reserved |
| D6 | 1 | Reserved |
| D5 | 1 | Increments triggered externally through CTRL pin |
| D4 | 1 | Reserved |
| D3 | 1 | SYNCOUT pin toggles at the end of a sweep |
| D2 | 1 | SYNCOUT pin toggles at the end of a sweep |
| D1 | 1 | Reserved |
| D0 | 1 | Reserved |

Start Frequency

The next two bytes in the sequence are the F_{START} registers, both MSB and LSB (see Table 2).

Table 2. F_{START} Registers

| D15 | D14 | D13 | D12 | D11 to D0 |
|-----|-----|-----|-----|---------------------------------------|
| 1 | 1 | 0 | 0 | 12 LSBs of F _{START} [11:0] |
| 1 | 1 | 0 | 1 | 12 MSBs of F _{START} [23:12] |

To generate a 1 MHz start frequency, the following equation defines the code to be loaded:

$$M = \frac{f_{OUT} \times 2^n}{f_{MCLK}}$$

where:

f_{OUT} = 1 MHz, the output frequency of AD5932.

f_{MCLK} = 50 MHz, the MCLK frequency.

n = 24 bits, the resolution of the on-chip accumulator.

$$M = \frac{f_{OUT} \times 2^n}{f_{MCLK}} = 335,544 = 0x51EB8$$

This hexadecimal value must be separated into the F_{START} MSB and F_{START} LSB.

0x51EB8 = 0101 0001 1110 1011 1000

Therefore, for the F_{START} LSB, the following data (Frame II) is loaded:

1100 1110 1011 1000

For the F_{START} MSB, the following code (Frame III) is loaded:

1101 0000 0101 0001

Frequency Increment

The Δf register is a 23-bit register that requires two 16-bit writes to be programmed. The direction of the increment is determined by the address bits (see Table 3).

Table 3. Δf Register Bits

| D15 | D14 | D13 | D12 | D11 | D10 to D0 | Scan Direction |
|-----|-----|-----|-----|-----|-----------------------|---------------------------------------|
| 0 | 0 | 1 | 0 | | 12 LSBs of Δf [11:0] | N/A |
| 0 | 0 | 1 | 1 | 0 | 11 MSBs of Δf [22:12] | Positive Δf (F _{START} + Δf) |
| 0 | 0 | 1 | 1 | 1 | 11 MSBs of Δf [22:12] | Negative Δf (F _{START} - Δf) |

For an increment of 0.1 MHz, the same method is used to calculate the increment size.

$$M = \frac{f_{OUT} \times 2^n}{f_{MCLK}}$$

where:

f_{OUT} = 0.1 MHz.

M = 0x8312.

Therefore, for an increasing increment sweep, the LSB (Frame IV) of the Δf register is

0010 0011 0001 0010

The MSB (Frame V) of the Δf register is

00110 000 0000 1000

Number of Increments (N_{INCR})

The end frequency is calculated by multiplying the frequency increment value (Δf) by the number of frequency increments, N_{INCR} . This is a 12-bit data register with four address bits, as shown in Table 4, where the maximum number of increments is 4095.

Table 4. N_{INCR} Data Bits

| D11 to D0 | Number of Increments |
|----------------|---|
| 0000 0000 0010 | Two frequency increments. This is the minimum number of frequency increments. |
| 0000 0000 0011 | Three frequency increments. |
| 0000 0000 0100 | Four frequency increments. |
| ... | ... |
| 1111 1111 1110 | 4094 frequency increments. |
| 1111 1111 1111 | 4095 frequency increments. |

To calculate the stop frequency, use the following equation:

$$f_{STOP} = F_{START} + N_{INCR} \times \Delta f$$

To obtain a stop frequency of 10 MHz with an F_{START} of 1 MHz and a Δf of 0.1 MHz, 90 increments are needed.

90 decimal = 5A = 0101 1010

Therefore, for the N_{INCR} register, load the following data (Frame VI):

0001 0000 0101 1010

Increment Interval

This is the last register that can be loaded. However, in the control register, the external increment control is selected; therefore, this register does not need to be written to. Refer to the [AD5932](#) data sheet for further details.

In the auto-increment mode, a single pulse at the CTRL pin starts and executes the frequency scan. In the external increment mode, the CTRL pin also starts the scan, but the frequency increment interval is determined by the time interval between sequential low-to-high transitions on the CTRL pin.

PROGRAMMING THE AD5932 FOR SINGLE FREQUENCY OUTPUT

Once the sweep is complete and the user measures the optimum frequency tone, for example, 2.5 MHz, it is possible to select this frequency value and transmit continuously. Load 2.5 MHz to the F_{START} register and then load to output by driving the CTRL pin high. Make no further low-to-high transitions on the CTRL pin so that the optimum frequency is available on the AD5932 VOUT pin continuously.