REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	PREPARED BY Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil/
Original date of drawing YY MM DD 16-11-01	CHECKED BY Phu H. Nguyen	TITLE MICROCIRCUIT, LINEAR-DIGITAL, WIDEBAND, 40 dB ISOLATION AT 1 GHz, CMOS 1.65 V TO 2.75 V, SPST SWITCH, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A | CODE IDENT. NO. 16236	DWG NO. V62/16613
	REV	PAGE 1 OF 12

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Wideband, 40 dB Isolation at 1 GHz, CMOS 1.65 V to 2.75 V, SPST Switch microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/16613	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADG901–EP	Wideband, 40 dB Isolation at 1 GHz, CMOS 1.65 V to 2.75 V, SPST Switch

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	JEDEC MO-229-WEED-4	Lead Frame Chip Scale Package [LFCSP]

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to GND	-0.5 V to +4.0 V 2/
Inputs to GND	-0.5 V- to V_{DD} + 0.3 V 2/ 3/
Continuous Current	Data + 15% 4/
Input Power	18 dBm 5/
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature	150°C
Lead temperature (Soldering, 10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C
ESD	1 kV

1.4 Thermal characteristics.

Thermal resistance

Case outline	θ_{JA}	θ_{JC}	Unit
Case X	48	1	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Tested at 125°C.
3/ When RF1 and RF2 are in the open position, the input to ground rating is −0.5 V to V_{DD} − 0.5 V.
4/ See Table I. – Continuous Current Per Channel.
5/ The switch is tested in both the open and closed positions. In the closed condition, power is applied to RF1, and RF2 is terminated to a 50 Ω resistor to GND. In the open condition, power is applied to RF1 and RF2.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum operating conditions and electrical performance characteristics are as specified in 1.3, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Truth table. The truth table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 Insertion Loss. The Insertion Loss shall be as shown in figure 6.

3.5.7 Switching Timing: t_{ON}, t_{OFF}. The Switching Timing: t_{ON}, t_{OFF} shall be as shown in figure 7.

3.5.8 Switching Timing: t_{RISE}, t_{FALL}. The Switching Timing: t_{RISE}, t_{FALL} shall be as shown in figure 8.

3.5.9 IP3. The IP3 shall be as shown in figure 9.

3.5.10 Video Feedthrough. The Video Feedthrough shall be as shown in figure 10.

3.5.11 OFF Isolation. The OFF Isolation shall be as shown in figure 11.

3.5.12 P1 dB. The P1 dB shall be as shown in figure12.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits Min	Limits Typ 3/	Limits Max	Unit
AC Electrical Characteristics						
−3 dB Frequency 4/				4.5		GHz
Insertion Loss	S_{21}, S_{12}	DC to 100 MHz; V_{DD} = 2.5 V ± 10%, See Figure 6		0.4	0.7	dB
		500 MHz; V_{DD} = 2.5 V ± 10%		0.6	1	
		1000 MHz; V_{DD} = 2.5 V ± 10%		0.8	1.25	
Isolation—RF1 to RF2	S_{21}, S_{12}	100 MHz	55	61		dB
		500 MHz	40	45		
		1000 MHz	31	38		
Return Loss (On Channel) 4/	S_{11}, S_{22}	DC to 100 MHz	18	28		dB
		500 MHz		25		
		1000 MHz		20		
Return Loss (Off Channel) 4/	S_{11}, S_{22}	DC to 100 MHz	15	23		dB
		500 MHz		21		
		1000 MHz		19		
On Switching Time 4/	t_{ON}	50% CTRL to 90% RF, see Figure 7		4	6.5	ns
Off Switching Time 4/	t_{OFF}	50% CTRL to 10% RF, see Figure 7		6.5	10.5	ns
Rise Time 4/	t_{RISE}	10% to 90% RF, see Figure 8		3.1	5.5	ns
Fall Time 4/	t_{FALL}	90% to 10% RF, see Figure 8		6.0	9.5	ns
Third-Order Intermodulation Intercept		900 MHz/901 MHz, 4 dBm, see Figure 9	28.5	36		dBm
Video Feedthrough 5/		See Figure 10		2.5		mVp-p
Input Power						
1 dB Input Compression 6/	P1dB	1000 MHz; see Figure 12		17		dBm
DC Electrical Characteristics						
Input High Voltage	V_{INH}	V_{DD} = 2.25 V to 2.75 V	1.7			V
	V_{INH}	V_{DD} = 1.65 V to 1.95 V	0.65 V_{DD}			V
Input Low Voltage	V_{INL}	V_{DD} = 2.25 V to 2.75 V			0.7	V
	V_{INL}	V_{DD} = 1.65 V to 1.95 V			0.35 V_{DD}	V
Input Leakage Current	I_I	0 ≤ V_{IN} ≤ 2.75 V		±0.1	±1	µA
Capacitance 4/						
RF1/RF2, RF Port On Capacitance	$C_{RF\ on}$	f = 1 MHz		1.2		pF
CTRL Input Capacitance	C_{CTRL}	f = 1 MHz		2.1		pF

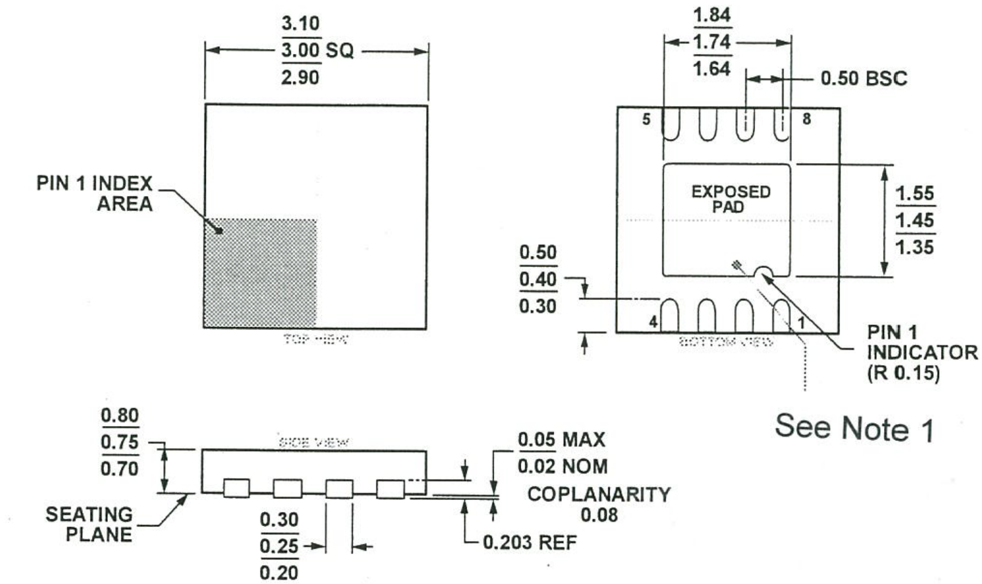
See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test		Symbol	Test conditions 2/	Limits Min	Typ 3/	Max	Unit
Power Requirements							
V_{DD}				1.65		2.75	V
Quiescent Power Supply Current		I_{DD}	Digital inputs = 0 V or V_{DD}		0.1	2.5	µA
Continuous Current Per Channel 4/							
V_{DD} = 2.75 V, V_{SS} = 0 V	T_A = 25°C		8-lead LFCSP, θ_{JA} = 48°C/W, dc bias = 0.5 V			70	mA
	T_A = 85°C					7	
	T_A = 105°C					3.85	
	T_A = 125°C					2.8	
V_{DD} = 1.65 V, V_{SS} = 0 V	T_A = 25°C		8-lead LFCSP, θ_{JA} = 48°C/W, dc bias = 0.5 V			56	mA
	T_A = 85°C					7	
	T_A = 105°C					3.85	
	T_A = 125°C					2.8	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ V_{DD} = 1.65 V to 2.75 V, GND = 0 V, input power = 0 dBm, temperature range = −55°C to +125°C, unless otherwise noted.
3/ Typical values are at V_{DD} = 2.5 V and 25°C, unless otherwise specified
4/ Guaranteed by design, not subject to production test.
5/ Video feedthrough is the dc transience at the output of any port of the switch when the control voltage is switched from high to low or low to high in a 50 Ω test setup, measured with 1 ns rise time pulses and 500 MHz bandwidth.
6/ For less than 100 MHz, refer to the AN-952 Application Note from manufacturer data for more information about power handling.

Case X



NOTES:

1. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section from the manufacturer data sheet.
2. The Lead Frame Chip Scale Package [LFCSP] has an exposed PAD. The exposed PAD must be tied to the substrate, GND.
3. All linear dimensions are in millimeters.
4. Falls within JEDEC MO-229-WEED-4.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{DD}	8	RF2
2	CTRL	7	GND
3	GND	6	GND
4	RF1	5	GND

FIGURE 2. Terminal connections.

Terminal number	Terminal symbol	**Description**
1	V_{DD}	Power Supply Input. These devices can be operated from 1.65 V to 2.75 V; decouple V_{DD} to GND.
2	CTRL	CMOS or LVTTL Logic Level. CTRL input must not exceed V_{DD}. Logic 0: RF1 isolated from RF2. Logic 1: RF1 to RF2.
3, 5, 6, 7	GND	Ground Reference Point for All Circuitry on the Device.
4	RF1	RF1 Port.
8	RF2	RF2 Port.
	EPAD	Exposed Pad. The LFCSP package has an exposed pad. The exposed pad must be tied to the substrate, GND.

FIGURE 3. Terminal function.

CTRL	**Signal Path**
0	RF1 isolated from RF2
1	RF1 to RF2

FIGURE 4. Truth table.

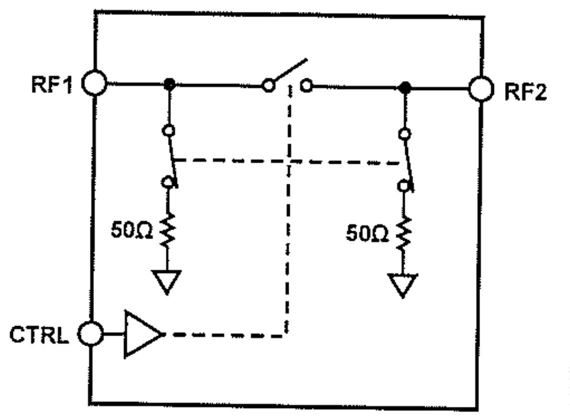


FIGURE 5. Functional block diagram.

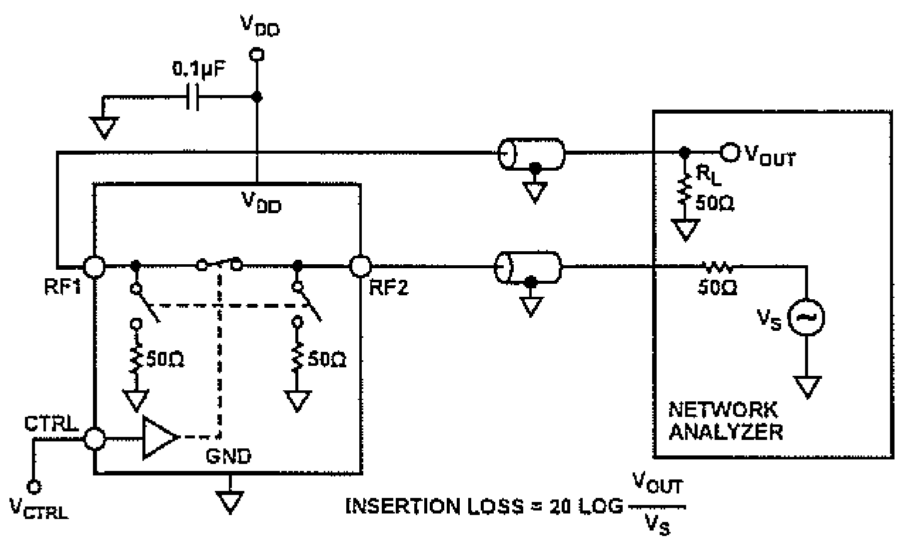


FIGURE 6. Insertion Loss.

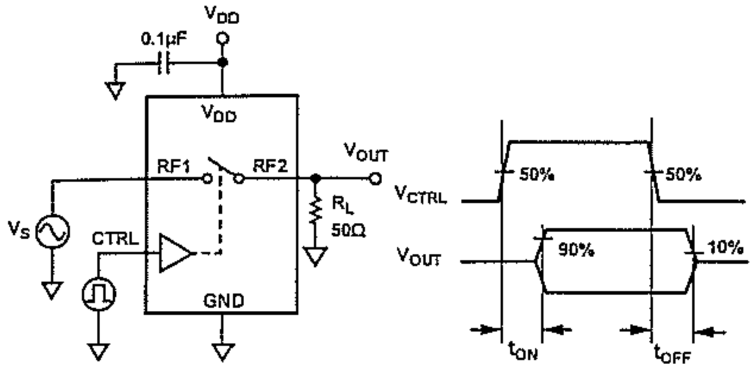


FIGURE 7. Switching Timing: t_{ON}, t_{OFF}.

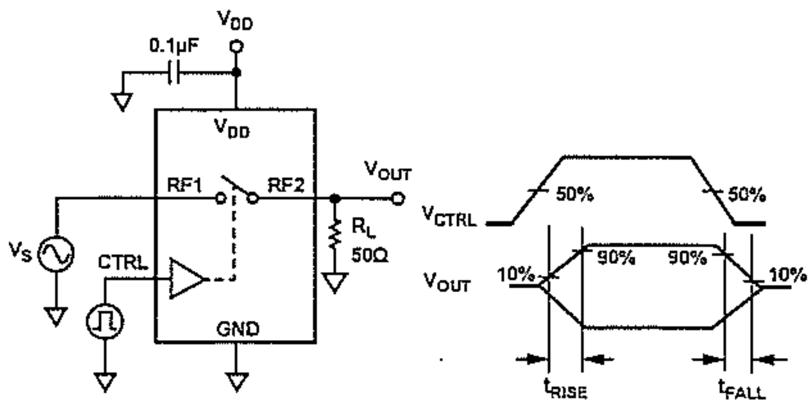


FIGURE 8. Switching Timing: t_{RISE}, t_{FALL}.

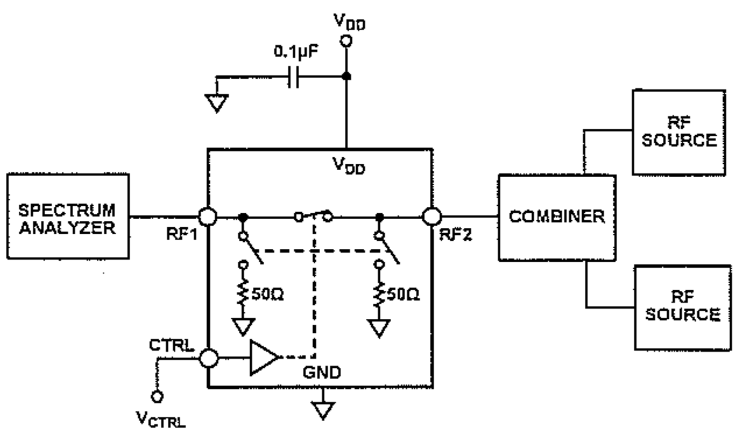


FIGURE 9. IP3.

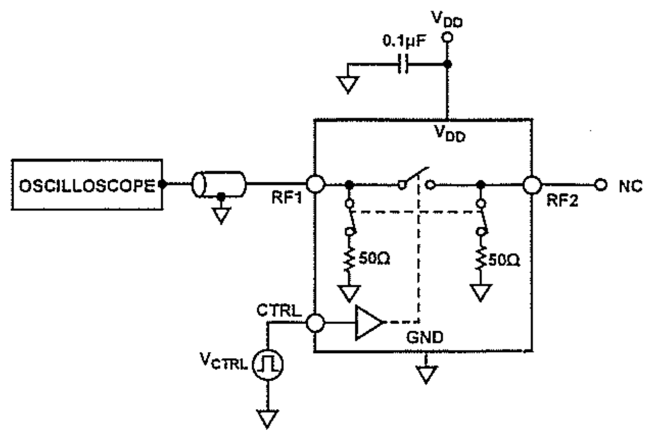


FIGURE 10. Video Feedthrough.

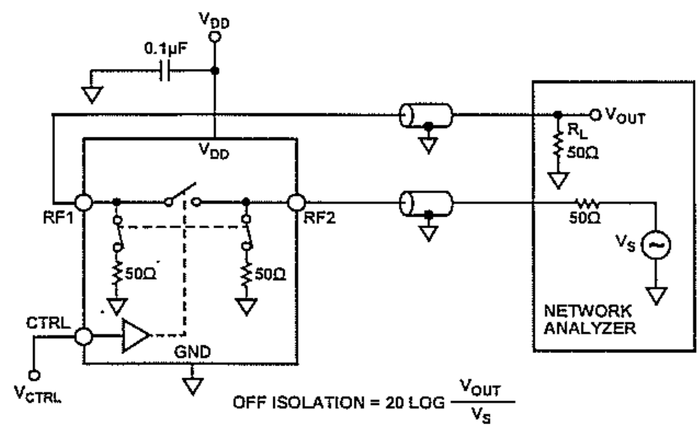


FIGURE 11. Off Isolation.

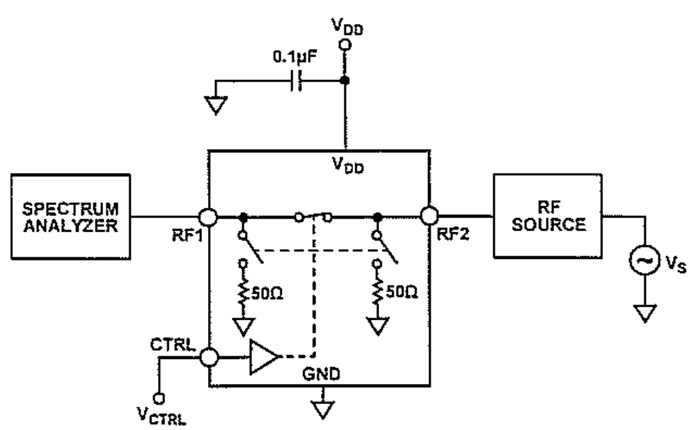


FIGURE 12. P1 dB.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Ordering Quantity	Vendor part number
V62/16613-01XE	24355	Tray 714 units	ADG901SCPZ-EP
		Reel 1500 units	ADG901SCPZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106