Evaluation Board User Guide
UG-582

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Evaluating the EVAL-CN0290-SDPZ

FEATURES

Self-contained board including:
- **ADF4106 PLL frequency synthesizer**
- **ADCLK905 ultrafast ECL clock/data buffer**
- **ADCLK925 ultrafast ECL clock/data buffer**
- **Ultralow noise voltage regulators: ADP150, ADP7102**
- **100 MHz VCXO**
- **USB interface**

Accompanying ADF4106 Integer-N software allows control of synthesizer functions from PC

ONLINE RESOURCES

Documents Needed
- **ADF4106 Data Sheet**
- **ADCLK905 Data Sheet**
- **ADCLK925 Data Sheet**
- **ADP150 Data Sheet**
- **ADP7102 Data Sheet**

Required Software
- **Integer-N programming software**

Design and Integration Files
- **Schematics, Layout Files, Bill of Materials**

EQUIPMENT NEEDED

A standard PC running Windows® XP, Windows Vista (32-bit), or Windows 7 with a USB port
EVAL-CN0290-SDPZ circuit evaluation board
5.5 V power supplies
A signal source, such as the Rohde & Schwarz SMA 100
A spectrum analyzer, such as the Rohde & Schwarz FSUP

GENERAL DESCRIPTION

The EVAL-CN0290-SDPZ is the evaluation board described in the Circuits From the Lab™ Circuit Note CN-0290, *Extending the Minimum Reference and Minimum Output Frequency of a Phase-Locked Loop.* A photo of the board is shown in Figure 1. It contains the ADF4106 synthesizer, the ADCLK905 clock buffer, ADCLK925 clock buffer, ultralow noise LDOs, and a 100 MHz VCXO. The board can be programmed using the ADF4106 Integer-N software. A USB cable is included with the board to connect to a PC USB port.

Additional information, including other PLL data sheets, technical notes, articles, and ADIsimPLL™ PLL simulation software from Analog Devices, Inc., is available at www.analog.com/pll.

PHOTO OF THE EVALUATION BOARD

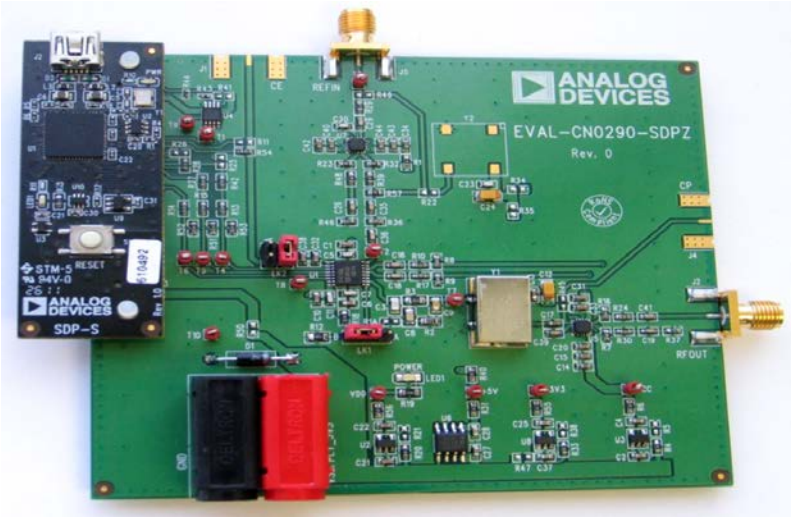

Figure 1. EVAL-CN0290-SDPZ

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REVISION HISTORY

8/13—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The user must apply 5.5 V to the VSUPPLY power connectors (4 mm banana connectors). LED 1 indicates when the main board is powered.

JUMPERS

Table 1 shows the required jumper positions for LK1 and LK2 for normal operation.

Table 1. Jumper Positions

Jumper	Position
LK1	B (RSET)
LK2	B (VDD)

Jumper LK1 in Position A enables the fastlock feature by the pin option, which is available on some PLL parts. The ADF4106 does not use this option; instead, the fastlock mode is enabled by programming the fastlock bit.

Jumper LK2 in Position A powers up the ADF4106 by writing to the CE pin.

RF OUTPUTS

The ADCLK925 RF output is ac-coupled out to the RFOUT SMA. RFOUT coupling to the spectrum analyzer should be set for 50 Ω. The unused RF output is terminated with a similar 50 Ω termination.

LOOP FILTER AND CHARGE PUMP CURRENT

The loop filter schematic is included in the evaluation board, and can be found at www.analog.com/CN0290-DesignSupport.

The default loop filter is set to 818 Hz. Using a charge pump setting of 5 mA is recommended.

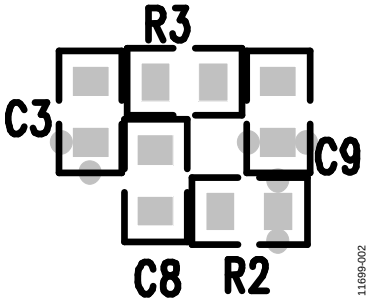

Figure 2. Loop Filter Layout

REFERENCE SOURCE

The default reference source for the board is an external reference using the REFIN SMA. The board has a footprint for a TCXO reference, if required.

In this case, remove the 51 Ω termination resistor, R36, and remove the 0 Ω link, R39, to isolate the ADCLK905 RF output.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

The control software for EVAL-CN0290-SDPZ uses the standard ADF4106 Integer-N programming software. For more details on the installation and use of this software, consult UG-476, *PLL Software Installation Guide,* and UG-161, *PLL Frequency Synthesizer Evaluation Board*.

After installing the software, run the software by clicking the **ADI PLL Int-N** file on the desktop or in the **Start** menu. The software front panel opens (see Figure 3).

Confirm that **SDP Board connected** is displayed in the bottom left corner of the window. Otherwise, the software has no connection to the evaluation board. In this case, check that the cable connection and USB drivers are correctly installed.

In the **Main Controls** tab of the software front panel, program the **RF VCO Output Frequency** to 100 MHz, the **PFD Frequency** to 1 MHz, the **Prescaler** to 8/9, and update all registers.

Note that the **RF VCO Output Frequency** box displayed in red, indicates that 100 MHz RF output frequency is below the data sheet minimum frequency level for a sine wave signal.

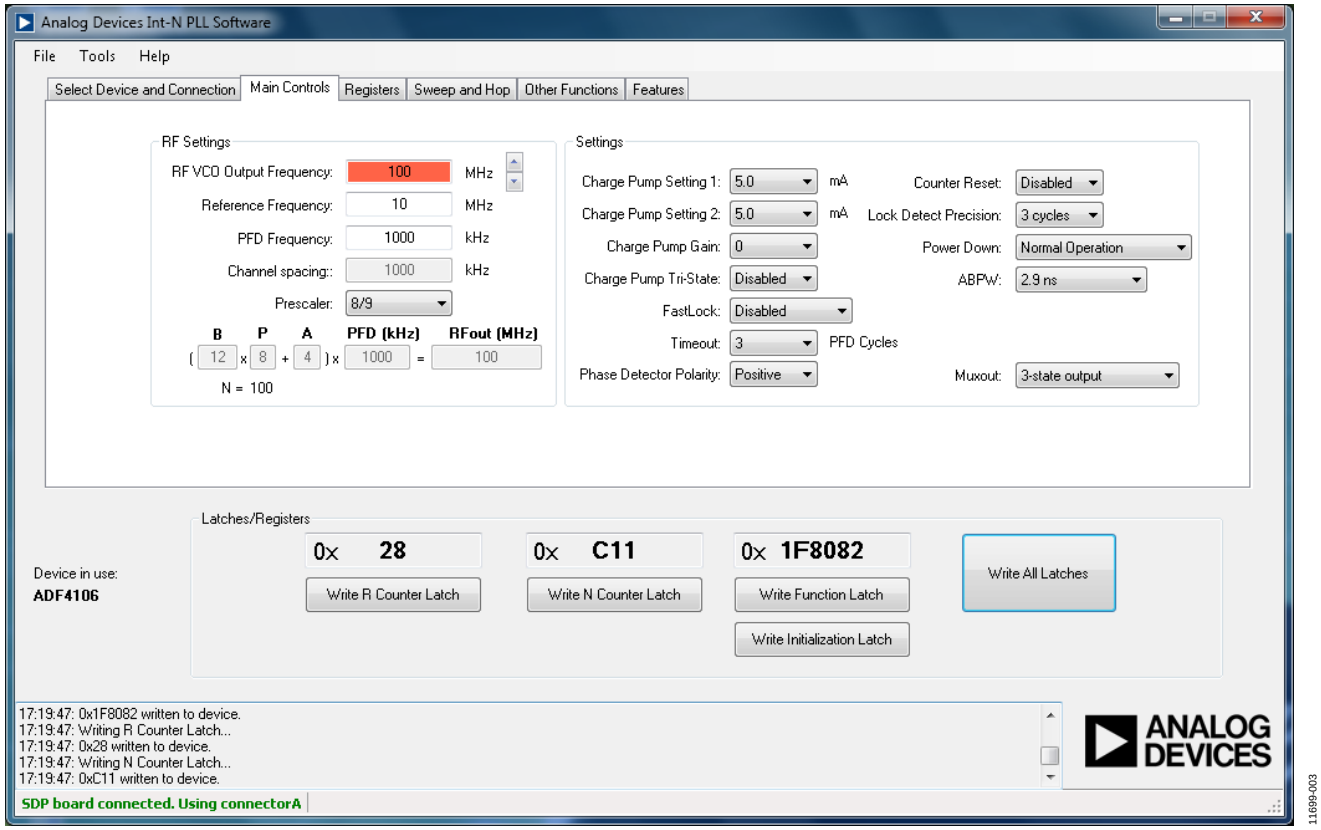

Figure 3. Software Front Panel

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ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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