REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add nominal dimension limits under figure 1. Update document paragraphs to current requirements. - ro	17-06-15	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV	A	A	A	A	A	A	A														
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REV STATUS OF PAGES			REV		A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
			PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY-MM-DD 11-07-21	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 8 CHANNEL, CMOS MULTIPLEXER, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** V62/11612
	REV A	**PAGE** 1 **OF** 24

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 8 channel CMOS multiplexer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/11612	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADG1408-EP	8 channel CMOS multiplexer

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MO-153-AB	Plastic thin shrink small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Positive supply voltage (V_{DD}) to negative supply voltage (V_{SS})	35 V
V_{DD} to ground (GND)	-0.3 V to +25 V
V_{SS} to GND	+0.3 V to -25 V
Analog inputs, digital inputs 2/	V_{SS} – 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Continuous current, source (S) or drain (D)	Table I data + 10%
Peak current, S or D (pulsed at 1 ms, 10% duty cycle maximum)	350 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature (T_J)	+150°C
Lead temperature, soldering:	
Vapor phase (60 seconds)	215°C
Infared (15 seconds)	220°C
Thermal resistance, junction to ambient (θ_{JC})	50°C/W
Thermal resistance, junction to ambient (θ_{JA})	150.4°C/W

1.4 Recommended operating conditions. 3/ 4/

Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Overvoltages at A, EN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

4/ All ratings and specifications, please refer to relevant EP datasheet.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuits. The timing waveforms and test circuits shall be as shown in figures 4 through 14.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
15 V dual supply.							
Unless otherwise specified, V_{DD} = +15 V ±10%, V_{SS} = -15 V, ±10%, GND = 0 V.							
Analog switch section.							
Analog signal range			-55°C to +125°C	01		V_{SS} to V_{DD}	V
On resistance	R_{ON}	V_S = ±10 V, I_S = -10 mA,	+25°C	01		4.7	Ω
		V_{DD} = +13.5 V, V_{SS} = -13.5 V, see figure 4	-55°C to +125°C			6.7	
On resistance match between channels	ΔR_{ON}	V_S = ±10 V, I_S = -10 mA,	+25°C	01		0.78	Ω
			-55°C to +125°C			1.1	
On resistance flatness	$R_{FLAT(ON)}$	V_S = ±10 V, I_S = -10 mA,	+25°C	01		0.72	Ω
			-55°C to +125°C			0.92	
Leakage current section.		V_{DD} = +16.5 V, V_{SS} = -16.5 V					
Source off leakage	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V,	+25°C	01		±0.2	nA
		see figure 5	-55°C to +125°C			±5	
Drain off leakage	$I_{D(off)}$	V_S = ±10 V, V_D = ∓10 V,	+25°C	01		±0.45	nA
		see figure 5	-55°C to +125°C			±30	
Channel on leakage	I_D,	V_S = V_D = ±10 V,	+25°C	01		±1.5	nA
	$I_{S(on)}$	see figure 6	-55°C to +125°C			±30	
Digital inputs section.							
Input high voltage	V_{INH}		-55°C to +125°C	01	2.0		V
Input low voltage	V_{INL}		-55°C to +125°C	01		0.8	V
Input current	I_{IN}	V_{IN} = V_{GND} or V_{DD}	+25°C	01	±0.005 typical		µA
			-55°C to +125°C			±0.1	
Digital input capacitance	C_{IN}		+25°C	01	4 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
15 V dual supply – continued.							
Unless otherwise specified, V_{DD} = +15 V ±10%, V_{SS} = -15 V, ±10%, GND = 0 V.							
Dynamic characteristics section. 2/							
Transition time	$t_{TRANSITION}$	V_S = 10 V, R_L = 100 Ω,	+25°C	01		170	ns
		C_L = 35 pF, see figure 7	-55°C to +125°C			240	
Break before make time delay	t_{BBM}	V_{S1} = V_{S2}= 10 V, R_L = 100 Ω,	+25°C	01	50 typical		ns
		C_L = 35 pF, see figure 8	-55°C to +125°C		19		
Active high digital input on time	$t_{ON(EN)}$	V_S = 10 V, R_L = 100 Ω,	+25°C	01		120	ns
		C_L = 35 pF, see figure 9	-55°C to +125°C			165	
Active high digital input off time	$t_{OFF(EN)}$	V_S = 10 V, R_L = 100 Ω,	+25°C	01		120	ns
		C_L = 35 pF, see figure 9	-55°C to +125°C			170	
Charge injection		V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see figure 10	+25°C	01	-50 typical		pC
Off isolation		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF, see figure 11	+25°C	01	-70 typical		dB
Channel to channel crosstalk		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF, see figure 12	+25°C	01	-70 typical		dB
Total harmonic distortion,	THD+N	f = 20 Hz to 20 kHz, R_L = 110 Ω, 15 V_{PP}, see figure 13	+25°C	01	0.025 typical		%
-3 dB bandwidth		R_L = 50 Ω, C_L = 5 pF, see figure 14	+25°C	01	60 typical		MHz
Insertion loss		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF, see figure 14	+25°C	01	0.24 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
15 V dual supply – continued.							
Unless otherwise specified, V_{DD} = +15 V ±10%, V_{SS} = -15 V, ±10%, GND = 0 V.							
Dynamic characteristics section – continued. 2/							
Source capacitance off	C_S(off)	f = 1 MHz	+25°C	01	14 typical		pF
Drain capacitance off	C_D(off)	f = 1 MHz	+25°C	01	80 typical		pF
Drain and source capacitance (on)	C_D, C_S (on)	f = 1 MHz	+25°C	01	135 typical		pF
Power requirements section.		V_{DD} = +16.5 V, V_{SS} = -16.5 V					
Positive supply current	I_{DD}	Digital inputs = 0 V or V_{DD}	+25°C	01	0.002 typical		µA
			-55°C to +125°C			1	
		Digital inputs = 5 V	+25°C		220 typical		
			-55°C to +125°C			420	
Negative supply current	I_{SS}	Digital inputs = 0 V, 5 V, or V_{DD}	+25°C	01	0.002 typical		µA
			-55°C to +125°C			1	
Positive power supply voltage	V_{DD}		-55°C to +125°C	01	±4.5		V
Negative power supply voltage	V_{SS}		-55°C to +125°C	01		±16.5	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
12 V single supply .							
Unless otherwise specified, V_{DD} = +12 V ±10%, V_{SS} = 0 V, GND = 0 V.							
Analog switch section.							
Analog signal range			-55°C to +125°C	01		0 to V_{DD}	V
On resistance	R_{ON}	V_S = 0 V to 10 V, I_S = -10 mA, V_{DD} = 10.8 V, V_{SS} = 0 V, see figure 4	+25°C	01		8	Ω
			-55°C to +125°C			11.2	
On resistance match between channels	ΔR_{ON}	V_S = 0 V to 10 V, I_S = -10 mA,	+25°C	01		0.82	Ω
			-55°C to +125°C			1.1	
On resistance flatness	$R_{F(ON)}$	V_S = 0 V to10 V, I_S = -10 mA,	+25°C	01		2.5	Ω
			-55°C to +125°C			2.8	
Leakage current section.		V_{DD} = 13.2 V					
Source off leakage	$I_S(off)$	V_S = 1 V and 10 V, V_D = 10 V and 1 V, see figure 5	+25°C	01		±0.2	nA
			-55°C to +125°C			±5	
Drain off leakage	$I_D(off)$	V_S = 1 V and 10 V, V_D = 10 V and 1 V, see figure 5	+25°C	01		±0.45	nA
			-55°C to +125°C			±37	
Channel on leakage	I_D, $I_S(on)$	V_S = V_D = 1 V or 10 V, see figure 6	+25°C	01		±0.44	nA
			-55°C to +125°C			±32	
Digital inputs section.							
Input high voltage	V_{INH}		-55°C to +125°C	01	2.0		V
Input low voltage	V_{INL}		-55°C to +125°C	01		0.8	V
Input current	I_{IN}	V_{IN} = V_{GND} or V_{DD}	+25°C	01	±0.005 typical		µA
			-55°C to +125°C			±0.1	
Digital input capacitance	C_{IN}		+25°C	01	5 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
12 V single supply - continued.							
Unless otherwise specified, V_{DD} = +12 V ±10%, V_{SS} = 0 V, GND = 0 V.							
Dynamic characteristics section. 2/							
Transition time	$t_{TRANSITION}$	V_S = 8 V, R_L = 100 Ω,	+25°C	01		260	ns
		C_L = 35 pF, see figure 7	-55°C to +125°C			380	
Break before make time delay	t_{BBM}	V_{S1} = V_{S2} = 8 V, R_L = 100 Ω,	+25°C	01	90 typical		ns
		C_L = 35 pF, see figure 8	-55°C to +125°C		40		
Active high digital input on time	$t_{ON(EN)}$	V_S = 8 V, R_L = 100 Ω,	+25°C	01		210	ns
		C_L = 35 pF, see figure 9	-55°C to +125°C			285	
Active high digital input off time	$t_{OFF(EN)}$	V_S = 8 V, R_L = 100 Ω,	+25°C	01		145	ns
		C_L = 35 pF, see figure 9	-55°C to +125°C			200	
Charge injection		V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see figure 10	+25°C	01	-12 typical		pC
Off isolation		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF, see figure 11	+25°C	01	-70 typical		dB
Channel to channel crosstalk		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF, see figure 12	+25°C	01	-70 typical		dB
-3 dB bandwidth		R_L = 50 Ω, C_L = 5 pF, see figure 14	+25°C	01	36 typical		MHz
Insertion loss		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF, see figure 14	+25°C	01	0.5 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
12 V single supply – continued.							
Unless otherwise specified, V_{DD} = +12 V ±10%, V_{SS} = 0 V, GND = 0 V.							
Dynamic characteristics section - continued. 2/							
Source capacitance off	C_S(off)	f = 1 MHz	+25°C	01	25 typical		pF
Drain capacitance off	C_D(off)	f = 1 MHz	+25°C	01	165 typical		pF
Drain and source capacitance (on)	C_D, C_S (on)	f = 1 MHz	+25°C	01	200 typical		pF
Power requirements section.		V_{DD} = 13.2 V					
Positive supply current	I_{DD}	Digital inputs = 0 V or V_{DD}	+25°C	01	0.002 typical		µA
			-55°C to +125°C			1	
		Digital inputs = 5 V	+25°C		220 typical		
			-55°C to +125°C			420	
Positive power supply voltage	V_{DD}	V_{SS} = 0 V, GND = 0 V	-55°C to +125°C	01	5	16.5	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
5 V dual supply .							
Unless otherwise specified, V_{DD} = +5 V ±10%, V_{SS} = -5 V, ±10%, GND = 0 V.							
Analog switch section.							
Analog signal range			-55°C to +125°C	01		V_{SS} to V_{DD}	V
On resistance	R_{ON}	V_S = ±4.5 V, I_S = -10 mA,	+25°C	01		9	Ω
		V_{DD} = +4.5 V, V_{SS} = -4.5 V, see figure 4	-55°C to +125°C			12	
On resistance match between channels	ΔR_{ON}	V_S = ±4.5 V, I_S = -10 mA,	+25°C	01		0.78	Ω
			-55°C to +125°C			1.1	
On resistance flatness	$R_{FLAT(ON)}$	V_S = ±4.5 V, I_S = -10 mA,	+25°C	01		2.5	Ω
			-55°C to +125°C			3	
Leakage current section.		V_{DD} = +5.5 V, V_{SS} = -5.5 V					
Source off leakage	I_S(off)	V_S = ±4.5 V, V_D = $\mp$4.5 V,	+25°C	01		±0.2	nA
		see figure 5	-55°C to +125°C			±5	
Drain off leakage	I_D(off)	V_S = ±4.5 V, V_D = $\mp$4.5 V,	+25°C	01		±0.45	nA
		see figure 5	-55°C to +125°C			±20	
Channel on leakage	I_D,	V_S = V_D = ±4.5 V,	+25°C	01		±0.3	nA
	I_S(on)	see figure 6	-55°C to +125°C			±22	
Digital inputs section.							
Input high voltage	V_{INH}		-55°C to +125°C	01	2.0		V
Input low voltage	V_{INL}		-55°C to +125°C	01		0.8	V
Input current	I_{IN}	V_{IN} = V_{GND} or V_{DD}	+25°C	01	±0.005 typical		µA
			-55°C to +125°C			±0.1	
Digital input capacitance	C_{IN}		+25°C	01	5 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
5 V dual supply – continued.							
Unless otherwise specified, V_{DD} = +5 V ±10%, V_{SS} = -5 V, ±10%, GND = 0 V.							
Dynamic characteristics section. 2/							
Transition time	$t_{TRANSITION}$	V_S = 5 V, R_L = 100 Ω,	+25°C	01		440	ns
		C_L = 35 pF, see figure 7	-55°C to +125°C			550	
Break before make time delay	t_{BBM}	V_{S1} = V_{S2}= 5 V, R_L = 100 Ω,	+25°C	01	100 typical		ns
		C_L = 35 pF, see figure 8	-55°C to +125°C		45		
Active high digital input on time	$t_{ON(EN)}$	V_S = 5 V, R_L = 100 Ω,	+25°C	01		330	ns
		C_L = 35 pF, see figure 9	-55°C to +125°C			440	
Active high digital input off time	$t_{OFF(EN)}$	V_S = 5 V, R_L = 100 Ω,	+25°C	01		285	ns
		C_L = 35 pF, see figure 9	-55°C to +125°C			370	
Charge injection		V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see figure 10	+25°C	01	-10 typical		pC
Off isolation		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF, see figure 11	+25°C	01	-70 typical		dB
Channel to channel crosstalk		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF, see figure 12	+25°C	01	-70 typical		dB
Total harmonic distortion,	THD+N	f = 20 Hz to 20 kHz, R_L = 110 Ω, 5 V_{PP}, see figure 13	+25°C	01	0.06 typical		%
-3 dB bandwidth		R_L = 50 Ω, C_L = 5 pF, see figure 14	+25°C	01	40 typical		MHz
Insertion loss		f = 1 MHz, R_L = 50 Ω, C_L = 5 pF, see figure 14	+25°C	01	0.5 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
5 V dual supply – continued.							
Unless otherwise specified, V_{DD} = +5 V ±10%, V_{SS} = -5 V, ±10%, GND = 0 V.							
Dynamic characteristics section – continued. 2/							
Source capacitance off	C_S(off)	f = 1 MHz	+25°C	01	20 typical		pF
Drain capacitance off	C_D(off)	f = 1 MHz	+25°C	01	130 typical		pF
Drain and source capacitance (on)	C_D, C_S (on)	f = 1 MHz	+25°C	01	180 typical		pF
Power requirements section.		V_{DD} = +5.5 V, V_{SS} = -5.5 V					
Positive supply current	I_{DD}	Digital inputs = 0 V or V_{DD}	+25°C	01	0.001 typical		µA
			-55°C to +125°C			1	
Negative supply current	I_{SS}	Digital inputs = 0 V, 5 V, or V_{DD}	+25°C	01	0.001 typical		µA
			-55°C to +125°C			1	
Positive power supply voltage	V_{DD}		-55°C to +125°C	01	±4.5		V
Negative power supply voltage	V_{SS}		-55°C to +125°C	01		±16.5	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Continuous current, per channel, source (S) or drain (D). 2/							
Continuous current, 15 V dual supply		V_{DD} = +13.5 V, V_{SS} = -13.5 V	25°C	01		190	mA
			85°C			105	
			125°C			50	
Continuous current, 12 V single supply		V_{DD} = 10.8 V, V_{SS} = 0 V	25°C	01		160	mA
			85°C			95	
			125°C			50	
Continuous current, 5 V dual supply		V_{DD} = +4.5, V_{SS} = -4.5 V	25°C	01		155	mA
			85°C			90	
			125°C			45	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Guaranteed by design, not subject to production test.

Case X

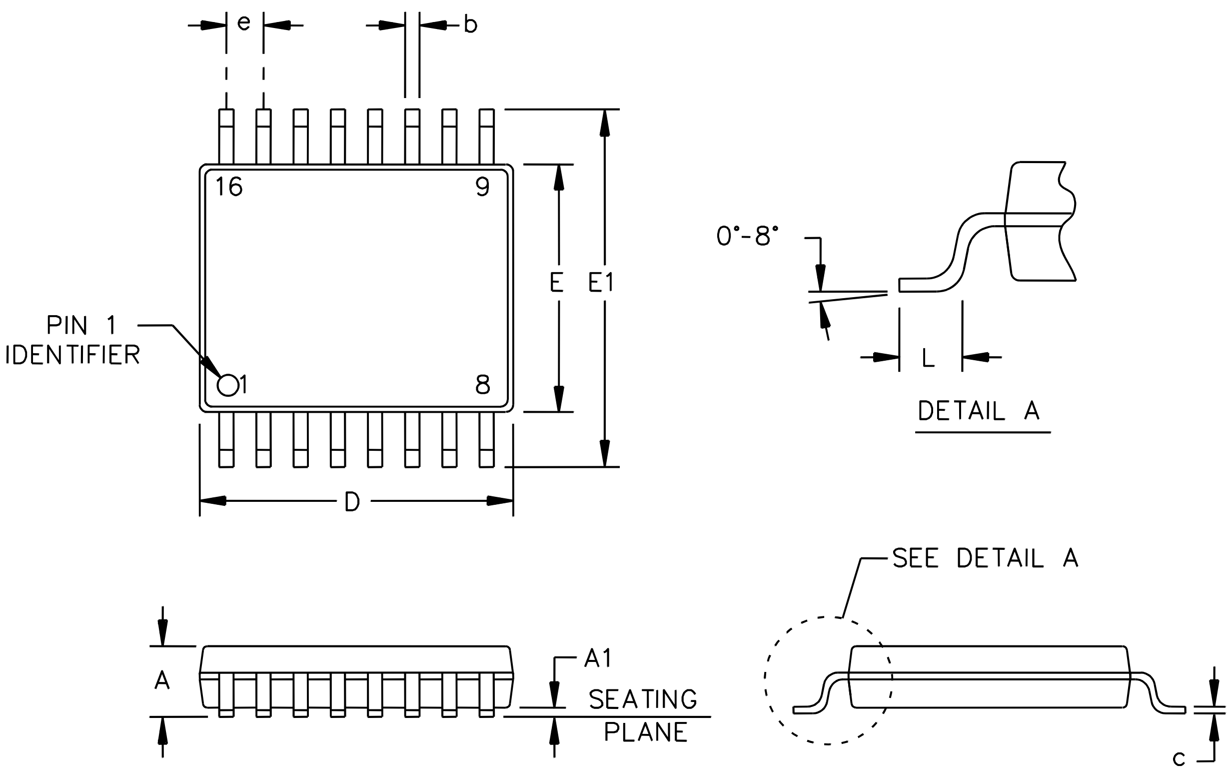


FIGURE 1. Case outline.

Case X – continued.

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	---	---	.047	---	---	1.20
A1	.001	---	.005	0.05	---	0.15
b	.007	---	.011	0.19	---	0.30
c	.003	---	.007	0.09	---	0.20
D	.192	.196	.200	4.90	5.00	5.10
E	.169	.173	.177	4.30	4.40	4.50
E1	.251 BSC			6.40 BSC		
e	.025 BSC			0.65 BSC		
L	.017	.023	.029	0.45	0.60	0.75

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-153-AB.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	A0	Logic control input.
2	EN	Active high digital input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	V_{SS}	Most negative power supply potential. In supply single applications, it can be connected to ground.
4	S1	Source terminal 1. Can be an input or an output.
5	S2	Source terminal 2. Can be an input or an output.
6	S3	Source terminal 3. Can be an input or an output.
7	S4	Source terminal 4. Can be an input or an output.
8	D	Drain terminal. Can be an input or an output.
9	S8	Source terminal 8. Can be an input or an output.
10	S7	Source terminal 7. Can be an input or an output.
11	S6	Source terminal 6. Can be an input or an output.
12	S5	Source terminal 5. Can be an input or an output.
13	V_{DD}	Most positive power supply potential.
14	GND	Ground (0 V) reference.
15	A2	Logic control input.
16	A1	Logic control input.

FIGURE 2. Terminal connections.

A2	A1	A0	EN	On switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

FIGURE 3. Truth table.

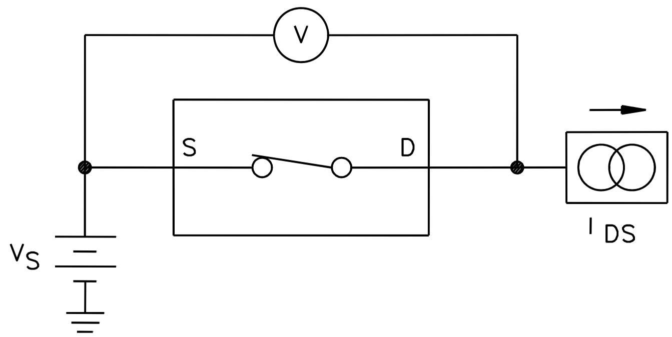


FIGURE 4. On resistance.

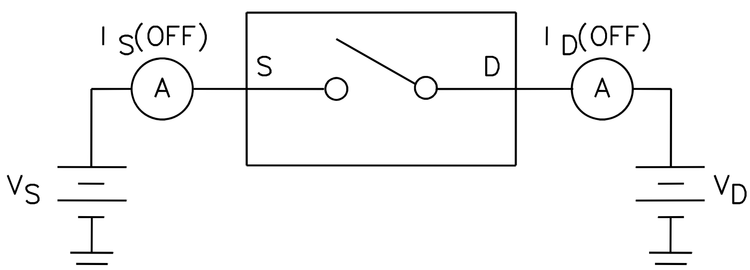


FIGURE 5. Off leakage.

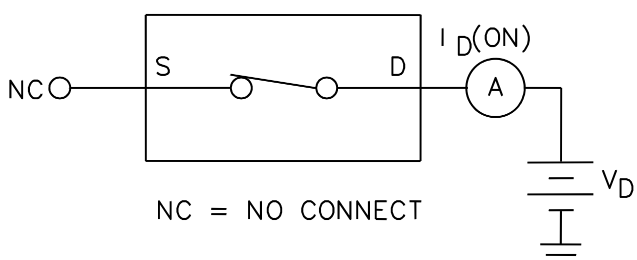


FIGURE 6. On leakage.

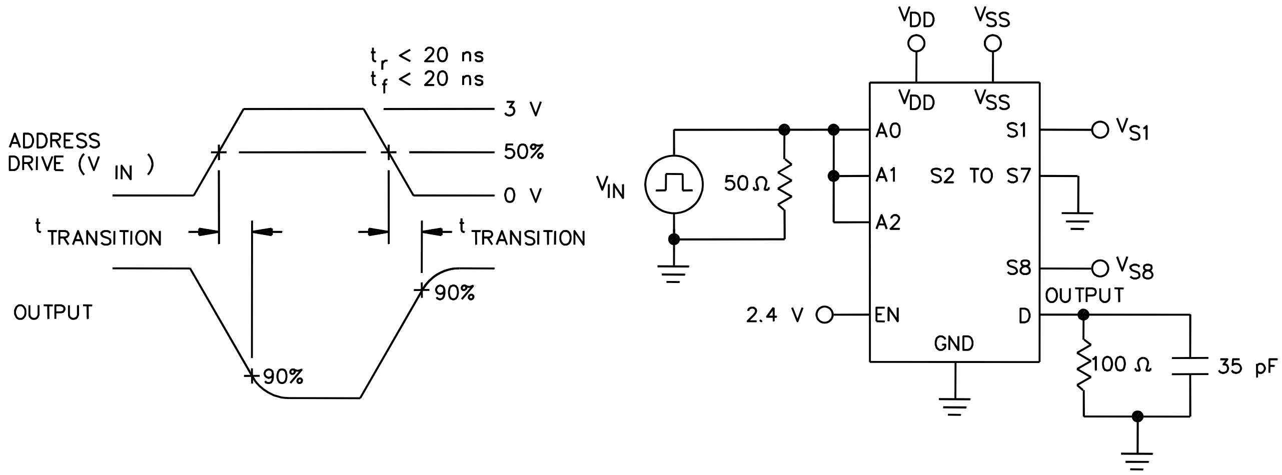


FIGURE 7. Address to output switching times, $t_{TRANSITIONS}$.

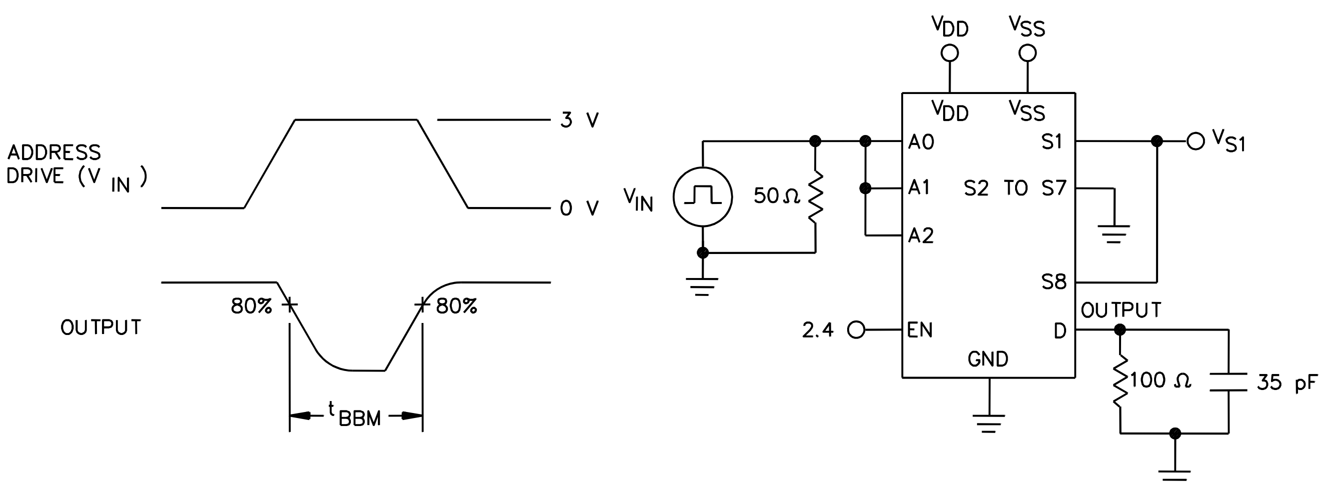


FIGURE 8. Break before make delay, t_{BBM}.

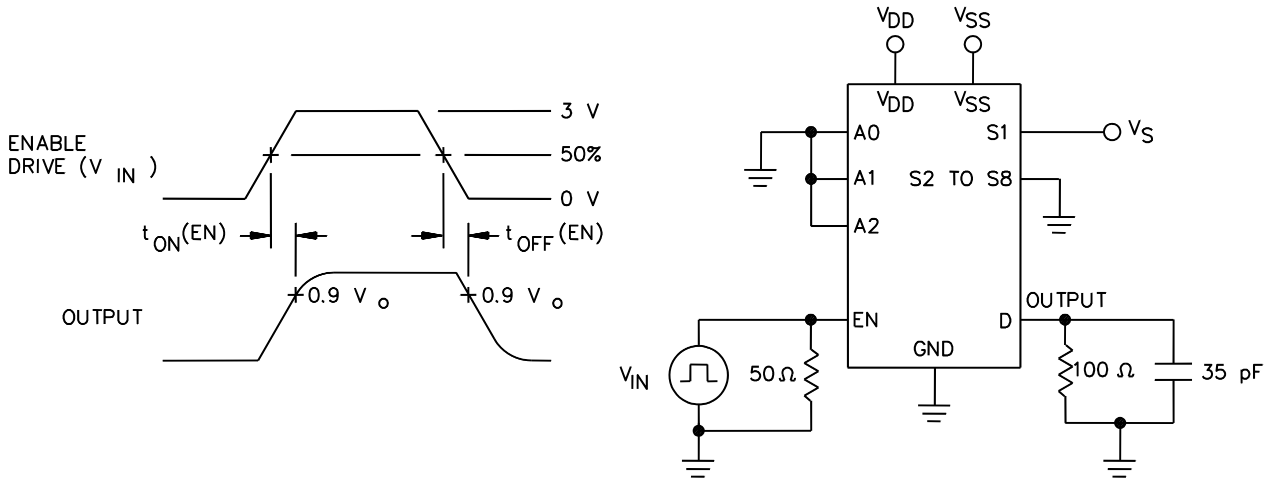


FIGURE 9. Enable delay, t_{ON} (EN), t_{OFF} (EN).

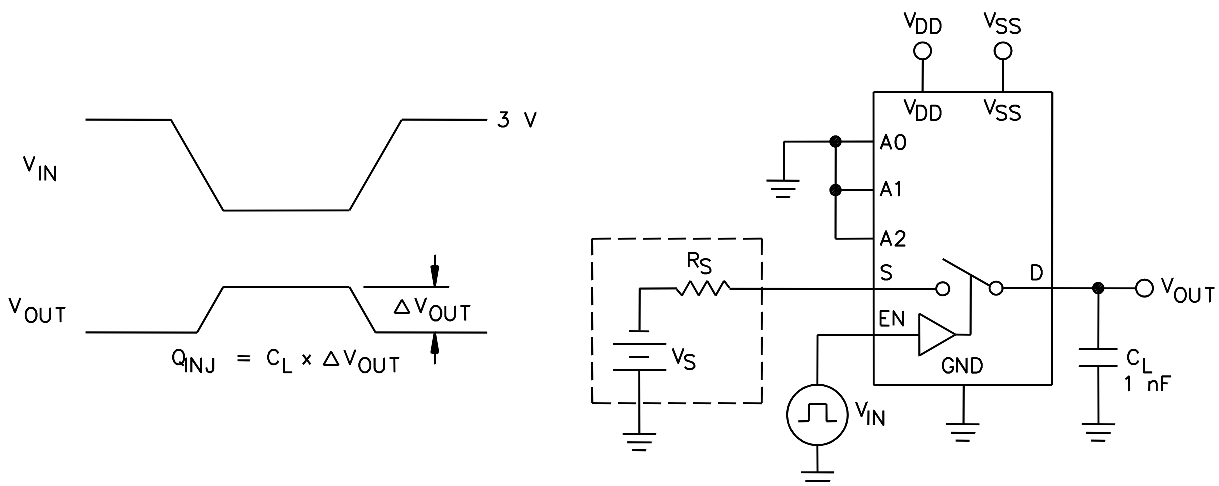


FIGURE 10. Charge injection.

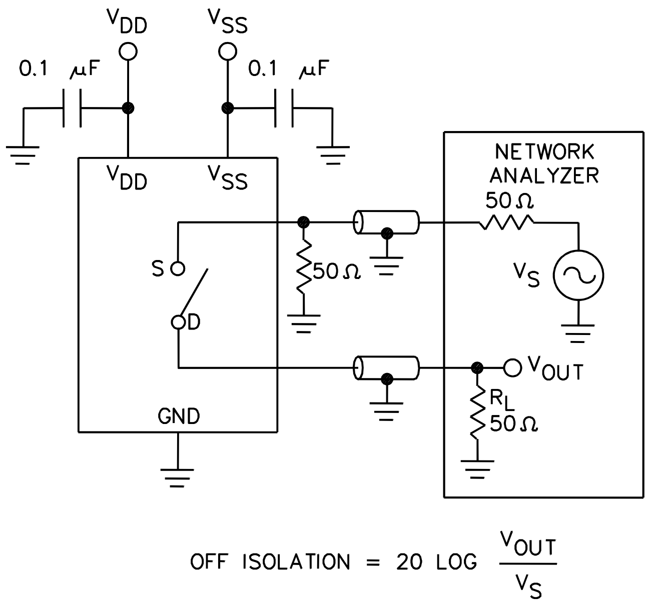


FIGURE 11. <u>Off isolation</u>.

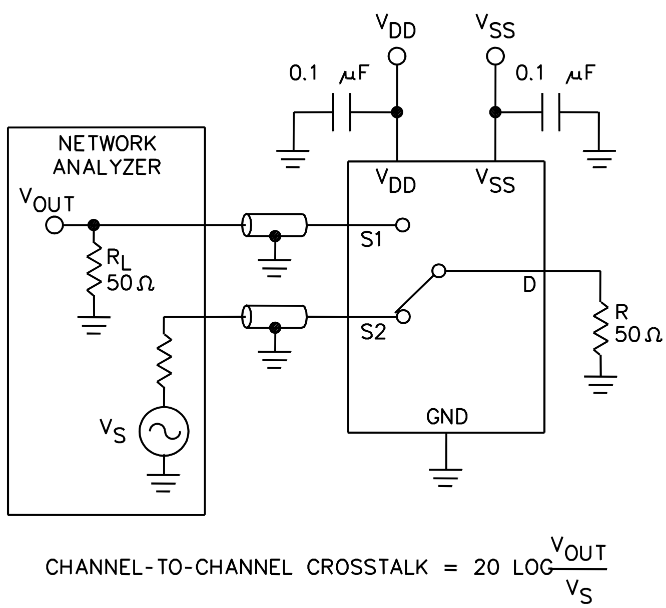


FIGURE 12. <u>Channel to channel crosstalk</u>.

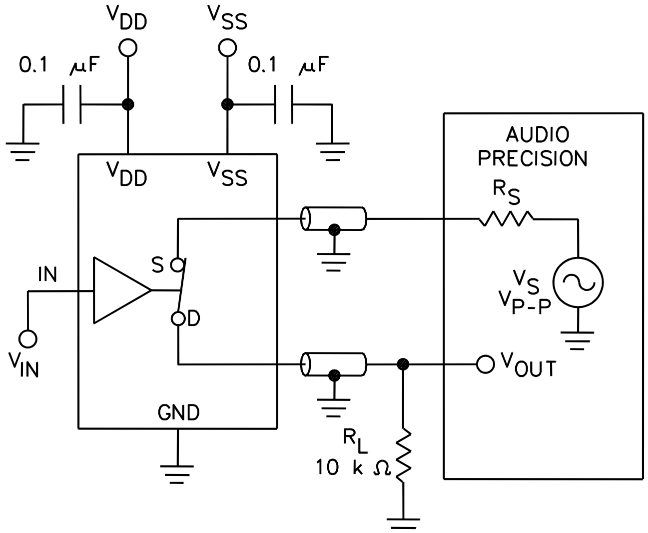
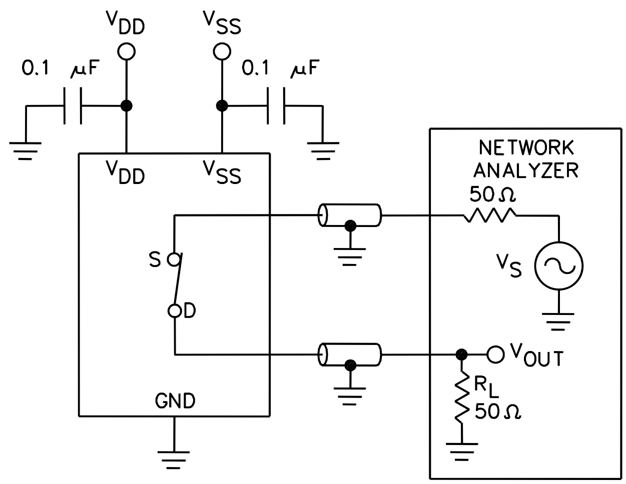


FIGURE 13. THD + noise.



$$\text{INSERTION LOSS} = 20\ \text{LOG}\ \frac{V_{OUT}\ \text{WITH SWITCH}}{V_{OUT}\ \text{WITHOUT SWITCH}}$$

FIGURE 14. Insertion loss.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/11612-01XB	24355	ADG1408SRU-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland