REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A

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Original date of drawing
YY MM DD
13-01-08

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Thomas M. Hess

TITLE

MICROCIRCUIT, LINEAR, 400 MHz TO 6 GHz BROADBAND QUADRATURE MODULATOR , MONOLITHIC SILICON

SIZE	**CODE IDENT. NO.**	**DWG NO.**
A	**16236**	**V62/12649**

REV

PAGE 1 **OF** 11

AMSC N/A

5962-V035-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 400 MHz to 6 GHz broadband quadrature modulator microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12649	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADL5375-EP	400 MHz to 6 GHz broadband quadrature modulator

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	24	JEDEC MO-220-WGGD	Lead Frame Chip Scale Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage, VPOS	5.5 V
IBBP, IBBN, QBBP, QBBN	0 V to 2 V
LOIP and LOIN	13 dBm
Internal power dissipation	1500 mW
θ_{JA} (Exposed paddle soldered down)	54 °C/W 2/
Operating temperature range:	-55°C to +105°C
Storage temperature range	-65°C to 150°C
Maximum junction temperature	150°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-2	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Per JEDC standard JESD 51-2.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Return Loss of LOIP (LOIN AC-Coupled to Ground) S11 and RFOUT S22 from 450 MHz to 6000 MHz. The Return Loss of LOIP (LOIN AC-Coupled to Ground) S11 and RFOUT S22 from 450 MHz to 6000 MHz shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Test conditions 2/	Limits			Unit
		Min	Typ	Max	
Operating frequency range					
Low frequency			400		MHz
High frequency			6000		
LO = 450 MHz					
Output power, P_{OUT}	V_{IQ} = 1 V p-p differential		0.85		dBm
Modulator voltage gain	RF output divided by baseband input voltage		-3.1		dB
Output P1dB			9.6		dBm
Output return loss			-16.4		dB
Carrier feedthrough			-47.5		dBm
Sideband suppression			-37.6		dBc
Quadrature error			1.7		Degrees
I/Q amplitude balance			0.07		dB
Second Harmonic	$P_{OUT} – (f_{LO} + (2 \times f_{BB}))$, P_{OUT} = 0.85 dBm		-75.9		dBc
Third Harmonic	$P_{OUT} – (f_{LO} + (3 \times f_{BB}))$, P_{OUT} = 0.85 dBm		-51.5		dBc
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz,		65.4		dBm
Output IP3	baseband I/Q amplitude per tone = 0.5 V p-p differential		26.6		
Noise floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		-160.5		dBm/Hz
LO = 900 MHz					
Output power, P_{OUT}	V_{IQ} = 1 V p-p differential		0.75		dBm
Modulator voltage gain	RF output divided by baseband input voltage		-3.2		dB
Output P1dB			9.6		dBm
Output return loss			-15.7		dB
Carrier feedthrough			-45.1		dBm
Sideband suppression			-52.8		dBc
Quadrature error			0.01		Degrees
I/Q amplitude balance			0.07		dB
Second Harmonic	$P_{OUT} – (f_{LO} + (2 \times f_{BB}))$, P_{OUT} = 0.75 dBm		-75.8		dBc
Third Harmonic	$P_{OUT} – (f_{LO} + (3 \times f_{BB}))$, P_{OUT} = 0.75 dBm		-50.7		dBc
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz,		62.6		dBm
Output IP3	baseband I/Q amplitude per tone = 0.5 V p-p differential		25.9		
Noise floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		-160.0		dBm/Hz
LO = 1900 MHz					
Output power, P_{OUT}	V_{IQ} = 1 V p-p differential		0.53		dBm
Modulator voltage gain	RF output divided by baseband input voltage		-3.4		dB
Output P1dB			9.9		dBm
Output return loss			-16.2		dB
Carrier feedthrough			-40.3		dBm
Sideband suppression			-50.2		dBc
Quadrature error			0.02		Degrees
I/Q amplitude balance			0.07		dB
Second Harmonic	$P_{OUT} – (f_{LO} + (2 \times f_{BB}))$, P_{OUT} = 0.53 dBm		-67.9		dBc
Third Harmonic	$P_{OUT} – (f_{LO} + (3 \times f_{BB}))$, P_{OUT} = 0.53 dBm		-51.8		dBc

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions 2/	Limits			Unit
		Min	Typ	Max	
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz,		62.6		dBm
Output IP3	baseband I/Q amplitude per tone = 0.5 V p-p differential		24.3		
Noise floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		-160.0		dBm/Hz
LO = 2150 MHz					
Output power, P_{OUT}	V_{IQ} = 1 V p-p differential		0.73		dBm
Modulator voltage gain	RF output divided by baseband input voltage		-3.2		dB
Output P1dB			10.0		dBm
Output return loss			-17.1		dB
Carrier feedthrough			-39.7		dBm
Sideband suppression			-47.3		dBc
Quadrature error			-0.16		Degrees
I/Q amplitude balance			0.07		dB
Second Harmonic	$P_{OUT} – (f_{LO} + (2 \times f_{BB}))$, P_{OUT} = 0.73 dBm		-71.3		dBc
Third Harmonic	$P_{OUT} – (f_{LO} + (3 \times f_{BB}))$, P_{OUT} = 0.73 dBm		-52.4		dBc
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz,		61.6		dBm
Output IP3	baseband I/Q amplitude per tone = 0.5 V p-p differential		24.2		
Noise floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		-159.5		dBm/Hz
LO = 2600 MHz					
Output power, P_{OUT}	V_{IQ} = 1 V p-p differential		0.61		dBm
Modulator voltage gain	RF output divided by baseband input voltage		-3.4		dB
Output P1dB			9.6		dBm
Output return loss			-19.3		dB
Carrier feedthrough			-36.5		dBm
Sideband suppression			-48.3		dBc
Quadrature error			-0.37		Degrees
I/Q amplitude balance			0.07		dB
Second Harmonic	$P_{OUT} – (f_{LO} + (2 \times f_{BB}))$, P_{OUT} = 0.61 dBm		-60.9		dBc
Third Harmonic	$P_{OUT} – (f_{LO} + (3 \times f_{BB}))$, P_{OUT} = 0.61 dBm		-51.3		dBc
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz,		55.0		dBm
Output IP3	baseband I/Q amplitude per tone = 0.5 V p-p differential		22.7		
Noise floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		-159.0		dBm/Hz
LO = 3500 MHz					
Output power, P_{OUT}	V_{IQ} = 1 V p-p differential		0.21		dBm
Modulator voltage gain	RF output divided by baseband input voltage		-3.8		dB
Output P1dB			9.6		dBm
Output return loss			-20.7		dB
Carrier feedthrough			-30.4		dBm
Sideband suppression			-48.3		dBc
Quadrature error			0.01		Degrees
I/Q amplitude balance			0.08		dB
Second Harmonic	$P_{OUT} – (f_{LO} + (2 \times f_{BB}))$, P_{OUT} = 0.21 dBm		-55.8		dBc
Third Harmonic	$P_{OUT} – (f_{LO} + (3 \times f_{BB}))$, P_{OUT} = 0.21 dBm		-50.2		dBc
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz,		51.1		dBm
Output IP3	baseband I/Q amplitude per tone = 0.5 V p-p differential		23.1		
Noise floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		-157.6		dBm/Hz

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

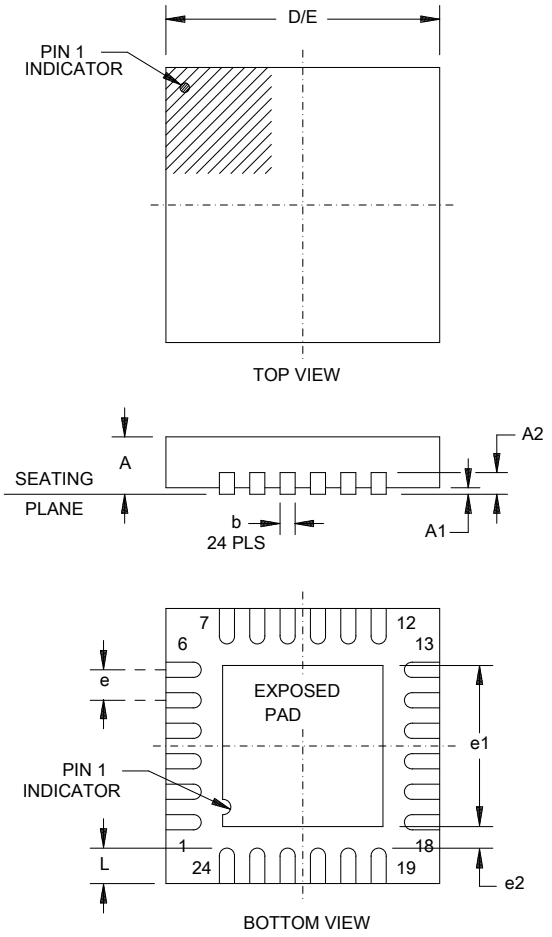
Test	Test conditions 2/	Limits			Unit
		Min	Typ	Max	
LO = 5800 MHz					
Output power, P_{OUT}	V_{IQ} = 1 V p-p differential		-1.36		dBm
Modulator voltage gain	RF output divided by baseband input voltage		-5.3		dB
Output P1dB			4.9		dBm
Output return loss			-7.4		dB
Carrier feedthrough			-19.5		dBm
Sideband suppression			-38.2		dBc
Quadrature error			-0.51		Degrees
I/Q amplitude balance			-0.05		dB
Second Harmonic	$P_{OUT} – (f_{LO} + (2 \times f_{BB}))$, P_{OUT} = -1.36 dBm		-52.6		dBc
Third Harmonic	$P_{OUT} – (f_{LO} + (3 \times f_{BB}))$, P_{OUT} = -1.36 dBm		-45.7		dBc
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz,		39.1		dBm
Output IP3	baseband I/Q amplitude per tone = 0.5 V p-p differential		14.6		
Noise floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		-153.0		dBm/Hz
LO inputs					
LO drive level	Characterization performed at typical level	-6	0	+6	dBm
Input return loss	500 MHz < f_{LO} < 3.3 GHz, see FIGURE 5 for return loss vs frequency		≤-10		dB
Baseband inputs (Pin IBBP, Pin IBBN, Pin QBBP, Pin QBBN)					
I/Q input bias level 3/			500		mV
Absolute voltage level 3/	On Pin IBBP, Pin IBBN, Pin QBBP, Pin QBBN	0		1	V
Input bias current	Current sourcing from each baseband input		41		µA
Input offset current			0.1		
Differential input impedance			60		kΩ
Bandwidth (0.1 dB)	LO = 1900 MHz, base band input = 500 mV p-p sine wave		95		MHz
Output disable (Pin DSOP)					
Off isolation	P_{OUT} (DSOP low) – P_{OUT} (DSOP high)		84		dB
	DSOP high, LO leakage, LO = 2150 MHz		-55		dBm
Turn ON settling time	DSOP high to low (90% of envelope)		220		ns
Turn OFF settling time	DSOP low to high (10% of envelope)		100		ns
DSOP high level (Logic 1)		2.0			V
DSOP low level (Logic 0)				0.8	
Power supply (Pin VPS1 and VPS2)					
Voltage		4.75		5.25	V
Supply current	DSOP = low		194		mA
	DSOP = High		126		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_S = 5 V; T_A = 25°C; LO = 0 dBm single-ended drive; baseband I/Q amplitude = 1 V p-p differential sine waves in quadrature with a 500 mV dc bias; baseband I/Q frequency (f_{BB}) = 1 MHz, unless otherwise noted.

3/ The input bias level can vary as long as the voltages on the individual IBBP, IBBN, QBBP, and QBBN pins remain within the specified absolute voltage level.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.70	0.80	e	0.50 BSC	
A1		0.05	e1	2.45	2.65
A2	0.20 REF		e2	0.25	
b	0.18	0.30	L	0.30	0.50
D/E	3.90	4.10			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-220-WGGD.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DSOP	13	NC
2	COMM	14	COMM
3	LOIP	15	NC
4	LOIN	16	RFOUT
5	COMM	17	COMM
6	NC	18	VPS1
7	NC	19	COMM
8	COMM	20	COMM
9	QBBN	21	IBBP
10	QBBP	22	IBBN
11	COMM	23	COMM
12	COMM	24	VPS2

NOTES:

1. NC = No connect. Do not connect to this pin.
2. Connect to the ground plane via a low impedance path.

FIGURE 2. Terminal connections.

Case outline X		
Terminal		Description
Number	Mnemonic	
1	DSOP	Output disable. A logic high on this pin disables the RF output. Connect this pin to ground or leave it floating to enable the output
2, 5, 8, 11, 12, 14, 17, 19, 20, 23	COMM	Input Common pins. Connect to ground plane via a low impedance path.
3,4	LOIP, LOIN	Local Oscillator inputs. Single-ended operation: The LOIP pin is driven from the LO source through an AC-coupling capacitor while the LOIN pin is ac-coupled to ground through a capacitor. Differential operation: The LOIP and LOIN pins must be driven differentially through ac-coupling capacitors in this mode of operation.
6, 7, 13, 15	NC	No connect. These pins can be left open or tied to ground.
9, 10, 21, 22	QBBN, QBBP, IBBN, IBBP	Differential in phase and Quadrature baseband inputs. These high impedance inputs should be dc-biased to the recommended level (500 mV). These inputs should be driven from a low impedance source. Nominal characterized ac signal swing is 500 mV p-p on each pin. This results in a differential drive of 1 V p-p. These inputs are not self-biased and must be externally biased.
16	RFOUT	RF output. Single ended, 50 Ω internally biased RF output. RFOUT must be ac-coupled to the load.
18, 24	VPS1, VPS2	Positive supply voltage pins. All pins should be connected to the same supply (V_S). To ensure adequate external bypassing, connect 0.1 µF and 100 pF capacitors between each pin and ground.
	EP	Exposed paddle. Connect to the ground plane via a low impedance path.

FIGURE 3. Terminal function.

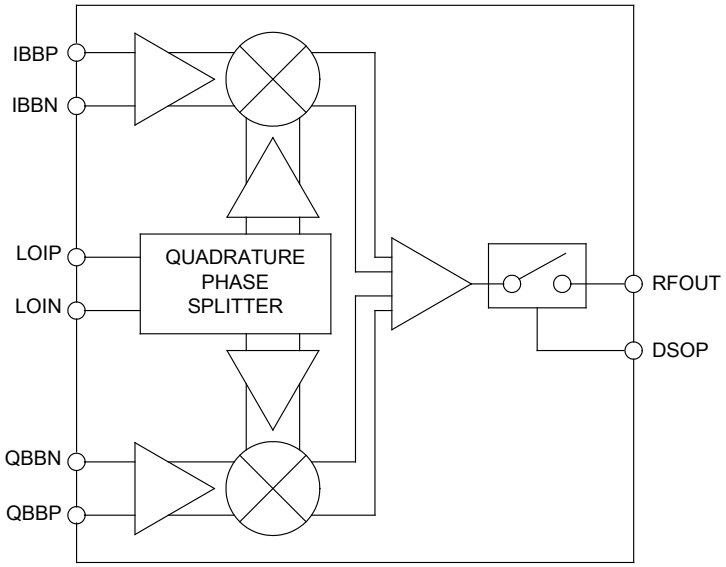


FIGURE 4. Functional block diagram.

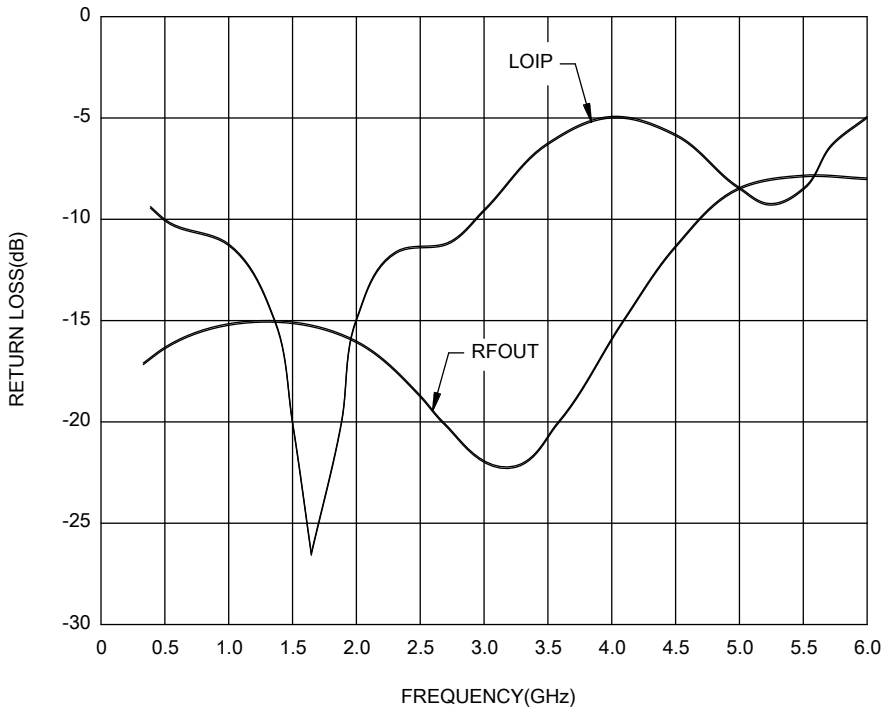


FIGURE 5. Return Loss of LOIP (LOIN AC-Coupled to Ground) S11 and RFOUT S22 from 450 MHz to 6000 MHz.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12649-01XE	24355	ADL5375-05SCPZEPR7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106