

High Performance Digital MEMS Microphone Standard Digital Audio Interface to Blackfin DSP

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 allows up to two digital microelectromechanical systems (MEMS) microphones to be interfaced to a digital signal processor (DSP) on a single data line. The ADMP441 consists of a MEMS microphone element and an I²S output. The I²S output allows stereo microphones to be used in an audio system without the need for a codec between the microphones and the processor. The ADMP MEMS microphones have a high signal-to-noise ratio (SNR) and a flat wideband frequency response, making them an excellent choice for high performance, low power applications.

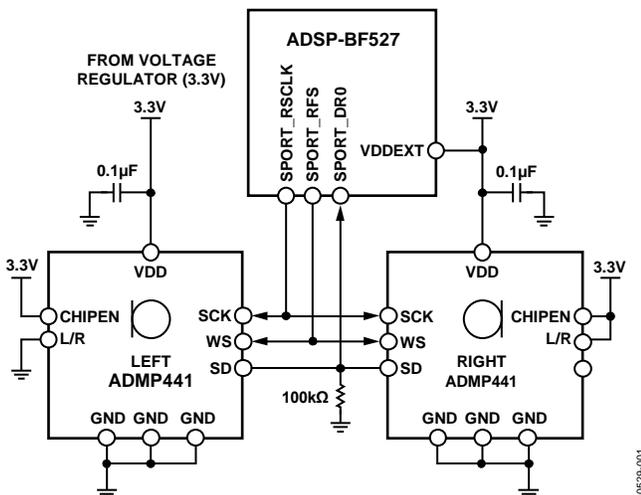


Figure 1. MEMS Microphone Connection to Blackfin DSP
(Simplified Schematic: All Connections Not Shown)

Up to two ADMP441 microphones can be input to a single data line on the ADSP-BF527 Blackfin® processor. The ADSP-BF527 can be set up with up to four serial data inputs; therefore, up to eight ADMP441 devices can connect to a single DSP.

CIRCUIT DESCRIPTION

Table 1. Devices Connected/Referenced

Product	Description
ADSP-BF527	Low power Blackfin processor with advanced peripherals
ADMP441	Omnidirectional microphone with bottom port and I ² S digital output

The ADMP441 microphones are connected to the synchronous serial port (SPORT) data input pins of the ADSP-BF527. The only necessary passive components in this circuit are a single 0.1 µF bypass capacitor for each ADMP441, and a large pull-down resistor (100 kΩ) on the SD line to discharge it while the ADMP441 output drivers are tristated. Place the bypass capacitors as close to the VDD pin (Pin 7) of the ADMP441 as possible.

Supply the VDD pin of the microphones from the same source as the 2.25 V to 3.3 V VDDEXT pin of the ADSP-BF527. Even though the ADMP441 can operate with VDD between 1.8 V and 3.3 V, VDDEXT on the ADSP-BF527 must be a minimum of 2.25 V.

There are three signals that must be connected between the ADMP441 and ADSP-BF527 for the I²S data stream: the frame clock signal, the bit clock signal, and the serial data. The ADSP-BF527 is the system clock master and generates the two I²S clocks.

This circuit demonstrates the microphones connected to a single data input on the SPORT0 input of the Blackfin. Each of the two SPORT inputs of the ADSP-BF527 has two sets of data receive pins that enable up to eight channels of I²S audio in. Table 2 shows the connections when using the serial SPORT0 input of the ADSP-BF527.

Table 2. Hardware Signal Connections

Signal	ADMP441	ADSP-BF527
Frame Clock	WS (Pin 3)	PF1/PPI_D1/RF50 (Pin PF1)
Bit Clock	SCK (Pin 1)	PF2/PPI_D2/RSCLK0 (Pin PF2)
Serial Data	SD (Pin 2)	PF0/PPI_D0/DR0PRI (Pin PF0)

Set the L/R pin on the two ADMP441 devices to opposite levels—one pulled to the VDD pin and the other to GND. When pulled to GND, the microphone outputs its data on the left channel of the I²S stream, and when pulled to VDD, it outputs its data on the right channel.

The ADMP441 is enabled by pulling the CHIPEN pin high. This pin can be tied either directly to the VDD of the microphone, which keeps it always enabled while it is powered, or it can be connected to a general-purpose input/output (GPIO) pin on the ADSP-BF527, allowing the Blackfin to enable and disable the microphone.

The ADMP441 has a sensitivity of -26 dBFS. In most applications, the microphone outputs require some gain added in the signal path of the Blackfin. If gain is added to the signal in the DSP, the output of the processor must still be limited to 0 dBFS.

ADSP-BF527 Register Settings

This section lists the SPORT register settings to set the [ADSP-BF527](#) into I²S master mode. The [ADSP-BF52x Blackfin Processor Hardware Reference](#) provides a more detailed description of these register settings.

Configure the SPORT_RCR1 register, the primary receive configuration register, with the following nondefault settings:

- RCKFE: Drive internal frame sync on falling edge of RSCLK
- RFSR: Require RFS for every data-word
- IRFS: Internal RFS used
- IRCLK: Internal receive clock select

Configure the SPORT_RCR2 register, the secondary receive configuration register, with the following nondefault settings:

- RSFSE: Receive stereo frame sync enable
- SLEN: 32-bit word length

Set the SPORT_RCLKDIV register, the SPORT receive serial clock divider register, to 17 (0x0011) and set the SPORT_RFSDIV register to 31 (0x001F). This sets the proper clock frequencies for both a 48 kHz frame clock and a 3.072 MHz bit clock, with a 120 MHz Blackfin system clock (SCLK).

The register settings described can be applied to either the SPORT0 register or the SPORT1 register on the [ADSP-BF527](#), depending on which is being used.

COMMON VARIATIONS

DSPs

This circuit can also be set up with other parts from the Blackfin family instead of an [ADSP-BF527](#). See the appropriate data sheets for details on the differences in number of SPORT channels and other variations. Consult the [Blackfin family product page](#) for more information.

Microphones

By removing one of the ADMP441 microphones, a mono microphone circuit using a single ADMP441 can be set up. The other connections remain the same in this mono configuration.

Additional ADMP441 microphones can be connected to the SPORT inputs of the [ADSP-BF527](#) in the same way as the first stereo pair.

LEARN MORE

The ADMP MEMS microphone products mentioned in this application note are manufactured by InvenSense, 1745 Technology Dr., San Jose, California 95110.

Elko, Gary W. and Kieran P. Harney. "A History of Consumer Microphones: The Electret Condenser Microphone Meets Micro-Electro-Mechanical-Systems," *Acoustics Today*, 2009.

Lewis, Jerad. AN-1112 Application Note, *Microphone Specifications Explained*. Analog Devices, Inc., 2013.

Lewis, Jerad. Technical Article MS-2275. *Common Inter-IC Digital Interfaces for Audio Data Transfer*. Analog Devices, Inc., 2012.

Nielsen, Jannik Hammel, and Claus Fürst. *Toward More Compact Digital Microphones*, Analog Dialogue Volume 41, September 2007, Analog Devices, Inc.

Data Sheets and Evaluation Boards

[ADSP-BF527 Data Sheet](#)

[ADSP-BF527 Evaluation Board \(ADZS-BF527-EZLITE\)](#)

[ADSP-BF52x Blackfin Processor Hardware Reference](#)

REVISION HISTORY

11/14—Rev. 0 to Rev. A

Changed Title of Document from CN-0266 to AN-1327	Universal
Deleted Evaluation and Design Support Section	1
Added Table 1; Renumbered Sequentially	1
Deleted Circuit Evaluation and Test Section	2
Changes to Learn More Section and Data Sheets and Evaluation Boards Section	2

1/12—Revision 0: Initial Version