

AD9142 to AD9142A Migration

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INTRODUCTION

The AD9142 and AD9142A are pin-compatible 16-bit, dual low voltage differential signaling (LVDS) high speed digital-to-analog converters (DACs). Both products have many of the same features, but the AD9142A services wider bandwidth applications compared to the AD9142 due to its higher maximum interface speed. Therefore, the AD9142A is the recommended product for new designs. For those who currently use the AD9142, consider migrating to the AD9142A. The purpose of this application note is to describe the differences between the two products and provide a guide on upgrading to the AD9142A from the AD9142. The AD9142A has additional interface features that allow the device to operate at higher interface rates (up to 575 MHz data clock input). The AD9142A also provides interface error detection features that allow the customers to debug the system interface timing more easily.

Compared to the AD9142, the AD9142A has additional feature blocks and slight pin functionality differences. The areas of the AD9142A that differ from the AD9142 are highlighted in Figure 1. The blue highlighted delay locked loop (DLL) and sample error detection (SED) blocks correspond to the interface support differences in the block diagram. The green highlighted DCIx, DACCLKx, FRAMEx/PARITYx, and REFx/SYNCx pins are areas of the device where the data sheet specifications are slightly different. The yellow highlighted data pins (D15x through D0x) and register map have additional serial port interface (SPI) software related differences. Refer to the AD9142 or AD9142A data sheet for details regarding features not addressed in this application note.

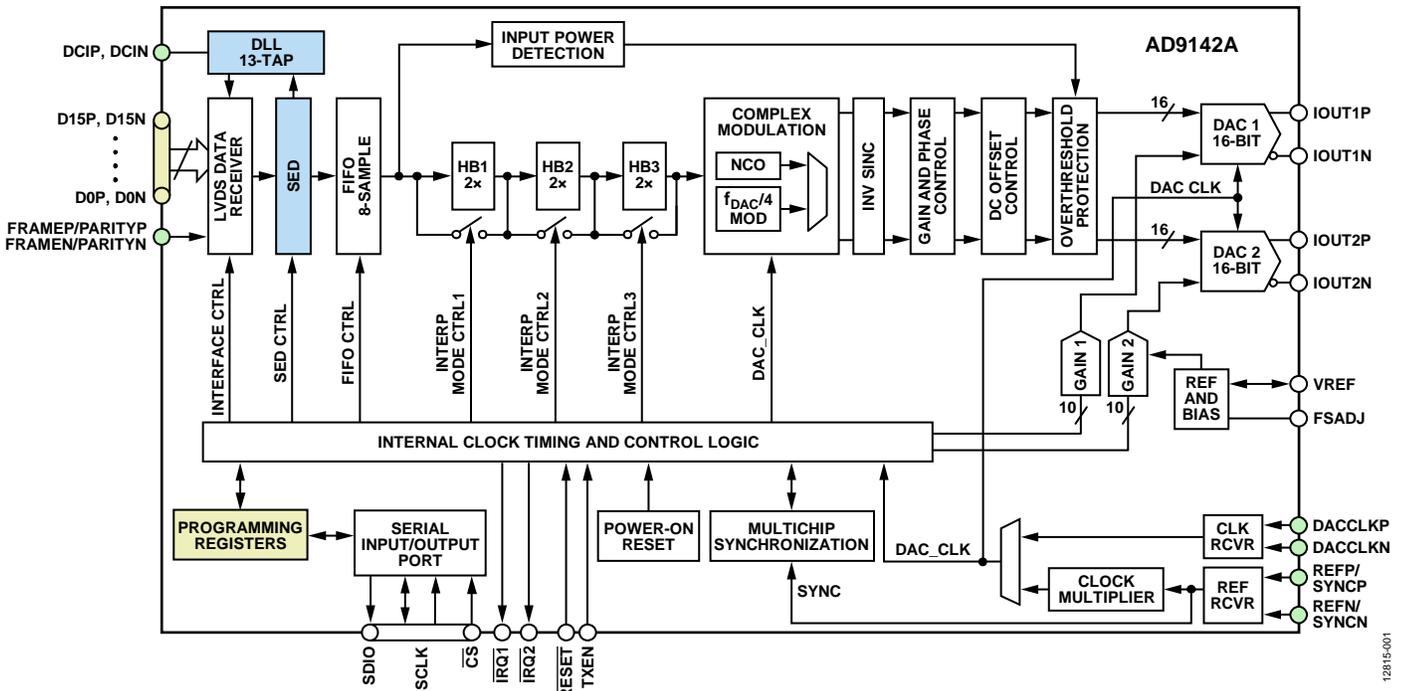


Figure 1. Block Diagram of the AD9142A

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REVISION HISTORY

1/15—Revision 0: Initial Version

PRODUCT COMPARISON OVERVIEW

The main differences between the [AD9142](#) and [AD9142A](#) are related to the data interface operation. The [AD9142](#) has a maximum of 250 MHz clock rate for the data clock input (DCIP and DCIN LVDS pin inputs). The [AD9142A](#), by contrast, has a maximum data interface rate of 575 MHz. Table 1 through Table 3 list specific feature differences between the [AD9142](#) and [AD9142A](#) products and include a brief description for each feature difference.

The Data Interface Features, Data Interface Error Checking, and Sync vs. DAC Clock Timing sections describe several of these features in more detail. The register addresses that correspond to each feature control are also included so that users can update their [AD9142](#) software for compatibility with the [AD9142A](#).

Table 1. Interface Feature Comparison

Feature	AD9142	AD9142A	Details
Interface Support	Delay line only	Delay line (bypass mode) and DLL	The delay line (bypass mode) setup and hold timing is different between the two products. When using delay line mode for the AD9142A , ensure the data clock input (DCI) signal is set to dc-coupled (SPI register setting). In addition to the delay line mode, the AD9142A includes a DLL to ease interface timing constraints, especially at high data rates. The DLL operates for DCI clock rates from 250 MHz to 575 MHz. Set the DCI to ac-coupled (SPI register setting).
Interface Error Checking Support	No features supported	Parity and SED and automatic error detection (AED)	Two types of interface error checking features are supported on the AD9142A only: SED/AED and parity. SED/AED uses a SPI-programmable pattern to check against input values that the device receives. Parity uses the frame signal as the parity bit. This feature shows errors in real time; it is not restricted to a SPI programmed repeating pattern to determine errors occurring at the interface.

Table 2. Data Sheet Specification Comparisons

Feature	AD9142	AD9142A	Details
Interface Timing	Delay line (bypass mode) interface timing specified	Delay line (bypass mode) and DLL interface timing specified	The DLL interface timing is specified in the AD9142A due to the added feature on this product. Bypass mode timing is specified on both products, but the timing is slightly shifted between the AD9142 and the AD9142A . There are also slightly different SPI programming writes required for the various delay setting options.
Sync Clock vs. DAC Clock Timing	Setup and hold times specified in data sheet	Setup and hold times specified in data sheet	The setup and hold times of the sync clock vs. the DAC clock are slightly shifted between the AD9142 and the AD9142A . The timing requirements are specified in the AD9142 and AD9142A data sheets.
Byte Mode Capabilities	Byte mode can be used with both sync on and sync off	Byte mode only works with sync off	AD9142 : Byte mode is operational when sync is off and both the SPI and frame signals can be used to reset the FIFO. However, when sync is on or when the NCO is used, only a frame FIFO request can reset the FIFO in these byte mode cases. The SPI signal cannot be used to reset the FIFO in either of these conditions in byte mode. AD9142A : Byte mode can only be used when operating with sync off and only the SPI FIFO request can be used to reset the FIFO, not the frame signal.
DCIx Pin Input Levels	DCIx levels specify a higher swing than data pins	DCIx levels specified with the same swing as data pins	The AD9142A does not require a special condition of a higher voltage swing level for the DCIx pins, DCIP (Pin 28)/DCIN (Pin 29), to operate, unlike the AD9142 .

Table 3. Additional SPI Register Comparisons

Feature	AD9142	AD9142A	Details
LVDS LSB Data Bit Power-Downs	Feature not supported	PWR_DOWN_DATA_INPUT_BITS SPI control	The AD9142A has the ability to power down the bottom 4 LSBs of the LVDS buffer to lower the resolution of the device. Use Register 0x39, Bits[3:0] to power down the corresponding data bit as desired.
Revision ID	ID = 0x05	ID = 0x0B	The version register (0x7F) indicates which revision of silicon is in the system.

DATA INTERFACE FEATURES

The [AD9142](#) interface operates at up to a 250 MHz data input clock rate. It provides a programmable delay line feature with four settings for different delay options depending on the system timing skew that needs compensation. The [AD9142A](#) has a programmable delay line feature like the [AD9142](#). It also has a DLL that allows the data interface to operate from a 250 MHz to 575 MHz data input clock rate. The timing specifications for the programmable delay line are slightly different between the [AD9142](#) and the [AD9142A](#). For those who are migrating their systems from the [AD9142](#) to the [AD9142A](#), review these timing

specifications. These timing differences and SPI delay settings are outlined in more detail in Table 5.

The DLL feature included in the [AD9142A](#) enables higher data rates and eases the interface timing constraints encountered at these higher data rates. To use this feature, program a set of registers for different controls in the feature. The DLL control bits and interrupt request (IRQ) controls related to the DLL are listed in Table 4, including the exact register addresses and some details regarding proper ways to program the device for various operation modes.

Table 4. Interface Support Details

Device	Register Addresses	Details
AD9142		
Interface IRQs	Not applicable	Not applicable.
Delay Line Enable	Register 0x5F, Bit 3	Writing a 1 to this bit enables the programmable delay line.
Programmable Delay Line Setting	Register 0x5E, Bits[7:0], Register 0x5F, Bits[2:0]	The four different delay settings are programmed through these registers using valid delay setting register values, detailed in Table 5.
Device Configuration	Register 0x79 = 0x18, Register 0x80 = 0xAD, Register 0xE1 = 0x1A	Required writes for start-up routine are needed for proper operation.
AD9142A		
Interface IRQs	IRQ enables: Register 0x04, Bits[5:4] IRQ status: Register 0x06, Bits[5:4] IRQx pin select: Register 0x08, Bits[5:4]	Interrupt enable mask bits, status bits, and IRQ output pin select bits for DLL lock and DLL warning.
Delay Line Enable/DLL Enable	Register 0x0A, Bit 7	Register location change and logic polarity change. Writing a 0 to this bit enables the straight programmable delay line (bypass mode). Writing a 1 to this bit starts the DLL state machine logic, which eases interface timing at higher input data speeds. The DLL must lock without any warnings to be stable and usable. For more information, see the AD9142A data sheet.
Programmable Delay Line Setting	Register 0x5E, Bits[7:0], Register 0x5F, Bits[2:0]	The four different delay settings are programmed through these registers using valid delay setting register values, detailed in Table 5.
Device Configuration	Using DLL: Register 0x5E = 0xFE Using delay line: Register 0x0D = 0x16	When using the DLL, turn off the LSB delay cell. When using the delay line, dc couple the DCI internally.
DLL Interface Controls	Register 0x0A to Register 0x0E	There are various interface controls for using the DLL. Follow Start-Up Sequence 1 for setting up the DLL and Start-Up Sequence 2 for setting up the delay line (bypass mode) interface. See the AD9142A data sheet for more information.

Table 5. Bypass Mode Interface Timing Support Details

Device	Delay 0	Delay 1	Delay 2	Delay 3
AD9142				
Register 0x5E, Bits[7:0]	0x00	0x07	0x7F	0xFF
Register 0x5F, Bits[2:0]	0x0	0x0	0x0	0x5
Setup Time, t_s (ns) ¹	-1.25	-1.50	-1.70	-1.93
Hold Time, t_H (ns)	2.51	2.82	3.23	3.64
$ t_s + t_H $ (ns)	1.26	1.32	1.53	1.71
AD9142A				
Register 0x5E, Bits[7:0]	0x00	0x80	0xF0	0xFE
Register 0x5F, Bits[7:0]	0x60	0x67	0x67	0x67
t_s (ns) ¹	-0.81	-0.97	-1.13	-1.28
t_H (ns)	1.96	2.20	2.53	2.79
$ t_s + t_H $ (ns)	1.15	1.23	1.40	1.51

¹ The negative sign indicates the direction of the setup time. The setup time is defined as positive when it is on the left side of the clock edge and negative when it is on the right side of the clock edge.

Example Interface Start-Up Routine Comparison

Table 6 highlights the differences between the [AD9142](#) and [AD9142A](#) in the start-up routines needed for a specific condition. Table 6 compares the different register writes needed for the delay line mode interface scheme, which is the common interface mode for both products. A similar start-up routine is described in both product data sheets.

Test Conditions

The test conditions used in the example start-up routine comparison in Table 6 are as follows:

- $f_{DCI} = f_{DATA} = 200$ MHz
- 8× interpolation
- Phase-locked loop (PLL) enabled: $f_{REF} = 200$ MHz, $f_{DAC} = 1.6$ GHz
- Voltage controlled oscillator (VCO) divider = $f_{VCO}/f_{DAC} = 1$
- Loop divider = $f_{DAC}/f_{REF} = 8$
- Inverse sinc enabled

Table 6. Example Start-Up Routine Comparison

Register Address	AD9142 Register Value	AD9142A Register Value	Description
0x00	0x20	0x20	Issue software reset
0x20	0x01	0x01	Device start-up configuration
0x79	0x18	Not applicable	AD9142 device start-up configuration only
0x80	0xAD	Not applicable	AD9142 device start-up configuration only
0xE1	0x1A	Not applicable	AD9142 device start-up configuration only
0x14	0xE7	0xE7	Configure PLL loop bandwidth and charge pump current
0x15	0xC2	0xC2	Configure VCO divider and loop divider
0x12	0xC0	0xC0	Enable PLL
0x12	0x80	0x80	Enable PLL autosearch mode, verify PLL is locked if Register 0x16, Bit 7 = 1
0x5E	0x00	0x00	Configure delay line interface delay setting of 0
0x5F	0x08	0x60	AD9142 : enable delay line and delay setting of 0; AD9142A : delay setting of 0
0x0D	Not applicable	0x16	DC couple DCI on the AD9142A only
0x0A	Not applicable	0x00	Turn off DLL and duty cycle correction on the AD9142A only
0x28	0x03	0x03	8× interpolation
0x25	0x01	0x01	Reset FIFO, Register 0x24 reads back one of the three values: 0x37, 0x40, 0x41
0x27	0x80	0x80	Enable inverse sinc
0x01	0x00	0x00	Power up DAC outputs

DATA INTERFACE ERROR CHECKING

A significant advantage of the [AD9142A](#) is that it provides data interface error checking capabilities. The [AD9142A](#) has SED/AED functions, in addition to parity checking functionality, to determine whether any errors are received on the interface.

These functions allow users to troubleshoot their data interface and verify that the timing constraints are met properly in their systems.

There are multiple controls available for users to program and specify the test conditions for these error checking features. The control bits and IRQ controls related to both SED/AED and parity are detailed in Table 7 and include the exact register address locations for each of the controls along with details regarding proper configuration of the feature options. For more information on the full functionality and programmability of each feature, refer to the [AD9142A](#) data sheet.

Table 7. Interface Error Checking Support Details

Device	Register Addresses	Details
AD9142 No Features Supported	Not applicable	Not applicable.
AD9142A Feature IRQs	IRQ enables: Register 0x04, Bit 7 for parity, Bit 6 for SED IRQ status: Register 0x06, Bit 7 for parity, Bit 6 for SED IRQx pin select: Register 0x08, Bit 7 for parity, Bit 6 for SED	Interrupt enable mask bits, status bits, and IRQ output pin select bits for parity and SED failures.
Frame Signal Usage	Register 0x09, Bit 5: set high when using parity Register 0x09, Bit 4: set high when using SED or normal frame operation (when needed) Register 0x09, Bits[1:0]: set to 1 for parity, 2 for SED or normal frame operation	A frame signal is required when running parity or when using a word depth of four for SED or AED. Certain other normal operating modes may require a frame signal, such as using byte mode interface or multichip synchronization schemes. Depending on the mode of operation, this register must be set appropriately for the type of frame signal needed.
SED/AED	Control bits and status flags: Register 0x60 SED/AED pattern values: Register 0x61 to Register 0x68	The control bits allow the user to program the SED/AED depth, select between SED and AED operation, clear any error flags, and enable the SED/AED comparison. The pattern sent to the device is programmed in the pattern value registers for the device to compare the bits actually received and raise any error flags in the status flag bits as well as the IRQ bits. For more information, see the AD9142A data sheet.
Parity	Control bits and status flags: Register 0x6A Error counters: Register 0x6B to Register 0x6C	The control bits allow the user to select between even and odd parity, clear any error flags, and enable the parity operation. If any errors occur on either the rising or falling edges of the clock, the error counters increment appropriately and raise corresponding error flags in the status flag bits as well as the IRQ bits. For more information, see the AD9142A data sheet.

SYNC vs. DAC CLOCK TIMING

In addition to the interface timing differences, there is a slight sync clock to DAC clock t_S and t_H shift between the [AD9142](#) and [AD9142A](#). The details of this shift are shown in Table 8. The timing details are included in each product data sheet. If using the multichip sync function on the [AD9142](#), note these slight timing differences to adjust user systems accordingly when migrating from the [AD9142](#) to the [AD9142A](#).

Table 8. Sync Clock and DAC Clock Timing Support Details

Falling Edge Sync Timing (default)	AD9142 Max (ps)	AD9142A Max (ps)
t_S (ns)	246	324
t_H (ns)	-11	-92
$ t_S + t_H $ (ns)	235	232