REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. - rrp	02-01-11	R. Monnin
B	Redrawn. Paragraphs updated to MIL-PRF-38535 requirements. - drw	13-11-14	Charles F. Saffle

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			B	B	B	B	B	B	B	B	B	B	B	B	B	
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

PREPARED BY
Sandra Rooney

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Sandra Rooney

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
94-06-22

REVISION LEVEL
B

MICROCIRCUIT, LINEAR, 16-BIT SERIAL/BYTE D/A CONVERTER, MONOLITHIC SILICON

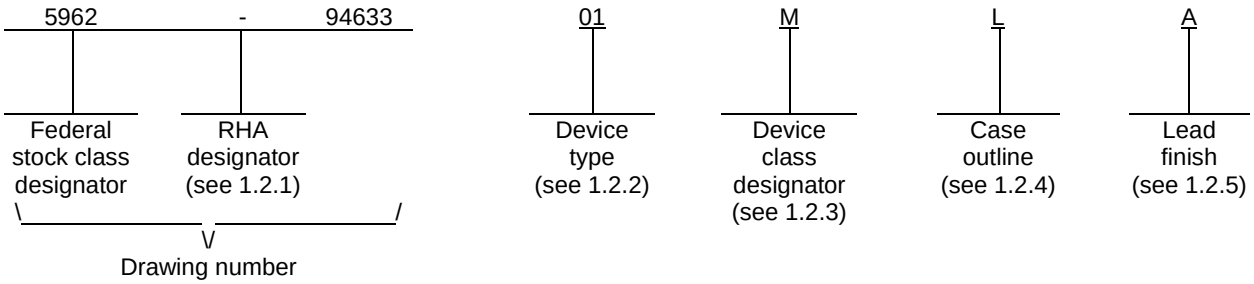
SIZE	CAGE CODE	
A	**67268**	**5962-94633**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	AD660S	16-bit serial/byte DACPORT

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

V_{LL} to DGND	-0.3 V to +7 V dc
V_{CC} to AGND	-0.3 V to +17.0 V dc
V_{EE} to AGND	+0.3 V to -17.0 V dc
AGND to DGND	±1 V
Digital inputs (Pins 5-12 and 14-19) to DGND	-1.0 V to +7.0 V dc
REF IN to AGND	±10.5 V
Span/Bipolar Offset to AGND	±10.5 V
REF OUT, V_{OUT}	Indefinite short to AGND, DGND, V_{CC}, V_{EE}, and V_{LL}
Power dissipation (P_D) at T_A = 60°C 2/	1000 mW
Storage temperature	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA})	80°C/W

1.4 Recommended operating conditions.

V_{LL} max	+5 V dc
V_{CC}/V_{EE}	±15 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Derate linearly above T_A = +60°C at 8.7 mW/°C.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 56 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V V_{LL} = +5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES	2/	1	01	16		Bits
Relative accuracy	RA		1	01		±2	LSB
			2, 3			±4	
Differential nonlinearity	DNL	Major carry errors	1	01		±2	LSB
			2, 3			±4	
Gain error	A_E	All bits on 3/, 4/	1	01		±0.1	% of FSR
Gain drift	TCA_E	All bits on 3/	2, 3	01		±25	ppm/°C
Unipolar offset error	V_{OS}	All bits off	1	01		±2.5	mV
Unipolar offset tempco	TCV_{OS}	All bits off	2, 3	01		3	ppm/°C
Bipolar zero error	B_{PZE}	MSB on, all others off	1	01		±7.5	mV
Bipolar zero tempco	TCB_{PZE}	MSB on, all others off	2, 3	01		5	ppm/°C
Reference output voltage	V_{REF}		1	01	9.99	10.01	V
Reference output drift	TCV_{REF}		2, 3	01		25	ppm/°C
Reference output external current	IV_{REF}	2/, 5/	1	01	2		mA
Reference output capacitive load	CLV_{REF}	2/	1	01		1000	pF
Reference input resistance	R_{IN}	2/	1	01	7	13	kΩ
Bipolar offset input resistance	$R_{IN}BPO$	2/	1	01	7	13	kΩ
Output voltage range	V_{OUT}	Unipolar range 2/	1	01		+10	V
		Bipolar range 2/				±10	
Output current	I_{OUT}	2/	1	01	5		mA
Capacitive load	C_L	2/	1	01		1000	pF
Output voltage settling time	t_{SL}	20 V step, T_A = +25°C 2/	9	01		13	µs
Digital input high voltage	V_{IH}		1, 2, 3	01	2		V
Digital input low voltage	V_{IL}		1, 2, 3	01		0.8	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V V_{LL} = +5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital input high current	I_{IH}	V_{IH} = +5.5 V	1, 2, 3	01		±10	µA
Digital input low current	I_{IL}	V_{IL} = 0 V	1, 2, 3	01		±10	µA
Power supply current	I_{LL}	V_{IH} = +5.5 V, V_{IL} = 0 V	1	01		2	mA
		V_{IH} = +2.4 V, V_{IL} = 0.4 V				7.5	
	I_{CC}					18	
	I_{EE}					-18	
Power supply rejection ratio	PSRR	+14.25 V ≤ V_{CC} ≤ +15.75 V	1	01		±2	ppm/%
		-14.25 V ≤ V_{EE} ≤ -15.75 V				±2	
		+4.5 V ≤ V_{LL} ≤ +5.5 V				±2	
Total harmonic distortion & noise	THD+N	0 dB, 990.5 Hz; Sample rate = 96 kHz	1	01		0.009	%
		-20 dB, 990.5 Hz; Sample rate = 96 kHz				0.056	
		-60 dB, 990.5 Hz; Sample rate = 96 kHz				5.6	
Signal-to-noise ratio	SNR		1	01	83		dB
Chip select	$t_{\overline{CS}}$	See figure 2A, 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	40		ns
			10, 11		50		
Data set-up	t_{DS}	See figure 2A, 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	40		ns
			10, 11		50		
Data hold	t_{DH}	See figure 2A, 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	0		ns
			10, 11		10		
Byte enable set-up	t_{BES}	See figure 2A, 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	40		ns
			10, 11		50		
Byte enable hold	t_{BEH}	See figure 2A, 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	0		ns
			10, 11		10		
LDAC hold	t_{LH}	See figure 2A, 2B 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	80		ns
			10, 11		100		
LDAC width	t_{LW}	See figure 2A, 2B 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	40		ns
			10, 11		50		
Serial clock	t_{CLK}	See figure 2B, 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	80		ns
			10, 11		100		
Serial clock low	t_{LO}	See figure 2B, 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	30		ns
			10, 11		50		

See footnotes at end of table.

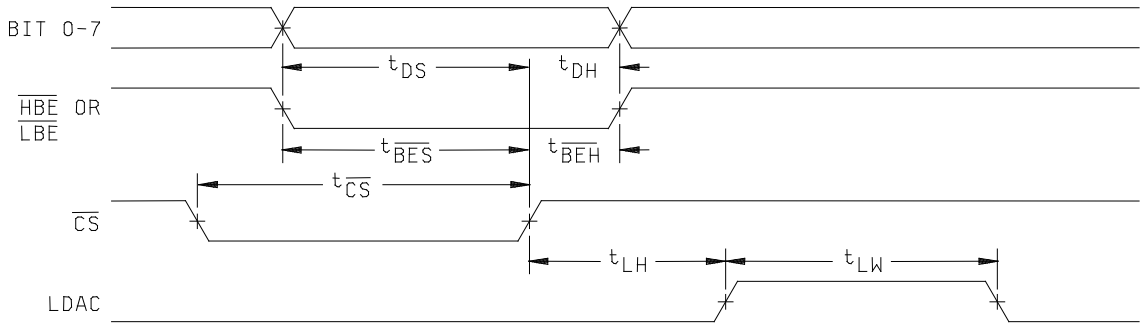
TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V V_{LL} = +5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Serial clock high	t_{HI}	See figure 2B 2/, V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	30		ns
			10, 11		50		
Serial set-up	t_{SS}	See figure 2B 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	0		ns
			10, 11		10		
Serial hold	t_{SH}	See figure 2B 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	0		ns
			10, 11		10		
Data set-up	t_{DS}	See figure 2B 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	40		ns
			10, 11		50		
Data hold	t_{DH}	See figure 2B 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	0		ns
			10, 11		10		
Clear width	$t_{\overline{CLR}}$	See figure 2C 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	80		ns
			10, 11		110		
Clear set-up time	t_{SET}	See figure 2C 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	80		ns
			10, 11		110		
Clear hold time	t_{HOLD}	See figure 2C 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	0		ns
			10, 11		10		
Serial out propagation delay time	t_{PROP}	See figure 2D 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	50		ns
			10, 11		100		
Data set-up	t_{DS}	See figure 2D 2/ V_{IH} = 2.4 V, V_{IL} = 0.4 V	9	01	50		ns

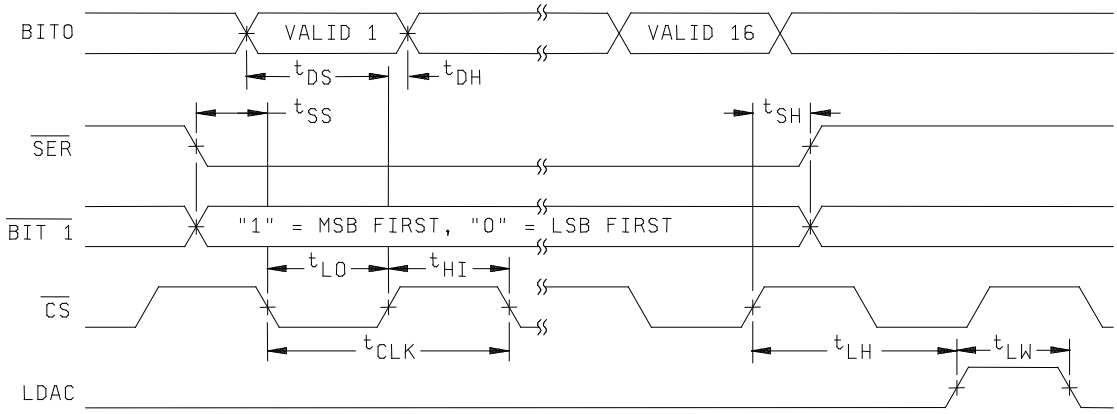
1/ For 16-bit resolution, 1 LSB = 0.0015% or FSR = 15 ppm of FSR. For 15-bit resolution, 1 LSB = 0.003% of FSR = 30 ppm of RSR. For 14-bit resolution, 1 LSB = 0.006% of FSR = 60 ppm of FSR. FSR stands for Full-Scale Range and is 10 V in unipolar mode and 20 V in bipolar mode.
2/ Guaranteed if not tested.
3/ Gain error and gain drift are measured using the internal reference.
4/ Measured with fixed 50 Ω resistors. Eliminating these resistors increases the gain error by 0.25% of FSR (Unipolar mode) or 0.50% of FSR (Bipolar mode).
5/ External current is defined as the current available in addition to that supplied to REF IN and SPAN/BIPOLAR OFFSET.

Device type	01
Case outline	L
Terminal number	Terminal symbol
1	$-V_{EE}$
2	$+V_{CC}$
3	$+V_{LL}$
4	DGND
5	DB7,15
6	DB6,14
7	DB5,13
8	DB4,12
9	DB3,11
10	DB2,10
11	DB1,9,MSB/$\overline{\text{LSB}}$
12	DB0,8,S_{IN}
13	S_{OUT}
14	$\overline{\text{CS}}$
15	$\overline{\text{LBE}}$, $\overline{\text{UNI}}$/BIP,CLR
16	$\overline{\text{HBE}}$
17	$\overline{\text{SER}}$
18	$\overline{\text{CLR}}$
19	LDAC
20	AGND
21	V_{OUT}
22	SPAN, BIPOLAR OFFSET
23	REF IN
24	REF OUT

FIGURE 1. Terminal connections.

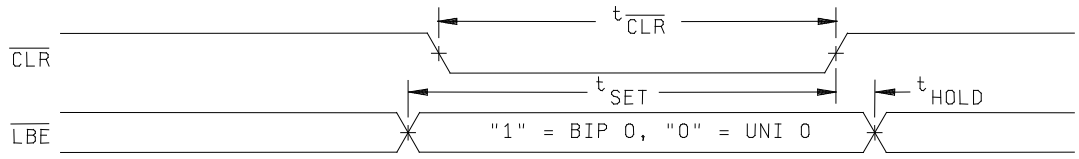


2A. BYTE LOAD TIMING

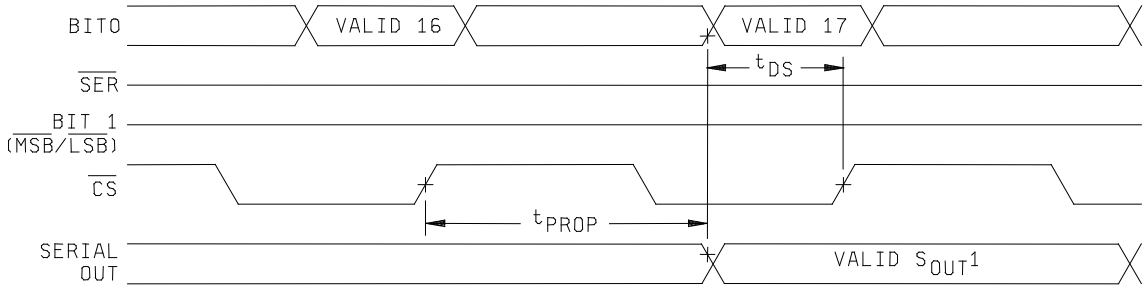


2B. SERIAL LOAD TIMING

FIGURE 2. Timing waveforms.



2C. ASYNCHRONOUS CLEAR TO BIPOLAR OF UNIPOLAR ZERO



2D. SERIAL OUT TIMING

FIGURE 2. Timing waveforms - continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 9, 10, 11 1/, 2/	1, 2, 3, 9, 10, 11 1/, 2/	1, 2, 3, 9, 10, 11 1/, 2/
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11 2/	1, 2, 3, 9, 10, 11 2/	1, 2, 3, 9, 10, 11 2/
Group C end-point electrical parameters (see 4.4)	1	1	1, 2, 3, 9, 10, 11 2/
Group D end-point electrical parameters (see 4.4)	1	1	1, 2, 3
Group E end-point electrical parameters (see 4.4)	- - -	- - -	- - -

1/ PDA applies to subgroup 1.
2/ Subgroups 9, 10, and 11 guaranteed if not tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-11-14

Approved sources of supply for SMD 5962-94633 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9463301MLA	24355	AD660SQ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices RT 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: 804 Woburn Street Wilmington, MA 01887-3462