

	REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED	

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	PREPARED BY RICK OFFICER		DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 <a href="http://www.landandmaritime.dla.mil/">http://www.landandmaritime.dla.mil/</a>	
Original date of drawing YY-MM-DD  13-06-17	CHECKED BY RAJESH PITHADIA		TITLE  MICROCIRCUIT, DIGITAL-LINEAR, CMOS, 8-BIT, BUFFERED MULTIPLYING DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON	
	APPROVED BY CHARLES F. SAFFLE			
	SIZE  A	CODE IDENT. NO.  16236	DWG NO.  V62/12659	
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## 1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance CMOS, 8 bit, buffered multiplying digital to analog converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/12659</u>	-	<u>01</u>	<u>X</u>	<u>B</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

### 1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	AD7524	CMOS, 8 bit, buffered multiplying digital to analog converter

### 1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	MS-012-AC	Plastic small outline package

### 1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{DD}$ ) to ground (GND) .....	-0.3 V to +17 V
DAC feedback resistor ( $V_{RFEEDBACK}$ ) to GND .....	$\pm 25$ V
DAC reference voltage input ( $V_{REF}$ ) to GND .....	$\pm 25$ V
Digital input voltage to GND .....	-0.3 V to $V_{DD} + 0.3$ V
DAC current output (OUT1), DAC analog ground (OUT2) to GND .....	-0.3 V to $V_{DD} + 0.3$ V
Power dissipation (PD) :	
To 75°C .....	450 mW
Derates above 75°C by .....	6 mW/°C
Storage temperature range ( $T_{STG}$ ) .....	-65°C to +150°C
Lead temperature (soldering, 10 seconds) .....	300°C

1.4 Recommended operating conditions. 2/

Operating free-air temperature range ( $T_A$ ) .....	-55°C to +125°C
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1.5 Thermal characteristics.

Thermal resistance, junction to case ( $\theta_{JC}$ ) .....	43°C/W (Non-standard 4 layer board)
Thermal resistance, junction to ambient ( $\theta_{JA}$ ) .....	81°C/W (Non-standard 4 layer board)

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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## 2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <http://www.jedec.org>)

## 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Timing waveforms. The timing waveforms shall be as shown in figure 3.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions VREF = 10 V, VOUT1 = VOUT2 = 0 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Static performance.							
Resolution		VDD = 5 V and 15 V	25°C	01	8		Bits
			-55°C to +125°C		8		
Relative accuracy		VDD = 5 V and 15 V	25°C	01		±1/2	LSB
			-55°C to +125°C			±1/2	
Monotonicity				01	Guaranteed		
Gain error 2/	AE	VDD = 5 V	25°C	01		±2 1/2	LSB
		VDD = 15 V				±1 1/4	
		VDD = 5 V	-55°C to +125°C			±3 1/2	
		VDD = 15 V				±1 1/2	
Average gain 3/ temperature coefficient  (Measured from 25°C to -55°C or from 25°C to +125°C)		VDD = 5 V	25°C	01	±40		ppm/ °C
		VDD = 15 V			±10		
		VDD = 5 V	-55°C to +125°C		±40		
		VDD = 15 V			±10		
DC supply rejection 3/	ΔGain/  ΔVDD	VDD = 5 V, ΔVDD = ±10%	25°C	01		0.08	%FSR/  %max
					0.002 typical		
		VDD = 15 V, ΔVDD = ±10%			0.02		
			0.001 typical				
		VDD = 5 V, ΔVDD = ±10%	-55°C to +125°C			0.16	
					0.01 typical		
		VDD = 15 V, ΔVDD = ±10%			0.04		
			0.005 typical				

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions VREF = 10 V, VOUT1 = VOUT2 = 0 V, unless otherwise specified		Temperature, TA	Device type	Limits		Unit
						Min	Max	
Static performance – continued.								
Output leakage current, pin 1	IOUT1	DB0 to DB7 = 0 V, WR, CS = 0 V, VREF = ±10 V	VDD = 5 V	25°C	01		±50	nA
			VDD = 15 V				±50	
			VDD = 5 V	-55°C to +125°C			±400	
			VDD = 15 V				±200	
Output leakage current, pin 2	IOUT2	DB0 to DB7 = VDD, WR, CS = 0 V, VREF = ±10 V	VDD = 5 V	25°C	01		±50	nA
			VDD = 15 V				±50	
			VDD = 5 V	-55°C to +125°C			±400	
			VDD = 15 V				±200	
Dynamic performance.								
Output current 3/ settling time (to 1/2 LSB)		OUT1 load = 100 Ω, CEXT = 13 pF, WR, CS = 0 V, DB0 to DB7 = 0 V to VDD to 0 V,	VDD = 5 V	25°C	01		400	ns
			VDD = 15 V				250	
			VDD = 5 V	-55°C to +125°C			500	
			VDD = 15 V				350	
AC feedthrough at 3/ at OUT1		VREF = ±10 V, 100 kHz sine wave, DB0 to DB7 = 0 V, WR, CS = 0 V,	VDD = 5 V	25°C	01		0.25	%FSR
			VDD = 15 V				0.25	
			VDD = 5 V	-55°C to +125°C			0.5	
			VDD = 15 V				0.5	
AC feedthrough at 3/ at OUT2		VREF = ±10 V, 100 kHz sine wave, DB0 to DB7 = 0 V, WR, CS = 0 V,	VDD = 5 V	25°C	01		0.25	%FSR
			VDD = 15 V				0.25	
			VDD = 5 V	-55°C to +125°C			0.5	
			VDD = 15 V				0.5	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions VREF = 10 V, VOUT1 = VOUT2 = 0 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Reference input.							
Reference input 4/  (VREF pin to GND)	RIN	VDD = 5 V and 15 V	25°C	01	5	20	kΩ
			-55°C to +125°C		5	20	
Analog outputs.							
Output capacitance 3/  							

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V <sub>REF</sub> = 10 V, V <sub>OUT1</sub> = V <sub>OUT2</sub> = 0 V, unless otherwise specified		Temperature, T <sub>A</sub>	Device type	Limits		Unit
						Min	Max	
Digital inputs - continued.								
Input current	I <sub>IN</sub>	V <sub>DD</sub> = 5 V, V <sub>IN</sub> = 0 V or V <sub>DD</sub>	25°C	01		±1	μA	
		V <sub>DD</sub> = 15 V, V <sub>IN</sub> = 0 V or V <sub>DD</sub>				±1		
		V <sub>DD</sub> = 5 V, V <sub>IN</sub> = 0 V or V <sub>DD</sub>	-55°C to +125°C			±10		
		V <sub>DD</sub> = 15 V, V <sub>IN</sub> = 0 V or V <sub>DD</sub>				±10		
Input capacitance <u>3/</u>	C <sub>IN</sub>	V <sub>DD</sub> = 5 V and 15 V, V <sub>IN</sub> = 0 V, DB0 to DB7	25°C	01		5	pF	
			-55°C to +125°C			5		
		V <sub>DD</sub> = 5 V and 15 V, V <sub>IN</sub> = 0 V, $\overline{\text{WR}}$ , $\overline{\text{CS}}$	25°C			20		
			-55°C to +125°C			20		
Switching characteristics.		See figure 3.						
Chip select to write <u>5/</u> setup time	t <sub>CS</sub>	t <sub>WR</sub> = t <sub>CS</sub>	V <sub>DD</sub> = 5 V	25°C	01	170		ns
			V <sub>DD</sub> = 15 V			100		
			V <sub>DD</sub> = 5 V	-55°C to +125°C		240		
			V <sub>DD</sub> = 15 V			150		
Chip select to write hold time	t <sub>CH</sub>	V <sub>DD</sub> = 5 V and 15 V	25°C	01	0		ns	
			-55°C to +125°C		0			
Write pulse width	t <sub>WR</sub>	t <sub>CS</sub> ≥ t <sub>WR</sub> ,  t <sub>CH</sub> ≥ 0	V <sub>DD</sub> = 5 V	25°C	01	170		ns
			V <sub>DD</sub> = 15 V			100		
			V <sub>DD</sub> = 5 V	-55°C to +125°C		240		
			V <sub>DD</sub> = 15 V			150		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions VREF = 10 V, VOUT1 = VOUT2 = 0 V, unless otherwise specified		Temperature, TA	Device type	Limits		Unit
						Min	Max	
Switching characteristics - continued. See figure 3								
Data setup time	tDS	VDD = 5 V	25°C	01	135		ns	
		VDD = 15 V			60			
		VDD = 5 V	-55°C to +125°C		170			
		VDD = 15 V			100			
Data hold time	tDH	VDD = 5 V and 15 V	25°C	01	10		ns	
			-55°C to +125°C		10			
Power supply								
Power supply current	IDD	All digital inputs  VIL or VIH	VDD = 5 V	25°C	01		1	mA
			VDD = 15 V			2		
			VDD = 5 V	-55°C to +125°C			2	
			VDD = 15 V				2	
		All digital inputs  0 V or VDD	VDD = 5 V	25°C			100	µA
			VDD = 15 V			100		
			VDD = 5 V	-55°C to +125°C			500	
			VDD = 15 V				500	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Gain error is measured using internal feedback resistor. Full scale range (FSR) =  $V_{REF}$ .

3/ Guaranteed not tested.

4/ DAC thin film resistor temperature coefficient is approximately  $-300\text{ ppm}/^\circ\text{C}$ .

5/ AC parameter, sample tested at  $25^\circ\text{C}$  to ensure conformance to specification.

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Case X

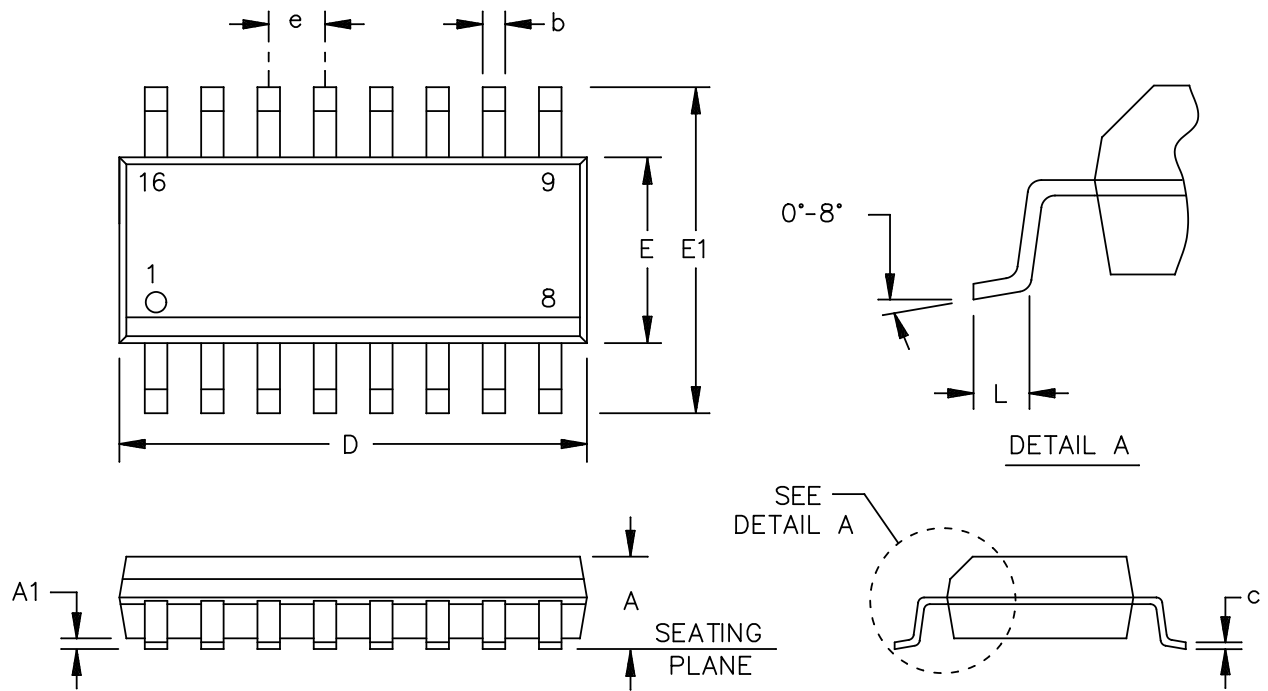


FIGURE 1. Case outline.

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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.0531	0.0689	1.35	1.75
A1	0.0039	0.0098	0.10	0.25
b	0.0122	0.0201	0.31	0.51
c	0.0067	0.0098	0.17	0.25
D	0.3858	0.3937	9.80	10.00
E	0.1496	0.1575	3.80	4.00
E1	0.2283	0.2441	5.80	6.20
e	0.0500 BSC		1.27 BSC	
L	0.0157	0.0500	0.40	1.27

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MS-012-AC.

FIGURE 1. Case outline - Continued.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	OUT1
2	OUT2
3	GND
4	DB7 (MSB)
5	DB6
6	DB5
7	DB4
8	DB3
9	DB2
10	DB1
11	DB0 (LSB)
12	$\overline{CS}$
13	$\overline{WR}$
14	V <sub>DD</sub>
15	V <sub>REF</sub>
16	R <sub>FEEDBACK</sub>

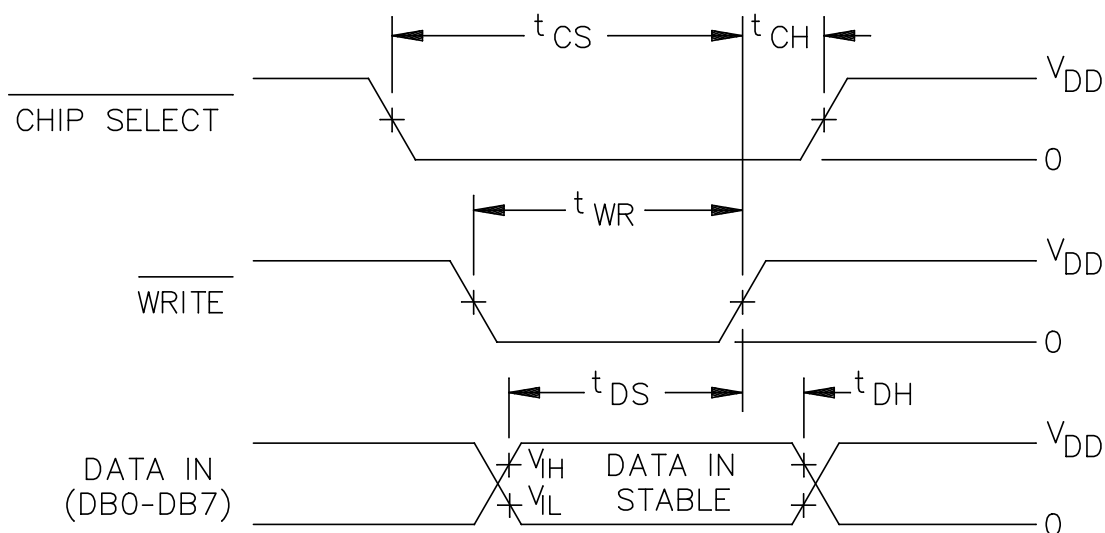
FIGURE 2. Terminal connections.

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Terminal symbol	Description
OUT1	DAC current output.
OUT2	DAC analog ground. This pin should normally be tied to the analog ground of the system.
GND	Ground.
DB7 (MSB) to DB0 (LSB)	Parallel data bit 7 to data bit 0.
$\overline{\text{CS}}$	Chip select input. Active low. Used in conjunction with $\overline{\text{WR}}$ to load parallel data to the input latch.
$\overline{\text{WR}}$	Write. When low, use in conjunction with $\overline{\text{CS}}$ to load parallel data.
V <sub>DD</sub>	Positive power supply input. These parts can be operated with a supply of 5 V.
V <sub>REF</sub>	DAC reference voltage input terminal.
R <sub>FEEDBACK</sub>	DAC feedback resistor pin. Establish voltage output of the DAC by connecting to external amplifier output.

FIGURE 2. Terminal connections - continued.

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NOTES:

1. All input signal rise and fall times measured from 10% to 90% of  $V_{DD}$ .  
 $V_{DD} = 5\text{ V}$ ,  $t_R = t_F = 20\text{ ns}$ ;  $V_{DD} = 15\text{ V}$ ,  $t_R = t_F = 40\text{ ns}$ .
2. Timing measurement reference level is  $(V_{IH} + V_{IL}) / 2$ .
3.  $t_{DS} + t_{DH}$  is approximately constant at 145 ns minimum at 25°C,  $V_{DD} = 5\text{ V}$  and  $t_{WR} = 170\text{ ns}$  minimum.  
The device is specified for a minimum  $t_{DH}$  of 10 ns. However, in applications where  $t_{DH} > 10\text{ ns}$ ,  $t_{DS}$  may be reduced accordingly up to the limit  $t_{DS} = 65\text{ ns}$ ,  $t_{DH} = 80\text{ ns}$ .

FIGURE 3. Timing waveforms.

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#### 4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

#### 5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

#### 6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/12659-01XB	24355	AD7524SRZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

#### CAGE code

24355

#### Source of supply

Analog Devices  
Route 1 Industrial Park  
P.O. Box 9106  
Norwood, MA 02062  
Point of contact: Raheen Business Park  
Limerick, Ireland

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