Application Report
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How to Achieve Power-Path Management Function for bq2408x

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ABSTRACT

This application report presents a simple external circuit for achieving a power-path management function while maintaining an overvoltage protection function and blocking reverse current for low-cost linear battery chargers such as the bq2408x . Brief design criteria and a trade-off study with test results are presented.

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1 Introduction

Feature-rich portable devices require operating the system while simultaneously charging the deeply discharged battery. The dynamic power-path management (PPM) battery chargers such as the bq2403x and the bq2407x can achieve such unique function with integrated MOSFETs for the smallest size solution. For consumer electronic devices, the low-cost solution is desirable. Many existing low-cost, single-cell linear chargers do not provide a PPM function. How does the designer achieve the PPM function while minimizing the system solution cost with existing low-cost linear battery chargers? This application report introduces a simple low-cost external circuit for achieving a PPM function while keeping the input overvoltage protection (OVP). The power-path MOSFET between the adapter input and the output is controlled by the power-good indicator ($\overline{PG}$) pin of bq24085/6/8 chargers, which are highly integrated Li-ion and Li-polymer linear chargers. In the following section, a simple external PPM circuit is introduced with OVP function and nonreverse battery leaking current from the battery to the input.

2 Simple PPM Circuit for bq2408x

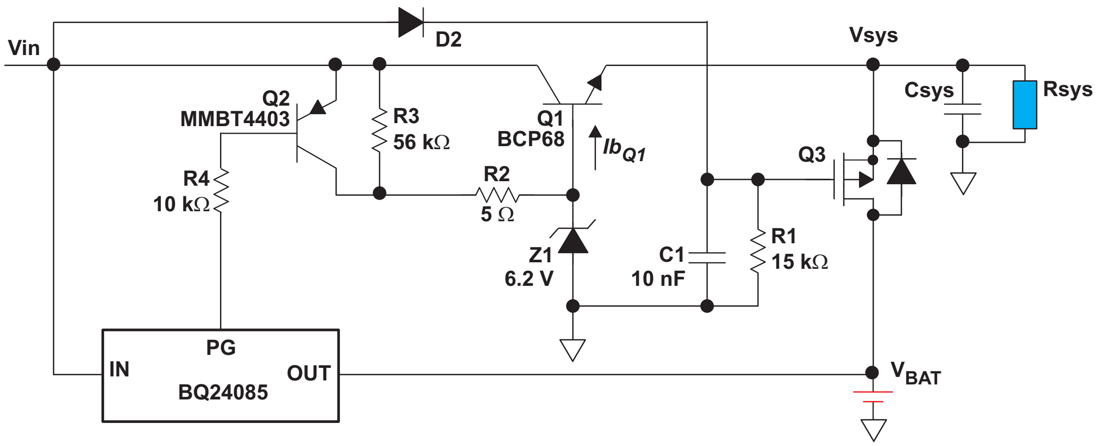


Figure 1. Power-Path Management Circuit With bq24085

Figure 1 shows a low-cost external PPM solution. The bipolar transistor Q1 is used to power the system, whereas the bq24085 is used to charge the battery independently. The MOSFET Q3 is turned on to power the system when the input power source Vin is removed. Because transistor Q1 has no body-diode across it, no battery leakage current occurs from the battery to the input during the battery removal. When the input voltage is within normal operating range, the $\overline{PG}$ pin pulls low and turns on Q2 after a 2.5-ms deglitch period. The current flowing through Q1 and R2 is partially used as the base current to drive the bipolar transistor Q1, which delivers the input power to the system. When the input voltage is below the overvoltage threshold (the overvoltage set point of bq24085 is 6.5 V), Q1 and Z1 regulate the system voltage at approximately Zener breakdown voltage minus 0.7 V, and the Q1 operates in linear regulation mode. When the input voltage is higher than the input OVP set point of the bq24085, the $\overline{PG}$ pin signal is actively high and immediately turns off Q2, which turns off Q1 for achieving input OVP function.

The gate drive of P-MOSFET Q3 consists of a diode D2, a resistor R1, and a capacitor C1 connected to ground. When the input voltage is available, the Q3 gate voltage is almost equal to the input voltage, which turns off Q3, so that the system is powered by the input power source. When the input power source is removed, the Q3 gate voltage is low and Q3 is turned on, so that the battery provides the power to the system.

In the circuit of Figure 1, a simple low-cost NPN transistor Q1 and diode Z1 regulate the output voltage. Q1 also can block reverse current. The collector-emitter voltage (Vce) drop of Q1 is a critical parameter for Q1's power dissipation and system load regulation. The following discussion describes the power dissipation across Q1 under three different operation modes.

1. Input voltage is higher than bq24085 UVLO threshold, but lower than Z1 clamp voltage.

   $Vce_{Q1} = Vbe_{Q1} + Ib_{Q1} \times R2 + Vce_{Q2}$

   Collector-emitter saturation voltage of Q2, Vce_{Q2}, can be found in the data sheet. System voltage is lower than input voltage by about Vce_{Q1}.

   For example: system load current of I_{sys} is 800 mA. Base-emitter voltage drop is 0.7 V. DC current gain β of Q1 is 100. Ib_{Q1} = 800 mA/100 = 8 mA; Vce_{Q2} is about 40 mV on MMBT4403 data sheet. So, the voltage drop across Q1 is given by

   $$Vce_{Q1} = 0.7 + 0.008 \times 5 + 0.04 = 0.78 \text{ (V)}$$

   Power dissipation of Q1 is given by

   $$Pd_{Q1} = Vce_{Q1} \times I_{sys} = 0.544 \text{ (W)}.$$

2. Input voltage is higher than Zener clamp voltage and lower than the input overvoltage set point of bq24085.

   In this condition, the base voltage of Q1 is clamped by Zener diode Z1. The Q1 operates in linear region, and its voltage drop is given by

   $$Vce_{Q1} = V_{in} – V_z + Vbe_{Q1}$$

   For = V_z = 6.2 V. IV_{in} = 6.5 V, I_{sys} = 800 mA, and Vbe_{Q1} = 0.7 V, then Vce_{Q1} = 1 V.

Power dissipation of Q1: $Pd_{Q1} = Vce_{Q1} \times I_{sys} = 0.8$ (W).

According to this analysis, Zener breaking voltage must be chosen close to OVP set point for reducing Q1 and Zener's power dissipation.

3. Input voltage is higher than input overvoltage or lower than UVLO set point.

   Under this condition, Q2 is off because $\overline{PG}$ is high output impedance. The base current of Q1 is very small, which keeps Q1 off and maintains OVP function as the bq24085 does.

3 Test Results of PPM Circuit With bq24085

1. Output voltage regulation under different loads

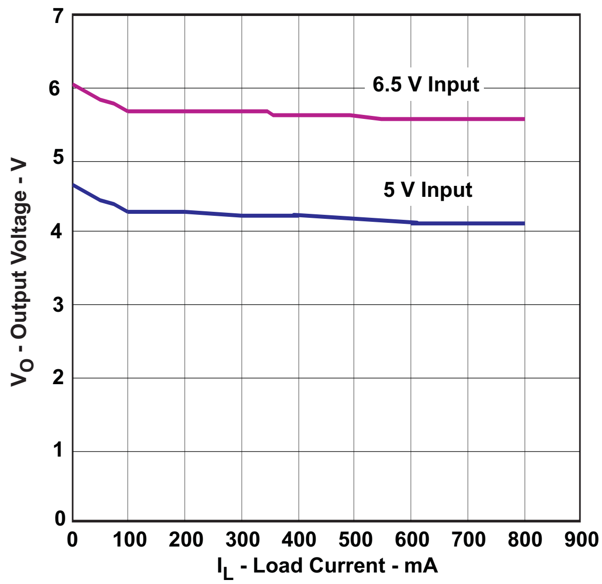
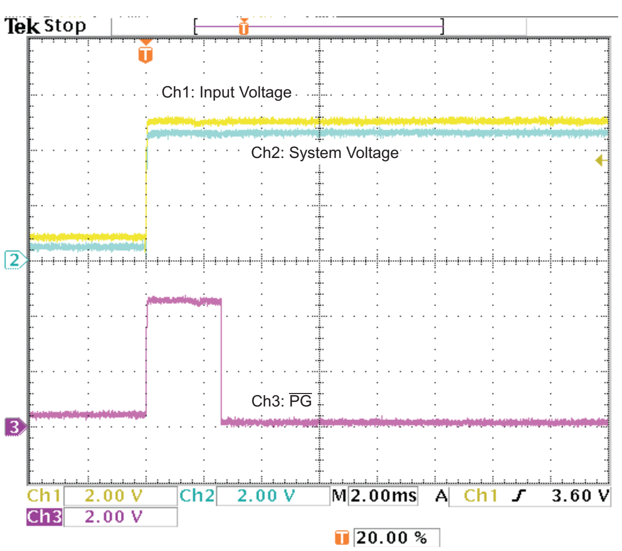


Figure 2. Load Regulation

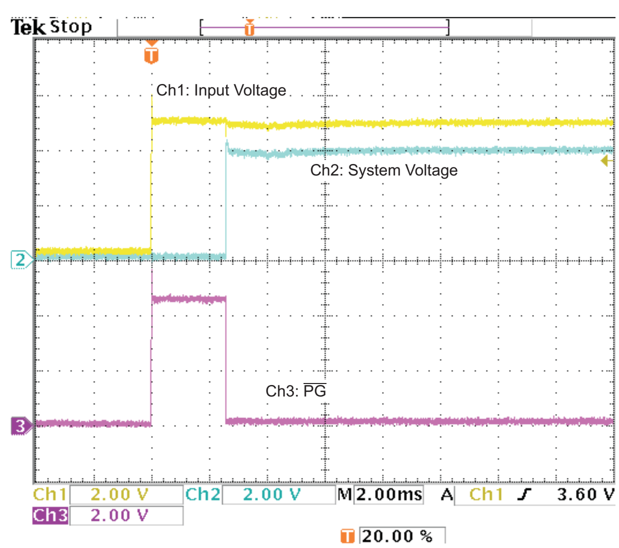
Figure 2 shows the output voltage regulation under system load current up to 800 mA. It shows that the circuit can achieve a reasonable regulation.

2. Transient waveform

   a. Input from 0 V to 5 V transient (normal input range)



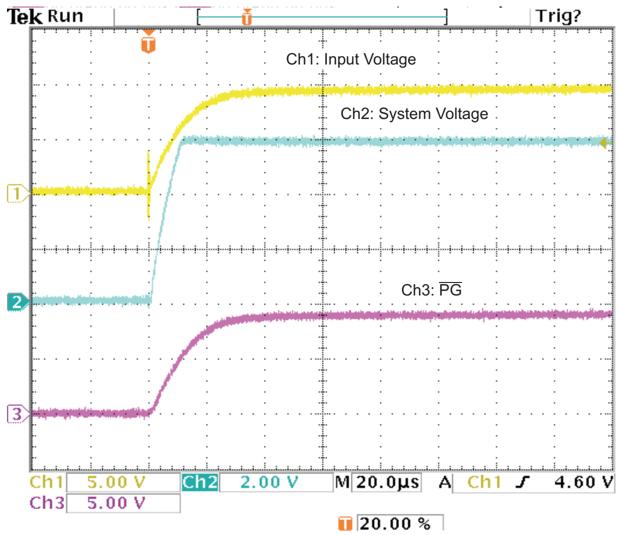
No Load



800 mA Load

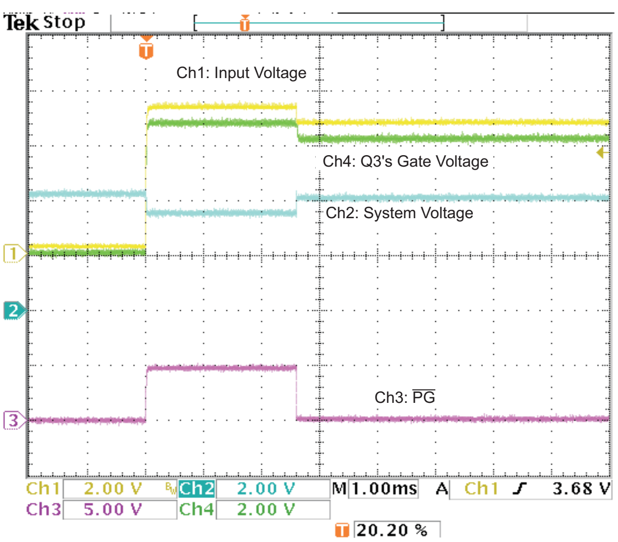
It is shown that $\overline{PG}$ pin pulls low to turn on the Q2 after a 2.5-ms delay. Then, Q1 received enough base current to support the system load current.

b. Input from 0 V to 10 V transient with no load

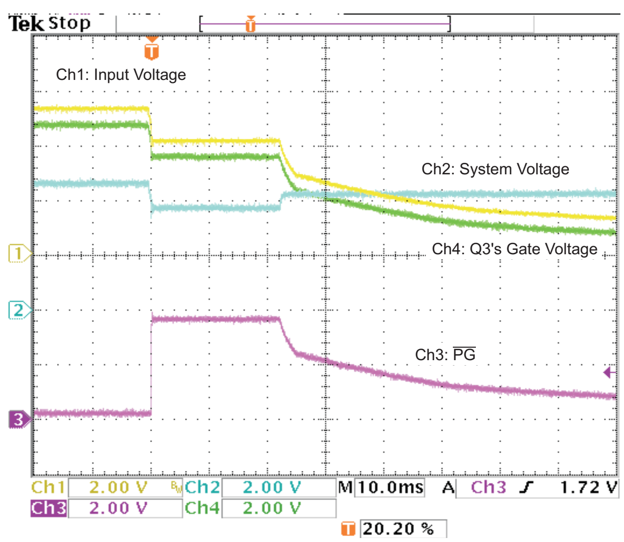


The PG pin holds Q2 off, and system voltage is regulated at approximately 6 V with no load condition. If system has some load, the voltage is even lower because Q2 is off and not enough base current is on Q1.

c. Adapter plug-in and removal



Adaptor Plug-in



Adaptor Removal

The battery voltage is set at 4.2 V; when the adapter is available, the gate voltage of Q3 follows the input voltage rising. It is lower than input voltage by the D2 forward voltage drop. P-MOSFET Q3 is turned off while Q3's gate-to-source voltage is smaller than turn-on threshold voltage. After Q3 is turned off, Q3's body diode holds the system load during the 2.5-ms $\overline{PG}$ deglitch period. After the deglitch period, $\overline{PG}$ pin turns on Q1 on, and the system is powered by the input power source.

When the adapter is removed, the $\overline{PG}$ pin is active-high and turns off Q1. The battery current goes through the Q3's body diode first and the gate capacitor of Q3 is discharged by R1; then, Q3 is turned on while Q3's gate-to-source voltage is bigger than the turn-on threshold voltage. The battery provides power to the system.

4 Reference

1. *Implementations of Battery Charger and Power-Path Management System Using bq2410x/11x/12x (bqSWITCHER™)* application report (SLUA376)