Application Report

SNAA011C–February 1994–Revised April 2013

# AN-929 Microcontroller Interface to the ADC12038 Families


## ABSTRACT

The ADC12038 families are 12-bit plus sign sampling ADC converters with serial I/O. These devices have configurable analog multiplexers with 2, 4, or 8 input channels. On request, these A/Ds perform a self calibration routine that minimizes linearity, zero, and full-scale errors. To minimize power consumption these devices have a power down mode that can be accessed by hardware (PD pin) or by a software instruction.


## Contents



## List of Figures



## List of Tables

# 1 General Overview

The serial I/O is configured to comply with the NSC MICROWIRE serial data exchange standard for easy interface to the COPS and HPC families of controllers, and can easily interface with standard shift registers and microprocessors. The conversion resolution can be selected by a software instruction to be 8-bits, 8-bits+sign, 12-bits or 12-bits+sign. 8-bit and 8-bit+sign conversions take less time than 12-bit and 12-bit+sign conversions (21 clock periods versus 44). In addition, selection of the output data format can be software programmable to be:

- 8-bits, 8-bits+sign, 12-bits, 12-bits+sign, 16-bits or 16-bits+sign in length
- MSB or LSB first
- Left or right justified

There are three ADC12038 families: low voltage, high speed and standard. Each family includes four different combinations of analog inputs and features as summarized in Table 1.

**Table 1. Summary of the Differences of the Devices in the Three ADC12038 Families**

| Device Number | Operating Supply Voltage and Power Dissipation | Maximum Clock Frequency (MHz) | Maximum Sampling Rate (kHz) | Number of MUX Inputs | MUX OUT and A/D IN Pins | Hardware Power Down Control (PD Pin) | Package Size and Type |
|---|---|---|---|---|---|---|---|
| ADC12030 | 5V ±10% 33 mW (max) @5V | 5 MHz | 73 kHz | 2 | NO | NO | 16-pin DIP & SO |
| ADC12032 | | | | 2 | YES | NO | 20-pin DIP & SO |
| ADC12034 | | | | 4 | YES | YES | 24-pin DIP & SO |
| ADC12038 | | | | 8 | YES | YES | 28-pin DIP & SO |
| ADC12L030 | 3.3V ±10% 15 mW (max) @3.3V | | | 2 | NO | NO | 16-pin DIP & SO |
| ADC12L032 | | | | 2 | YES | NO | 20-pin DIP & SO |
| ADC12L034 | | | | 4 | YES | YES | 24-pin DIP & SO |
| ADC12L038 | | | | 8 | YES | YES | 28-pin DIP & SO |
| ADC12H030 | 5V ±10% 36 mW (max) @5V | 8 MHz | 116 kHz | 2 | NO | NO | 16-pin DIP & SO |
| ADC12H032 | | | | 2 | YES | NO | 20-pin DIP & SO |
| ADC12H034 | | | | 4 | YES | YES | 24-pin DIP & SO |
| ADC12H038 | | | | 8 | YES | YES | 28-pin DIP & SO |

Throughout this application report, the ADC12038 will be referred to. Any of this information will also apply to all the devices in the ADC12038 families. The device-specific data sheets should be used in conjunction with this document to help you understand the operation of these devices. The scope of this application report focuses on the digital interface. A brief overview of the digital functionality of these devices is included.

## *1.1 Serial Interface*

The ADC12038 families of analog-to-digital converters can be programmed for many modes of operation through their serial digital interface. The serial interface for the ADC12038 is comprised of the digital control lines SCLK, $\overline{\text{CS}}$, DO, DI, EOC, $\overline{\text{DOR}}$, PD and $\overline{\text{CONV}}$. Table 2 gives a brief pin description for each of these control lines.

**Table 2. Digital Control Pin Descriptions**

| Pin Name | Description |
|---|---|
| SCLK | This is the serial data clock input. The clock applied to this input controls the rate at which the serial data exchange occurs. With $\overline{\text{CS}}$ low the rising edge of SCLK loads the information on the DI pin into the multiplexer address and mode select shift register. This address controls which channel of the analog input multiplexer (MUX) is selected and the mode of operation for the ADC. With $\overline{\text{CS}}$ low the falling edge shifts of SCLK the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{\text{CS}}$ is low continuously, the first bit of the data is clocked out on the rising edge of end of conversion (EOC). When $\overline{\text{CS}}$ is toggled the falling edge of $\overline{\text{CS}}$ always clocks out the first bit of data. $\overline{\text{CS}}$ should be brought low when SCLK is low. |
| $\overline{\text{CS}}$ | This is the chip select pin. When a logic low is applied to this pin the device is selected, activating the DO, DI, and SCLK serial interface lines. The falling edge of $\overline{\text{CS}}$ resets a conversion in progress and starts the sequence for a new conversion. When $\overline{\text{CS}}$ is brought low during a conversion in progress, the conversion is prematurely ended and the data in the output latches may be corrupted, requiring the data output at this time to be ignored. $\overline{\text{CS}}$ should be brought low when SCLK is low. |
| DI | The data input pin. The data applied to this pin is shifted by the rising edge of SCLK into the multiplexer address and mode select register. Table 4 Table 5 Table 6 Table 7 show the assignments of the multiplexer address and the mode select data. |
| DO | The data output pin. This pin is an active push/pull output when $\overline{\text{CS}}$ is Low. When $\overline{\text{CS}}$ is High this output is in TRI-STATE. The ADC conversion result and converter status data are clocked out by the falling edge of SCLK on this pin. |
| EOC | This pin is an active push/pull output and indicates the status of the device. When Low, it signals that the ADC is busy with a conversion, auto-calibration, auto-zero or power down cycle. The rising edge of EOC signals the end of one of these cycles. |
| $\overline{\text{DOR}}$ | This is the data output ready pin. This pin is an active push/pull output. It is useful only when $\overline{\text{CS}}$ is toggled. |
| $\overline{\text{CONV}}$ | A logic Low is required on this pin to program any mode or change the ADC's configuration (12-bit conversion, 8-bit conversion, Auto Cal, Auto Zero, and so forth) as listed in the Mode Programming Table (Table 4). When this pin is high the ADC is placed in the read data only mode. While in the read data only mode, bringing $\overline{\text{CS}}$ low and Pulsing SCLK will only clock out on DO any data stored in the ADCs output shift register. The data on DI will be neglected. A new conversion will not be started and the ADC will remain in the mode and/or configuration previously programmed. Read data only cannot be performed while a conversion, Auto-Cal or Auto-Zero are in progress. |
| PD | This is the power down pin. When PD is high, the ADC is powered down; when PD is low, the ADC is powered up. |

The interplay of these lines can be graphically seen in the timing diagram of Figure 1.

The chip select pin ($\overline{\text{CS}}$) enables the logic inputs and DO output. Eight bits of data that control the ADC are clocked in on the digital input pin (DI) by the rising edge of the serial clock (SCLK) when $\overline{\text{CS}}$ is low. Taking $\overline{\text{CS}}$ will output the first bit of data (DBO) on DO. While $\overline{\text{CS}}$ is low, the falling edge of SCLK clocks the data out on the digital output pin (DO). $\overline{\text{CS}}$ should only be brought low when SCLK is low. The functions of the convert input ($\overline{\text{CONV}}$), data output ready ($\overline{\text{DOR}}$) and end of conversion output (EOC) pins are covered in more detail in the device-specific data sheet. The simplest interface to the ADC12038 requires only 4 control lines: DO, DI, SCLK and $\overline{\text{CS}}$. For this case $\overline{\text{CONV}}$ and PD are grounded and EOC and $\overline{\text{DOR}}$ outputs are not used.

## 1.2 Serial Output Word Format

The diagram in Figure 2 shows a 16-bit serial output word. The ADC12038 family can be programmed to provide unsigned output data in 8-bit, 12-bit, or 16-bit word lengths or signed data in 9-bit, 13-bit, or 17-bit word lengths. The data format can be right- or left-justified, MSB or LSB first. Table 3 summarizes the available serial output data formats. Table 4 describes the serial input word required to select the available serial output data formats.

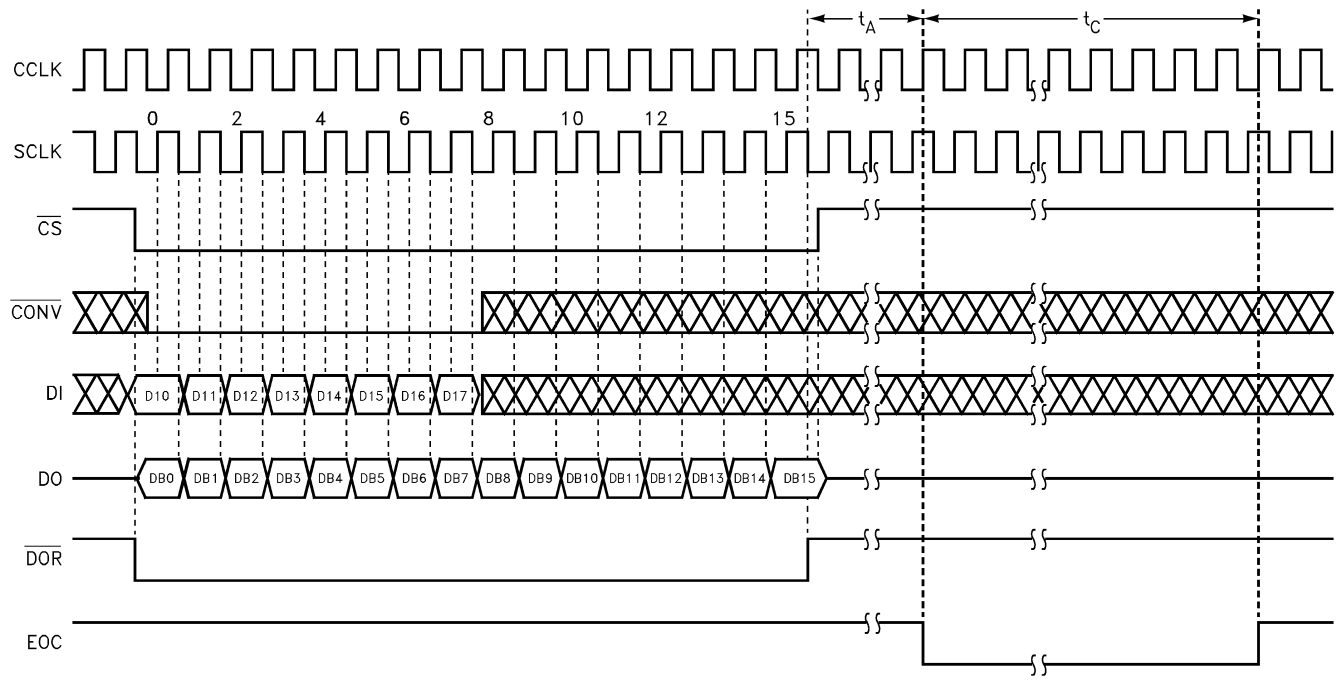



**Figure 1. Timing Diagram for a 12-Bit Plus Sign Conversion With a 16-Bit Serial Output Word Format on DO**

**Table 3. Data Out Formats**

| DO Formats | | | DB0 | DB1 | DB2 | DB3 | DB4 | DB5 | DB6 | DB7 | DB8 | DB9 | DB10 | DB11 | DB12 | DB13 | DB14 | DB15 | DB16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| with Sign | MSB First | 17 Bits | Sign | Sign | Sign | Sign | Sign | MSB | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | LSB |
| | | 13 Bits | Sign | MSB | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | LSB | | | | |
| | | 9 Bits | Sign | MSB | 6 | 5 | 4 | 3 | 2 | 1 | LSB | | | | | | | | |
| | LSB First | 17 Bits | LSB | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | MSB | Sign | Sign | Sign | Sign | Sign |
| | | 13 Bits | LSB | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | MSB | Sign | | | | |
| | | 9 Bits | LSB | 1 | 2 | 3 | 4 | 5 | 6 | MSB | Sign | | | | | | | | |
| without Sign | MSB First | 16 Bits | 0 | 0 | 0 | 0 | MSB | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | LSB | |
| | | 12 Bits | MSB | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | LSB | | | | | |
| | | 8 Bits | MSB | 6 | 5 | 4 | 3 | 2 | 1 | LSB | | | | | | | | | |
| | LSB First | 16 Bits | LSB | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | MSB | 0 | 0 | 0 | 0 | |
| | | 12 Bits | LSB | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | MSB | | | | | |
| | | 8 Bits | LSB | 1 | 2 | 3 | 4 | 5 | 6 | MSB | | | | | | | | | |

The falling edge of SCLK strobes out the digital word on DO when $\overline{CS}$ is low. The digital word length will vary in accord with the digital word format. Thus, for 8-bits + sign resolution 9 clock cycles are required.

As shown in the timing diagram (Figure 1), the acquisition time (the period of time during which the analog input is being sampled) starts on the falling edge of the last data clock cycle. For 16 bits of data that would be the 16th clock; for 8 bits of data that would be the 8th clock. The length of the acquisition time that can be programmed by you with an instruction, (see Table 4). The acquisition time can be set to 6, 10, 18, or 34 CCLK cycles.

### 1.3 Selecting Output Word Format and Mode

While $\overline{CS}$ is low, the rising edge of SCLK strobes in the data bits DI0–DI7 on the DI control line. For the ADC12038, the values of DI0–DI7 determine the digital output word format, mode select, and multiplexer configuration. For the ADC12034, 7 bits of data (DI0–DI6) are required. The ADC12032, and ADC12030 require only 6 bits of data (DI0–DI5). Mode Select determines the number of clock periods for the acquisition time ($t_A$), software power up/down, Auto Cal, Auto Zero and other functions as shown in Table 4.

**Table 4. Mode Programing** [(1)]

| ADC12038 | DI0 | DI1 | DI2 | DI3 | DI4 | DI5 | DI6 | DI7 | Mode Select (Current) | DO Format (next Conversion Cycle) |
|---|---|---|---|---|---|---|---|---|---|---|
| ADC12034 | DI0 | DI1 | DI2 | | DI3 | DI4 | DI5 | DI6 | | |
| ADC12030 and ADC12032 | DI0 | DI1 | | | DI2 | DI3 | DI4 | DI5 | | |
| | MUX Address, see Table 5 Table 6 or Table 7 | | | | L | L | L | L | 12-Bit Conversion | 12- or 13-Bit MSB First |
| | MUX Address, see Table 5 Table 6 or Table 7 | | | | L | L | L | H | 12-Bit Conversion | 16-Bit MSB First |
| | MUX Address, see Table 5 Table 6 or Table 7 | | | | L | L | H | L | 8-Bit Conversion | 8- or 9-Bit MSB First |
| | L | L | L | L | L | L | H | H | 12-Bit Conversion of Full-Scale | 12- or 13-Bit MSB First |
| | MUX Address, see Table 5 Table 6 or Table 7 | | | | L | H | L | L | 12-Bit Conversion | 12- or 13-Bit LSB First |
| | MUX Address, see Table 5 Table 6 or Table 7 | | | | L | H | L | H | 12-Bit Conversion | 16-Bit LSB First |
| | MUX Address, see Table 5 Table 6 or Table 7 | | | | L | H | H | L | 8-Bit Conversion | 8- or 9-Bit LSB First |
| | L | L | L | L | L | H | H | H | 12-Bit Conversion of Offset | 12- or 13-Bit LSB First |
| | L | L | L | L | H | L | L | L | Auto Cal | No Change |
| | L | L | L | L | H | L | L | H | Auto Zero | No Change |
| | L | L | L | L | H | L | H | L | Power Up | No Change |
| | L | L | L | L | H | L | H | H | Power Down | No Change |
| | L | L | L | L | H | H | L | L | Read Status Register (LSB First) | No Change |
| | L | L | L | L | H | H | L | H | Data Out without Sign | No Change |
| | H | L | L | L | H | H | L | H | Data Out with Sign | No Change |
| | L | L | L | L | H | H | H | L | Acquisition Time—4 CCLK Cycles | No Change |
| | L | H | L | L | H | H | H | L | Acquisition Time—8 CCLK Cycles | No Change |
| | H | L | L | L | H | H | H | L | Acquisition Time—16 CCLK Cycles | No Change |
| | H | H | L | L | H | H | H | L | Acquisition Time—32 CCLK Cycles | No Change |
| | L | L | L | L | H | H | H | H | User Mode | No Change |
| | H | L | L | L | H | H | H | H | Test Mode (CH1–CH7 become Active Outputs) | No Change |

(1) The A/D powers up with No CAL, No Auto-Zero, 10 CCLK cycles acquisition time, sign bit on, 13-bit MSB first format, power up, and user mode.

## 1.4 Multiplexer Addressing

The analog input channel configuration is selected during mode programming using the “MUX address” bits in Table 4. These bits and their effects are defined in Table 5, Table 6, and Table 7.

**Table 5. ADC12038 Multiplexer Addressing**

| MUX Address | | | | Analog Channel Addressed and Assignment With A/D IN1 tied to MUXOUT1 and A/D IN2 tied to MUXOUT2 | | | | | | | | | A/D Input Polarity Assignment | | Multiplexer Output Channel Assignment | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DI0 | DI1 | DI2 | DI3 | CH0 | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 | COM | A/D IN1 | A/D IN2 | MUXOUT1 | MUXOUT2 | Mode |
| L | L | L | L | + | − | | | | | | | | + | − | CH0 | CH1 | Differential |
| L | L | L | H | | | + | − | | | | | | + | − | CH2 | CH3 | |
| L | L | H | L | | | | | + | − | | | | + | − | CH4 | CH5 | |
| L | L | H | H | | | | | | | + | − | | + | − | CH6 | CH7 | |
| L | H | L | L | − | + | | | | | | | | − | + | CH0 | CH1 | |
| L | H | L | H | | | − | + | | | | | | − | + | CH2 | CH3 | |
| L | H | H | L | | | | | − | + | | | | − | + | CH4 | CH5 | |
| L | H | H | H | | | | | | | − | + | | − | + | CH6 | CH7 | |
| H | L | L | L | + | | | | | | | | − | + | − | CH0 | COM | Single-Ended |
| H | L | L | H | | | + | | | | | | − | + | − | CH2 | COM | |
| H | L | H | L | | | | | + | | | | − | + | − | CH4 | COM | |
| H | L | H | H | | | | | | | + | | − | + | − | CH6 | COM | |
| H | H | L | L | | + | | | | | | | − | + | − | CH1 | COM | |
| H | H | L | H | | | | + | | | | | − | + | − | CH3 | COM | |
| H | H | H | L | | | | | | + | | | − | + | − | CH5 | COM | |
| H | H | H | H | | | | | | | | + | − | + | − | CH7 | COM | |

**Table 6. ADC12034 Multiplexer Addressing**

| MUX Address | | | Analog Channel Addressed and Assignment With A/D IN1 tied to MUXOUT1 and A/D IN2 tied to MUXOUT2 | | | | | A/D Input Polarity Assignment | | Multiplexer Output Channel Assignment | | Mode |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DI0 | DI1 | DI2 | CH0 | CH1 | CH2 | CH3 | COM | A/D IN1 | A/D IN2 | MUXOUT1 | MUXOUT2 | |
| L | L | L | + | − | | | | + | − | CH0 | CH1 | Differential |
| L | L | H | | | + | − | | + | − | CH2 | CH3 | |
| L | H | L | − | + | | | | − | + | CH0 | CH1 | |
| L | H | H | | | − | + | | − | + | CH2 | CH3 | |
| H | L | L | + | | | | − | + | − | CH0 | COM | Single- Ended |
| H | L | H | | | + | | − | + | − | CH2 | COM | |
| H | H | L | | + | | | − | + | − | CH1 | COM | |
| H | H | H | | | | + | − | + | − | CH3 | COM | |

**Table 7. ADC12032 and ADC12030 Multiplexer Addressing [(1)]**

| MUX Address | | Analog Channel Addressed and Assignment With A/D IN1 tied to MUXOUT1 and A/D IN2 tied to MUXOUT2 | | | A/D Input Polarity Assignment | | Multiplexer Output Channel Assignment | | |
|---|---|---|---|---|---|---|---|---|---|
| DI0 | DI1 | CH0 | CH1 | COM | A/D IN1 | A/D IN2 | MUXOUT1 | MUXOUT2 | Mode |
| L | L | + | − | | + | − | CH0 | CH1 | Differential |
| L | H | − | + | | − | + | CH0 | CH1 | |
| H | L | + | | − | + | − | CH0 | COM | Single- Ended |
| H | H | | + | − | + | − | CH1 | COM | |

(1) MUXOUT1, MUXOUT2, A/D IN1 and A/D IN2 pins are not available on the ADC12030. A/D IN1 is tied internally to MUXOUT1: A/D IN2 is tied internally to MUXOUT2.

As can be seen in the tables, 4, 3 or 2 bits of the serial digital input word control the channel selection. These bits are part of an 8-, 7-, or 6-bit serial word that controls the function of the devices.

## 1.5 Status Register Definition

On request, the ADC12038 provides status information indicating power up or power down status, output data format, Auto-Cal status, and User/Test Mode status. Table 8 defines the digital output data obtained after requesting a “Status Read”.

When $\overline{CS}$ is used it is not necessary to clock all the status bits out. $\overline{CS}$ may be brought high at any time to restart a new serial data communication.

## 1.6 Programming Procedure

The example in Figure 2 shows a typical sequence of events after power is applied to the ADC12038.

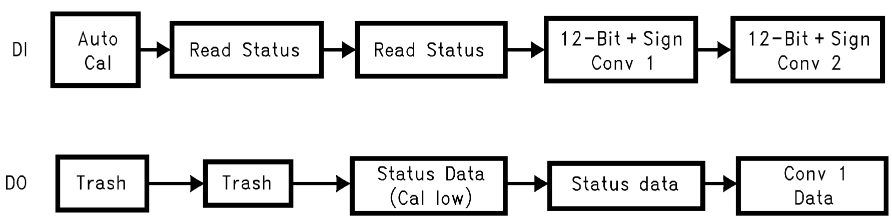



**Figure 2. Typical Instruction Sequence after Power Up**

The first instruction to the ADC via DI initiates Auto Cal. The data output on DO at that time is meaningless and is completely random. To obtain the specified accuracy of the device it is necessary to issue an Auto Cal instruction after the power supply and reference voltage to the device have been given enough time to stabilize. The Auto Cal instruction initiates an internal calibration sequence without which the specified accuracy of the device would be unattainable. To determine whether the Auto Cal has been completed, a Read Status instruction is issued to the device. Again, the data obtained while issuing the Read Status instruction has no significance since the Auto Cal instruction modifies the data in the output shift register. To retrieve the status information an additional read status instruction is issued to the ADC. At this time the status data is available on DO. If the Cal signal in the status word is low, Auto Cal has been completed. Therefore, the next instruction issued can start a conversion. The data output, while clocking in the “start conversion request”, is again status information. Status can not be read during a conversion. To preserve the integrity of the A/D conversion, there is no end of conversion bit in the status word. If $\overline{CS}$ is brought low during a conversion, that conversion is stopped and never completed. EOC can be used to determine the end of a conversion or the A/D controller can keep track in software of when it would be appropriate to communicate to the A/D again. Once it has been determined that the A/D has completed a conversion another instruction can be transmitted to the A/D. The data from this conversion can be accessed when the next instruction is issued to the A/D.

**Table 8. Status Register**

| **Status Bit Location** | DB0 | DB1 | DB2 | DB3 | DB4 | DB5 | DB6 | DB7 | DB8 |
|---|---|---|---|---|---|---|---|---|---|
| **Status Bit** | PU | PD | Cal | 8 or 9 | 12 or 13 | 16 or 17 | Sign | Justification | Test Mode |
| **Function** | Device Status | | | DO Output Format Status | | | | | |
| | "High" indicates a Power Up State | "High" indicates a Power Down State | "High" indicates an Auto-Cal Sequence is in progress | "High" indicates an 8- or 9-bit format | "High" indicates a 12- or 13-bit format | "High" indicates a 16- or 17-bit format | "High" indicates that the sign bit is included. When "Low", the sign bit is not included. | When "High", the conversion result will be output MSB first. When "Low", the result will be output LSB first. | When "High", the device is in test mode. When "Low", the device is in user mode. |

## 2 General Flow Chart for a Microcontroller Interface

Below is a flow chart that can be used for a microcontroller interface to the ADC12038. The data required by the ADC12038 is given in parentheses.

The timing diagrams shown to the right are suggested for each instruction issued to the ADC.

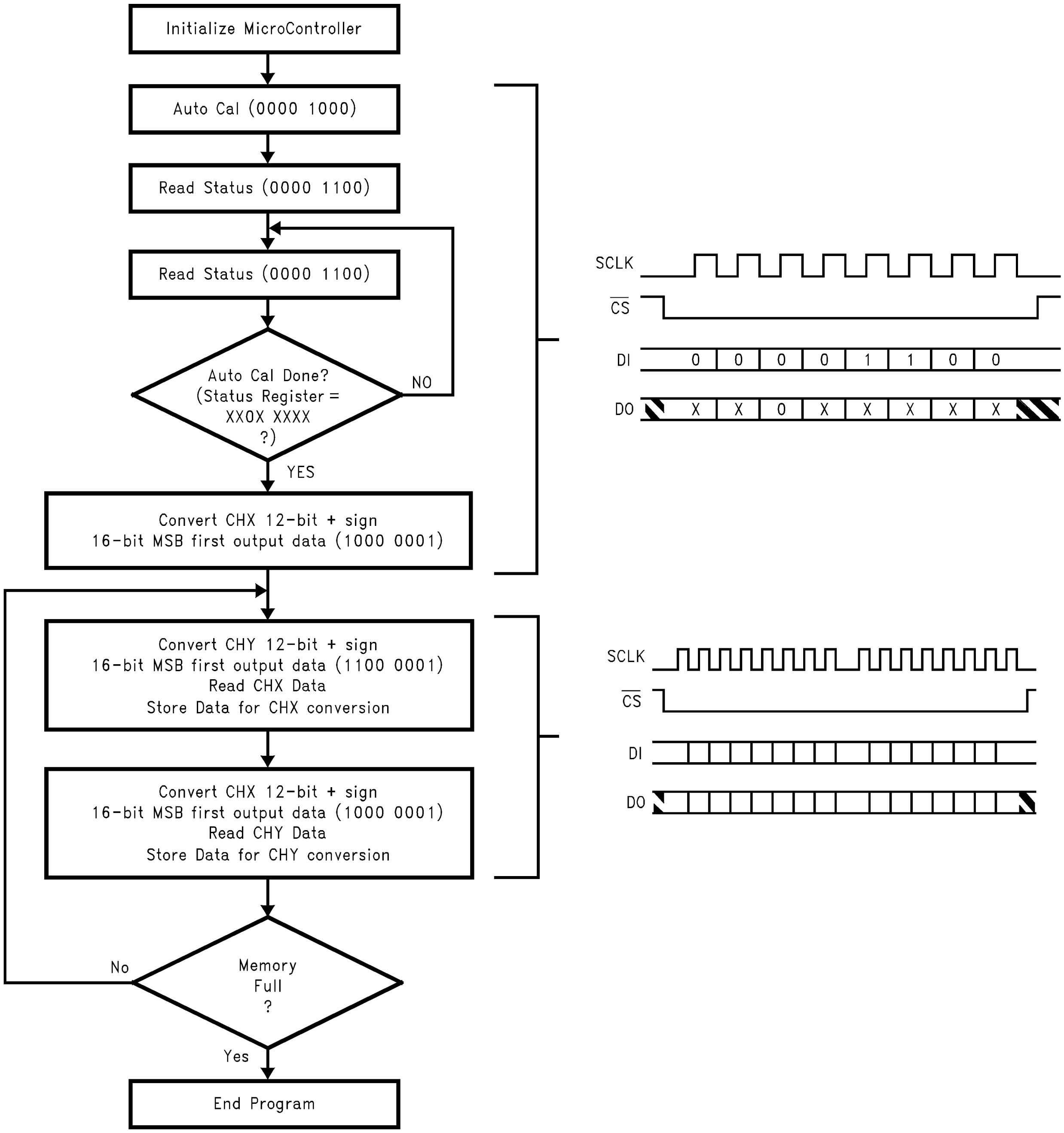



**Figure 3. ADC12038 Program Flow Chart and Timing**

# 3 Examples of Microcontroller Hardware Implementations

## 3.1 The 68HC11

Figure 4 shows the hardware interface to a Motorola M68HC11 microcontroller. Motorola's Serial Peripheral Interface (SPI) SCK, MISO, and MOSI lines are directly tied to the SCLK, DO and DI of the ADC12038. Port B bit 0 is used to generate the $\overline{CS}$ to the ADC.

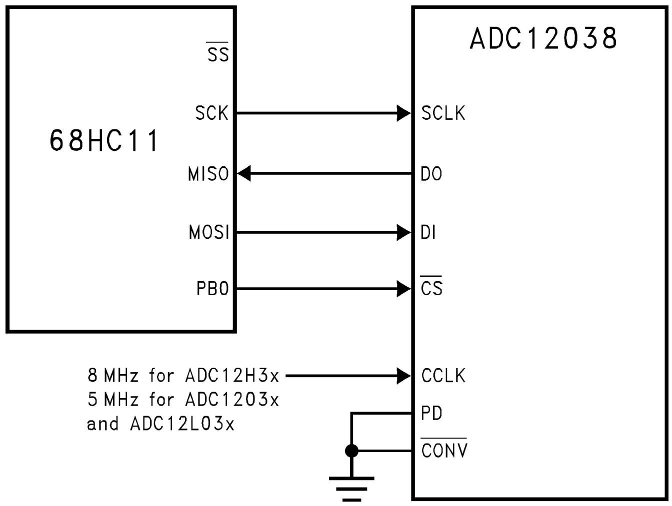



**Figure 4. 68HC11 ADC12038 Hardware Interface**

## 3.2 Texas Instruments HPC and COP

The serial I/O for these devices is configured to comply with the NSC MICROWIRE serial data exchange standard for easy interface to the COPS and HPC families of controllers. The output data format is software-programmable, making the serial interface extremely flexible and an ideal choice for many applications. Figure 5 shows an implementation of TI's HPC microcontroller interface. The serial clock (SK), serial input data (SI) and serial output data (SO) lines of the HPC, used in TI's MICROWIRE interface, are tied directly to the ADC12038. Port B, bit 6 is used to generate a $\overline{CS}$ for the ADC.

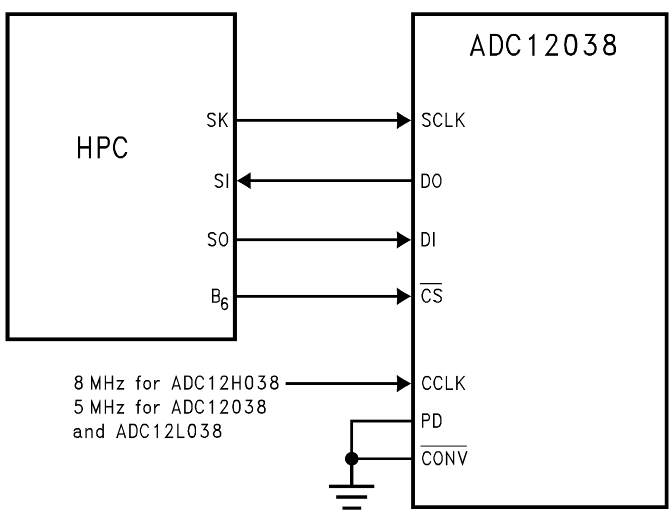



**Figure 5. HPC to ADC12038 Hardware Interface**

### 3.3 The 8051

Figure 6 shows the ADC12038 connected to an Intel 8051. The 8051 serial interface does not support the protocol of the serial interface for this device. Therefore, three port lines from the 8051 (P1.0, P1.1 and P1.2) can be used to talk to the ADC. The software toggles these lines directly to form the signals necessary to control the ADC.

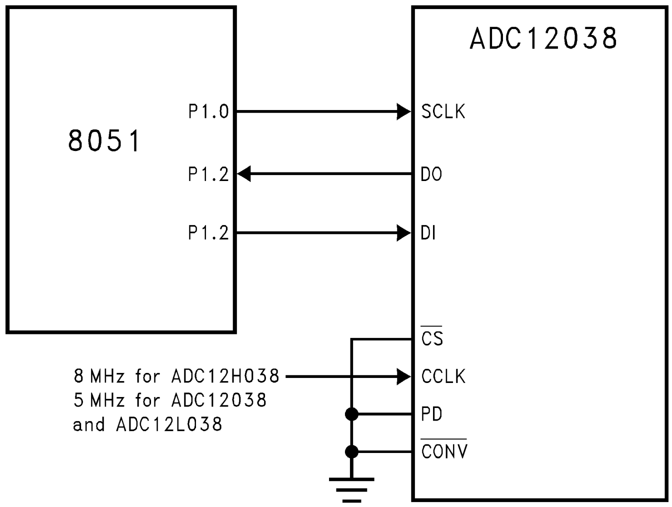



**Figure 6. 8051 ADC12038 Hardware Interface**

## 4 68HC11 SPI Interface

This section describes in detail an SPI interface to the ADC12038. Figure 7, shown below, is a detailed schematic of the interface. The Motorola M68HC11EVB evaluation board was used to verify the program included at the end of this section. Therefore, the schematic shown here shows the connections required to the 68HC11 evaluation board.

### 4.1 68HC11 SPI Port and Register Initialization for the ADC12038

The 68HC11 SPI interface is ideal for driving the ADC12038. The SCK, MISO, and MOSI lines of the SPI tie directly to the SCLK, DO and DI lines of the ADC. $\overline{CS}$ for the ADC is generated using a line of the 68HC11's output port B. Here is a brief overview of the 68HC11 ports and registers used by the SPI.

The 68HC11 has four I/O ports. Port D can be set up as a general purpose I/O port or it can be used for the SPI interface and Serial Control Interface (SCI). The signal assignments for port D when used for SPI or SCI follow:

| PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
|---|---|---|---|---|---|---|---|
| X | X | SS | SCK | MOSI | MISO | TXD | RXD |

Slave select (SS), serial clock (SCK), Master output slave input (MOSI), Master input Slave output (MISO) are used for the SPI. SCI uses TXD and RXD.

There are two registers in the 68HC11 that need to be initialized: the Data Direction Register for port D (DDRD) and the Serial Peripheral Control Register (SPCR).

### 4.1.1 DDRD

If ones are placed in the locations corresponding to the signal assignments for port D, those signals will be selected as outputs (except for the SS location). A one placed in the SS location disables that function. The SS input can be used for synchronizing master/slave communications between 68HC11s on the SPI bus. If SS is enabled and the 68HC11 is set as master then the SS input should be hard wired to a logical “high” for our case. Shown below is the data required to initialize DDRD for the ADC12038 interface. SS is disabled; SCK and MOSI are set as outputs; MISO is set as an input. TXD and RXD are not used but are set as input and output.

| PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
|---|---|---|---|---|---|---|---|
| X | X | 1 | 1 | 1 | 0 | 1 | 0 |

DDRD resides at address i009. On the 68HC11 development board this address is 1009. All register addresses on the development board start at 1000. 0000 through 0FFF are used by the software that controls the development board. In an actual system the registers can be remapped to any 4k boundary by software.

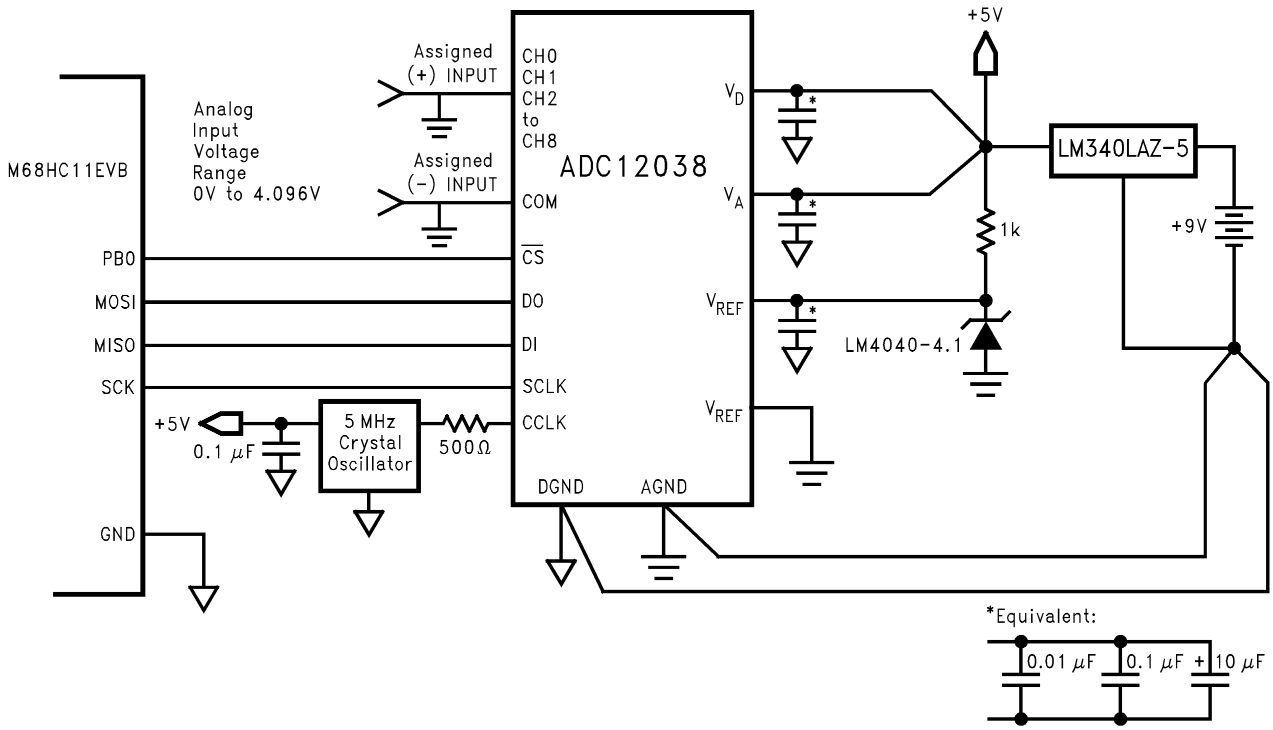



**Figure 7. Detailed Schematic of ADC12038 to M68HC11EVB Interface**

### 4.1.2 SPCR

On power up the SPI is disabled. The data stored in the Serial Peripheral Control Register (SPCR) controls how the SPI functions. SPCR resides at address 1028 for the development board. The table below summarizes the functions of the bits in this register. The Serial Peripheral Interrupt Enable (SPIE) bit when set to 1 allows the use of an interrupt to signal when an I/O exchange has completed. The Serial Peripheral Enable (SPE) bit when set to 1 enables the SPI. DWOM bit when set to 1 sets the outputs of port D to open drain. When this bit is low port D has totem pole outputs. MSTR bit controls whether this 68HC11 is a master or slave. When set to a 1 the 68HC11 is set as a master. In the slave mode SCK is an input. The CPOL and CPHA control the inactive level of the SCK output as well as which edge of the SCK output strobes the data out or in on the MISO or MOSI pins of port D. With both these bits set low the timing is as shown in Figure 8.

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|
| SPIE | SPE | DWOM | MSTR | CPOL | CPHA | SPR1 | SPR0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

The 68HC11 clocks in the data on MISO using the rising edge of SCK. Data on MOSI changes on the falling edge of SCK. This timing matches what the ADC12038 expects. SPR1 and SPR2 control the frequency of SCK as shown in Table 9.

**Table 9. SCK Frequency Control**

| XTAL Frequency | Internal Processor Clock | SCK Frequency | Internal Processor Clock Divide by | SPR1 | SPR0 |
|---|---|---|---|---|---|
| 8 MHz | 2 MHz | 1 MHz | 2 | 0 | 0 |
| 8 MHz | 2 MHz | 500 kHz | 4 | 0 | 1 |
| 8 MHz | 2 MHz | 250 kHz | 8 | 1 | 0 |
| 8 MHz | 2 MHz | 125 kHz | 16 | 1 | 1 |

The SPI Status Register (SPSR) logs the status of the SPI I/O interchange. The only bit that is of concern is the SPI,F which when set, signals that the SPI interchange is complete.

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|
| SPIF | | | | | | | |

SPI Data Register (SPDR) is an 8-bit register used to exchange input and output data on the SPI. A write to this register will initiate an SPI exchange. The data input to the 68HC11 after an SPI exchange will reside in this register. This register resides at address 1029 for the development system.

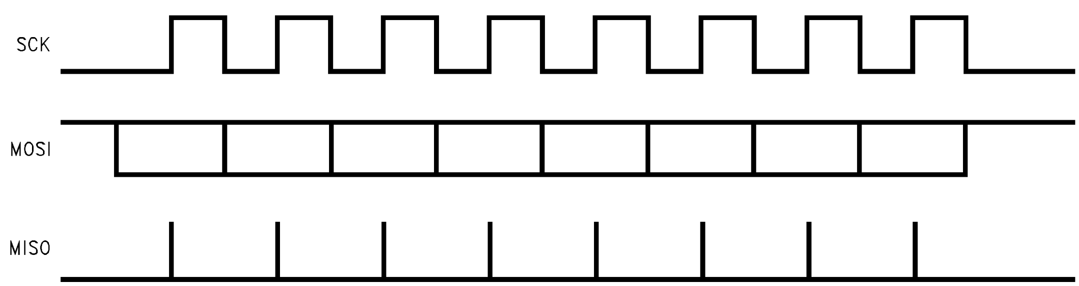
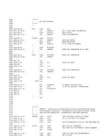



**Figure 8. SPI Timing Diagram Required for the ADC12038**

## 4.2 68HC11 Program Listing

The following program listing follows the flow chart given in Section 2.

```
*************************************************************************************
                    *       Emmy Denton                 3/4/93
                    *
                    *       ADC12'38 MC68HC11 SPI Interface
                    *
                    *
                    *       This program
                    *               1. Initializes the SPI interface
                    *               2. Starts a self calibration
                    *               3. Fills memory locations C200-C2FF with
                    *                conversions of CH0 and CH1 set up as single ended,
                    *                12-bit +sign MSB first
                    *
*************************************************************************************
                    *
0081                CH0CONV  EQU    %10000001         ADC DI FOR CH0 CONVERSION
00c1                CH1CONV  EQU    %11000001         ADC DI FOR CH1 CONVERSION
0008                CAL      EQU    $08               ADC DI FOR CALIBRAITON
000c                STATUS   EQU    $0C               ADC DI FOR STATUS READ
c1ff                STARTDATA EQU   $C1FF             START ADDRESS - 1 FOR CONVERSION RESULTS
c2ff                ENDDATA  EQU    $C2FF             END ADDRESS FOR CONVERSION RESULTS
1009                DDRD     EQU    $1009             DATA DIRECTION REGISTER ADDRESS
1028                SPCR     EQU    $1028             SPI CONTROL REGISTER ADDRESS
1029                SPSR     EQU    $1029             SPI STATUS REGISTER ADDRESS
102a                SPDR     EQU    $102A             SPI DATA REGISTER ADDRESS
1004                PORTB    EQU    $1004             PORT B ADDRESS
1008                PORTD    EQU    $1008             PORT D ADDRESS (SPI OUTPUT)


c000                         ORG    $C000             STARTING ADDRESS OF PROGRAM*





                    *******
                    *        INITIALIZE SPI INTERFACE PORT
                    *******
c000 86 20                   LDAA   #$20
c002 b7 10 08                STAA   PORTD             SET SCK TO 0, MISO TO 0, SS TO 1

c005 86 3a                   LDAA   #$3A              SET DDRD: DISABLE SS; SCK, MOSI, TXD - OUTPUTS;
c007 b7 10 09                STAA   DDRD                        MISO,RXD - INPUTS.
                    *
c00a 86 50                   LDAA   #$50              SET SPCR
c00c b7 10 28                STAA   SPCR





                    *******
                    *        INITIALIZE PORT B AND X INDEX REGISTER
                    *******
c00f f6 10 04                LDAB   PORTB             PLACE PORT B DATA INTO ACC B
c012 ca 01                   ORAB   #$01              (BIT 0 OF PORT B IS ADC CS) SET CS OF ADC HIGH
c014 f7 10 04                STAB   PORTB
c017 ce c1 ff                LDX    #STARTDATA        SET X INDEX REGISTER TO START OF ADC DATA
                    *




                    *
```



```
                     *
                     *******
                     *        SBWRADC - Subroutine to Output/Input 16 bits to/from ADC (SPI port)
                     *        UPON ENTERING SUBROUTINE - ACCUMULATOR A and B HAVE DATA TO OUTPUT TO ADC
                     *        UPON EXITING SUBROUTINE - ACCUMULATOR A AND B HAVE DATA FROM ADC
                     *******


c06e f6 10 04        SBWRADC  LDAB   PORTB           READ PREVIOUS SETTING OF PORTB
c071 c4 fe                    ANDB   #$FE            SET CS LOW (BIT 0 OF PORTB)
c073 f7 10 04                 STAB   PORTB
c076 b7 10 2a                 STAA   SPDR            WRITE ACCUMULATOR A TO SPI PORT AND READ BYTE 1

c079 b6 10 29        SPIWTB   LDAA   SPSR            WAIT FOR SPI INTERFACE
c07c 84 80                    ANDA   #$80            AND RESET SPI FOR ANOTHER TIMING SEQUENCE
c07e 27 f9                    BEQ    SPIWTB

c080 f6 10 2a                 LDAB   SPDR            LOAD SPI DATA (BYTE 1) INTO ACCUMULATOR B
c083 b7 10 2a                 STAA   SPDR            WRITE ACCUMULATOR A TO SPI PORT AND READ BYTE 2

c086 b6 10 29        SPIWTC   LDAA   SPSR            WAIT FOR SPI INTERFACE
c089 84 80                    ANDA   #$80            AND RESET SPI FOR ANOTHER TIMING SEQUENCE
c08b 27 f9                    BEQ    SPIWTC

c08d b6 10 04                 LDAA   PORTB           SET CS HIGH
c090 8a 01                    ORAA   #$01
c092 b7 10 04                 STAA   PORTB
c095 b6 10 2a                 LDAA   SPDR            LOAD SPI DATA (BYTE 2) INTO ACCUMULATOR A

c098 39                       RTS
                     *
```

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265