Application Report
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Low-Voltage (1.2-V) High-Efficiency Synchronous Buck Converter With TPS43000 PWM Controller

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ABSTRACT

The TPS43000 is a high-frequency, voltage-mode, synchronous PWM controller that can be flexibly used in buck, boost, buck-boost, and SEPIC topologies. This reference design explains the design procedure of a step-down application from 3.3 V to 1.2 V with the TPS43000 PWM controller.

Contents

1 Introduction

This full-featured controller is designed to drive a pair of external MOSFETs (N or P) and can be used with a wide range of output voltages and power levels. It can be widely used in networking equipment, servers, PDAs, cellular phones, and telecommunication applications. The datasheet describes the functionalities of the controller in more detail.

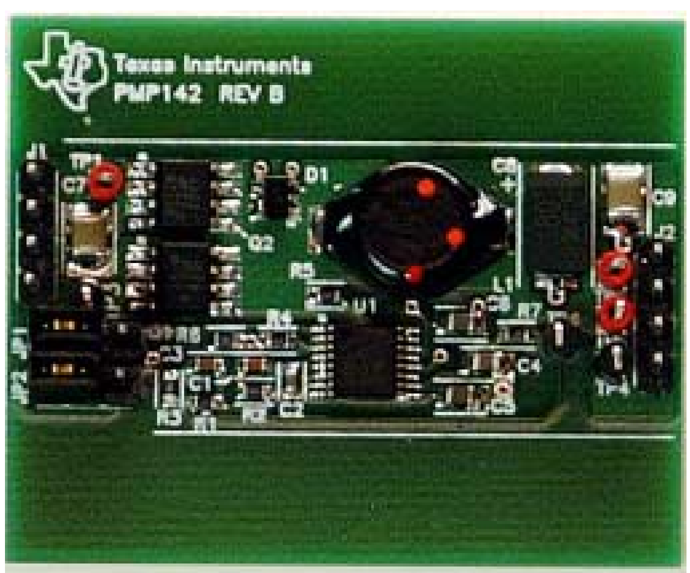

Figure 1. PMP 142 Board

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A schematic of this board is shown in Figure 1. Recommended parts list is provided in Table 1. The layout of the PCB board is shown in Figure 8.

The specification for this board is as follows:

- V_{IN} = 3.3 V ±15%
- V_{OUT} = 1.2 V
- 2 A ≤ I_{OUT} ≤ 5 A, nominal current is 3 A
- Ripple = 1%
- Efficiency at nominal load > 90%

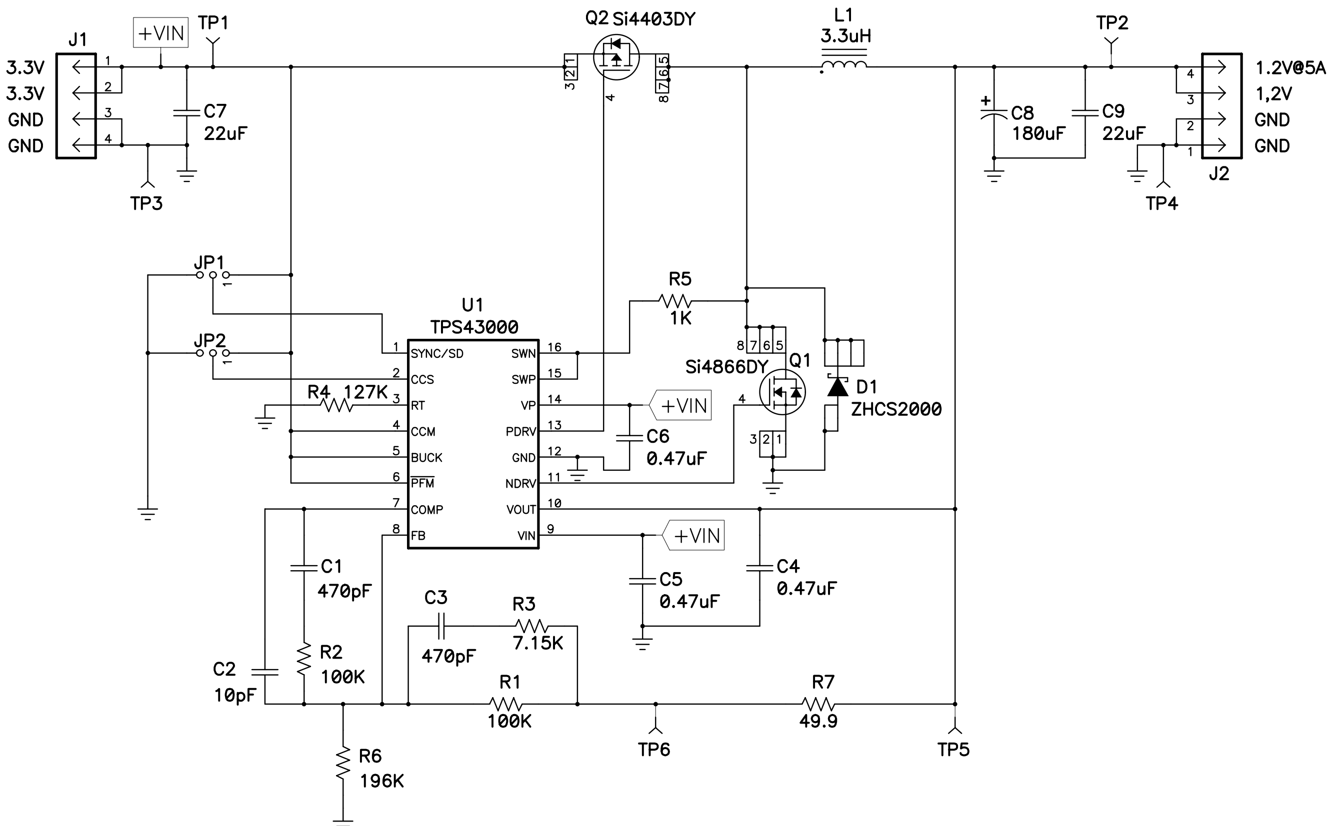

Figure 2. PMP142 Schematic

2 Design Procedure

2.1 Frequency Setting

The TPS43000 can operate either in constant frequency, or in an automatic PFM mode. In the automatic PFM mode, the controller goes to sleep when the inductor current goes discontinuous, and wakes up when the output voltage has fallen by 2%. (Please refer to the TPS43000 Data Sheet, TI Literature No. SLUS489 for more information.)The PFM mode is not used in this application. The converter is designed to operate at fixed 300 kHz.

A resistor, R4, connected from the RT pin to ground, programs the oscillator frequency. The approximate operating frequency is calculated in equation (1).

$$f\,(\mathrm{MHz}) = \frac{38}{\mathrm{R4}\ (\mathrm{k}\Omega)} \tag{1}$$

R4 = 127 kΩ is chosen for 300-kHz operation.

2.2 Inductance Value

The inductance value can be calculated as shown in equation (2).

$$L_{(min)} = \frac{V_{OUT}}{f \times I_{RIPPLE}} \times \left(1 - \frac{V_{OUT}}{V_{IN(min)}}\right) \tag{2}$$

I_{RIPPLE} is the ripple current flowing through the inductor, which affects the output voltage ripple and core losses. Based on 20% ripple current and 300 kHz, the inductance value is calculated as 2.7 µH and a 3.3 µH inductor is chosen.

2.3 Input and Output Capacitors

The output capacitance and required ESR can be calculated by equations (3) and (4).

$$C_{OUTPUT\ (min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} \tag{3}$$

$$ESR_{OUT} = \frac{V_{RIPPLE}}{I_{RIPPLE}} \tag{4}$$

With 1% output voltage ripple, the capacitance required is at least 29 µF and its ESR should be less than 15 mΩ. A Panasonic 2-V/180-µF capacitor is chosen with an ESR of 18 mΩ.

The required input capacitance is calculated in equation (5). The calculated value is approximately 70 µF. Considering that there is always a bulk capacitor on the output of a front-stage power supply, a 22-µF ceramic capacitor is used here, in order to handle the RMS current.

$$C_{IN\ (min)} = I_{OUT\ (max)} \times D_{(max)} \times \frac{T_S}{V_{IN}} \tag{5}$$

2.4 Compensation Design

The TPS43000 uses voltage-mode control. R1, R2, and R3 along with C1, C2 and C3, form a Type III compensator network. The L-C frequency of the power stage, f_C is approximately 6.5 kHz and the ESR zero is around 49.1 kHz, as shown in Figure 3. The overall crossover frequency, f_{0db} , is chosen at 25 kHz for reasonable transient response and stability. The two zeros, f_{Z1} and f_{Z2} from the compensator are set at 0.5 f_C and f_C separately. The two poles f_{P1} and f_{P2} are set at ESR zero and 0.5*f*. The frequency of poles and zeros are defined by the following equations:

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1}$$

$$f_{Z2} \approx \frac{1}{2\pi \times R1 \times C3} \quad \text{assuming } R1 \gg R3$$

$$f_{P1} = \frac{1}{2\pi \times R3 \times C3}$$

$$f_{P2} \approx \frac{1}{2\pi \times R2 \times C2} \quad \text{assuming } C1 \gg C2$$

The compensator values are calculated as follows:

C1 = 470 pF, C2 = 10 pF, C3 = 470 pF, R1 = 100 kΩ, R2 = 100 kΩ, and R3 = 7.15 kΩ.

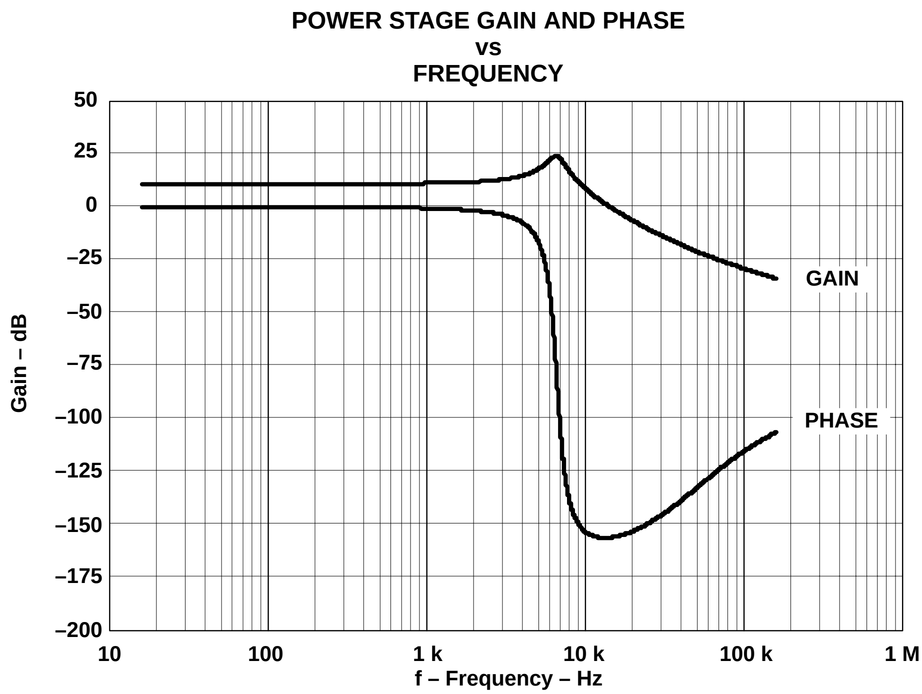

Figure 3.

2.5 MOSFETs and Diode

For a 1.2-V output voltage, the lower the $R_{DS(on)}$ of the MOSFET, the higher the efficiency. Si4486 ($R_{DS(on)}$ = 10 mΩ) and Si4403DV ($R_{DS(on)}$ = 20 mΩ) are chosen for their low $R_{DS(on)}$ values.

2.6 Current Limiting

Two types of current limiting can be selected from the controller. Detailed information is available in the datasheet (TI Literature No. SLUS489). A jumper, JP2, is used to choose different current limiting. By tying pin CCS to VIN, the controller enters pulse-by-pulse current limiting and the current-limiting threshold is calculated by equation (6):

$$I_{MAX\,(p-p)} = \frac{150\ mV}{R_{DS(on)}} \qquad (6)$$

in which $R_{DS(on)}$ is the on-resistance of Q2. In this design, the threshold is approximately 7.5A.

By tying the CCS pin to ground, the controller enters hiccup-mode overcurrent limiting . The current-limiting threshold is calculated in equation (7). The threshold in this case is approximately 12.5 A.

$$I_{MAX\,(hu)} = \frac{250\ mV}{R_{DS(on)}} \qquad (7)$$

2.7 Voltage Sense Resistor

R1 and R6 operate as the output voltage divider. The internal reference voltage is 0.8 V. The relationship between the output voltage and divider is described in equation (8).

$$\frac{V_{REF}}{R6} = \frac{V_{OUT}}{R1 + R6} \qquad (8)$$

Setting resistor R1 to 100 kΩ and using a value of 1.2-V output regulation, R6 is calculated as 196 kΩ.

3 Test Results

3.1 Efficiency Curves

Efficiency tested at different loads and input voltages is shown in Figure 4. The maximum efficiency is as high as 91.3% at 1.2-V output.

3.2 Typical Operation Waveform

Typical operating waveforms are shown in Figure 5 with V_{IN} = 3.3 V, I_{OUT} = 5 A.

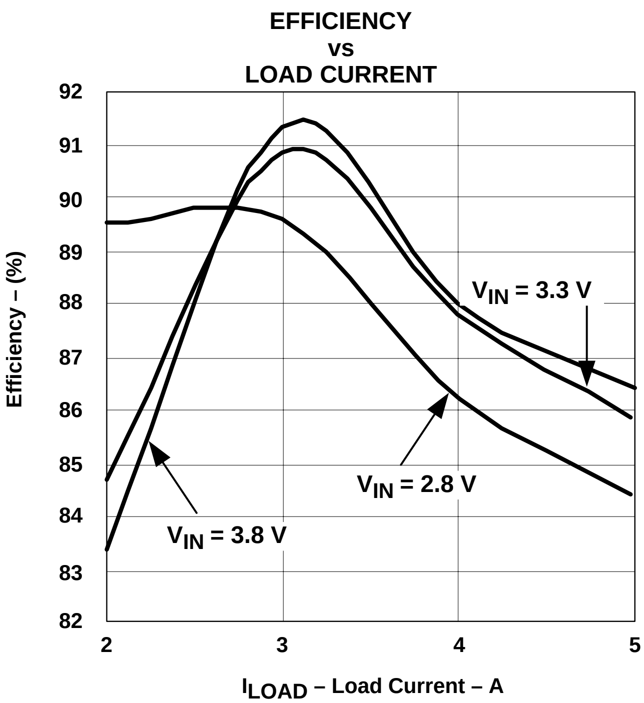

Figure 4.

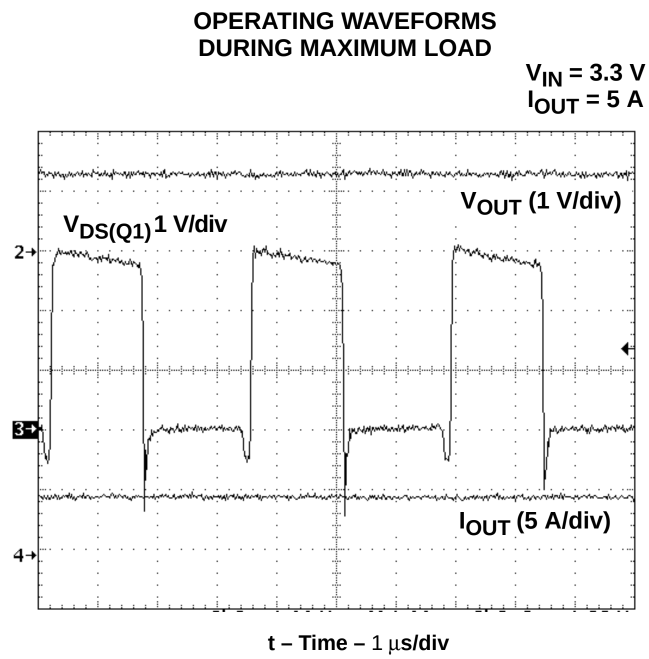

Figure 5.

3.3 Transient Response and Output Ripple Voltage

The output ripple is approximately 12 mV peak-to-peak with a 5-A output. When the load changes from 2 A to 5 A, the overshooting voltage is approximately 70 mV.

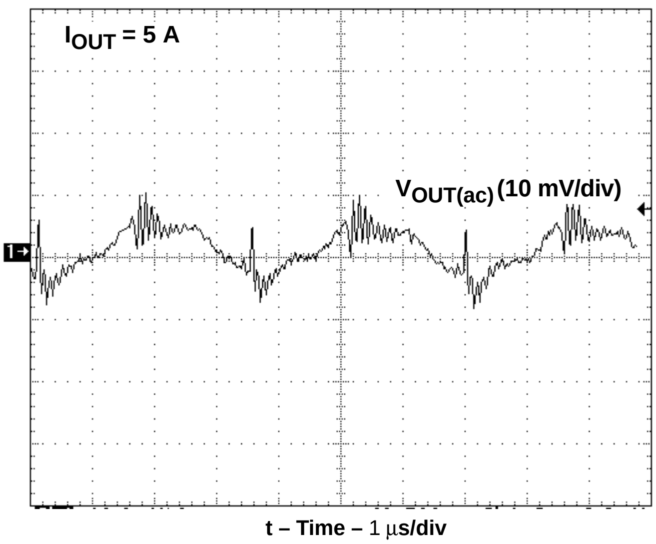

Figure 6. Output Ripple

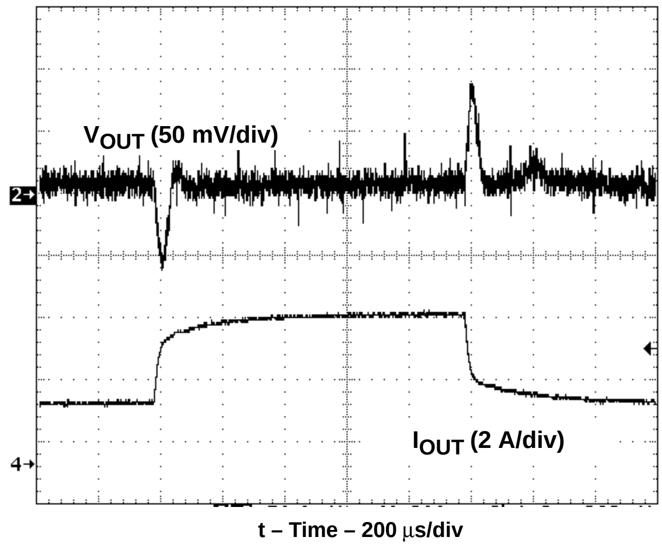

Figure 7. Transient Response

4 PCB Layout

Figures 8 and 9 show the PCB layout . All components are on the top side of the board. The bottom side of the board is the ground plane. The PWB is made large to dissipate the losses.

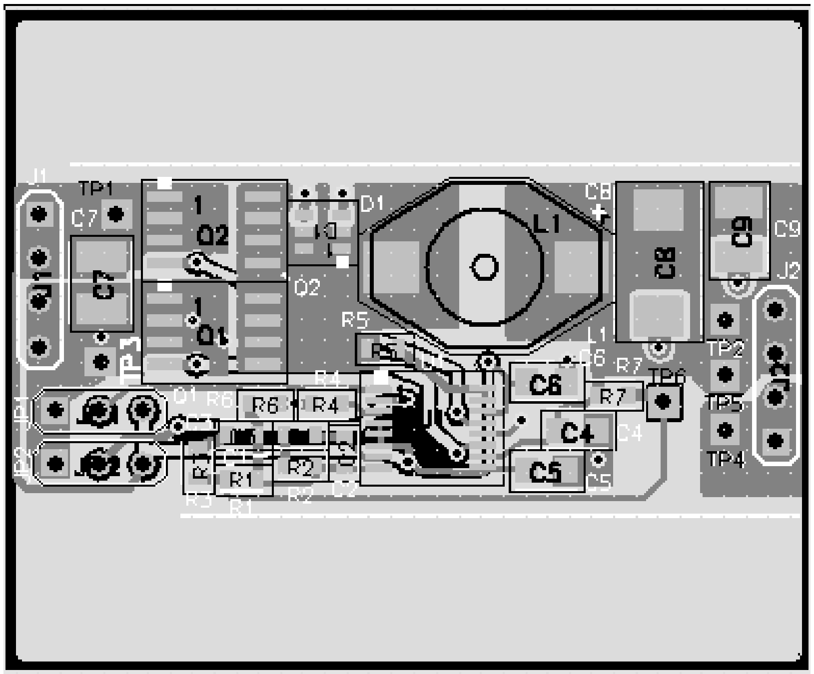

Figure 8. Top Side

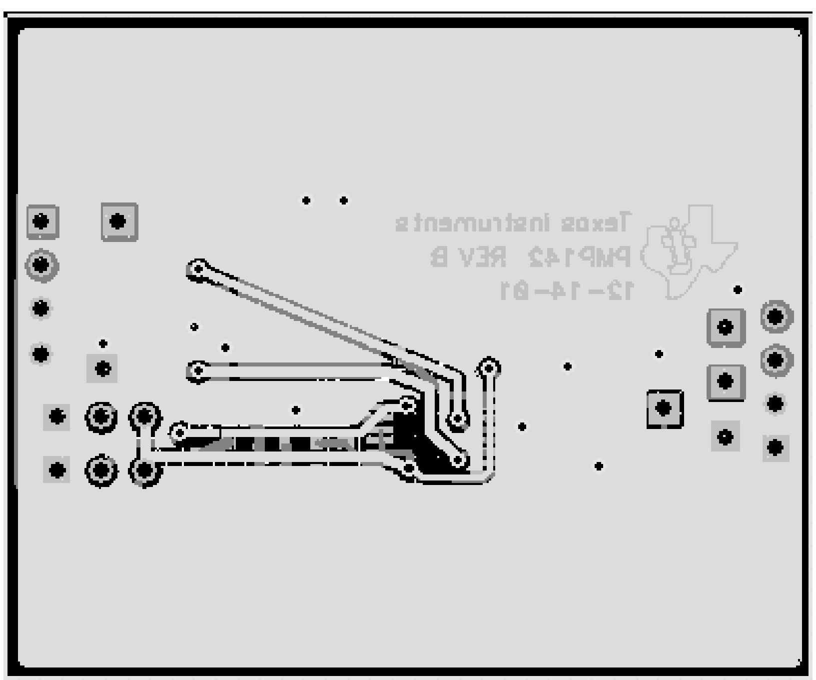

Figure 9. Bottom Side

5 Bill of Materials

Table 1 lists the board components and their values, which can be modified to meet the application requirements.

Table 1. Bill of Materials

REFERENCE DESIGNATOR	QTY	PART NUMBER	DESCRIPTION	MFG	SIZE
C1,C3	1	GRM1885C1H471J K	Capacitor, ceramic, 470 pF, 50 V, COG, 5%	Murata	603
C2	1	GRM1885C1H100J K	Capacitor, ceramic, 10 pF, 50 V, COG, 5%	Murata	603
C4,C5,C6	3	GRM219R71C474K K	Capacitor, ceramic, 0.47 µF, 16 V, X7R, 10%	Murata	805
C7,C9	2	JMK325BJ226MM	Capacitor, ceramic, 22 µF, 6.3 V, 20%	Taiyo-Yuden	1210
C8	1	EEFUD0D181R	Capacitor, 180 µF, 2.0 V, 18 mΩ, 20%	Panasonic	7343 (D)
D1	1	ZHCS2000	Diode, schottky, 2 A, 40 V	Zetex	SOT23–6
J1,J2	2	PTC36SAAN	Header, 4-pin, 100 mil spacing, (36-pin strip)	Sullins	0.100 x 4”
L1	1	U2PB–3R3	Inductor, SMT, 3.3 µH, 6.5 A, 15 mΩ	Cooper	13.8 X 10.4mm
R5	1	Std	Resistor, chip, 1 kΩ, 1/16-W, 1%	Std	603
R3	1	Std	Resistor, chip, 7.15 kΩ, 1/16–W, 1%	Std	603
R7	1	Std	Resistor, chip, 49.9 Ω, 1/16-W, 1%	Std	603
R1	1	Std	Resistor, chip, 100 kΩ, 1/16-W, 1%	Std	603
R4	1	Std	Resistor, chip, 127 kΩ, 1/16-W, 1%	Std	603
R6	1	Std	Resistor, chip, 196 kΩ, 1/16-W, 1%	Std	603
R2	1	Std	Resistor, chip, 100 kΩ, 1/16-W, 1%	Std	603
Q2	1	Si4403DY	MOSFET, P-channel, 1.8-V_{GS}, 9 A, 17 mΩ	Siliconix	SO–8
Q1	1	Si4866DY	MOSFET, N–channel, 2.5-V_{GS}, 17 A, 10 mΩ	Siliconix	SO–8
**U1	1	TPS43000PW	Multi–topology high-frequency PWM controller	Texas Instruments	TSSOP–16
TP1,TP2,TP3,TP4,TP5,TP6	6	240–333	Test point, black, 1 mm	Farnell	0.038”
N/A	1	PMP142	Printed circuit board, FR4, 0.032, SMOBC	any	

IMPORTANT NOTICE

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265