Application Report
SPRAC91A–May 2017–Revised July 2017

PRU-ICSS Migration Guide: AM335x to AM57x

Catalog Processors

ABSTRACT

This software migration guide assists in porting legacy software developed for the Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS) on AM335x to AM57x platforms.

Contents

1 Introduction 2
2 AM335x and AM57x Hardware Differences 2
3 Porting AM335x PRU Software to AM57x 8
4 References 9

List of Figures

1 AM335x PRU-ICSS Block Diagram 2
2 AM57x PRU-ICSS Block Diagram 3

List of Tables

1 PRU-ICSS Base Address Comparison for Global Memory Map 4
2 Constant Table Differences 4
3 INTC Event Differences 5
4 ARM Mapping of Source Interrupt to Event Number Comparison 7
5 PRU Firmware Checklist 8
6 ARM Code Checklist 8

Trademarks

1 Introduction

This document details the PRU subsystem hardware differences and outline software modifications required for porting PRU firmware and ARM code to AM57x.

For details about the PRU-ICSS on each device, see the PRU-ICSS chapter in the AM335x [1] and AM572x [2]/AM571x/AM570x [3] Technical Reference Manual for details about the PRU-ICSS on each device.

NOTE: The focus of this document is broad market support. Some industrial specific or ICSS features may be omitted.

2 AM335x and AM57x Hardware Differences

This section provides an overview of the hardware differences between AM335x and AM57x. Both a high-level overview of the SoC-level hardware differences and a detailed overview of the PRU-ICSS hardware differences are included.

2.1 SoC-Level Hardware Differences

AM335x and AM57x devices support different peripherals and features. The System-on-Chip (SoC) memory map, peripheral register map, pinmuxing, ARM interrupt controller events, and eDMA mapping also differ between the devices. For additional details, see the device-specific data sheets and user guides available at the device product pages:

- AM335x
- AM572x / AM571x / AM570x

2.2 PRU-ICSS Hardware Differences Between AM335x and AM57x

compares the PRU-ICSS hardware between AM335x and AM57x. One primary difference is that AM335x has one instance of the PRU-ICSS, while AM57x has two instances.

Figure 1 and Figure 2 show a comparison block diagram of the subsystems.

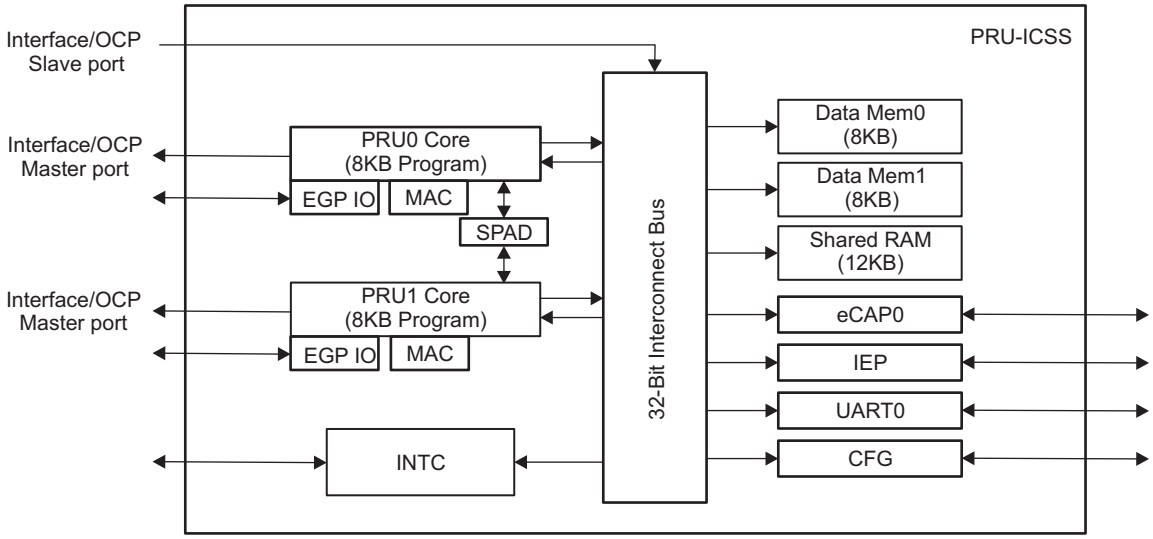

Figure 1. AM335x PRU-ICSS Block Diagram

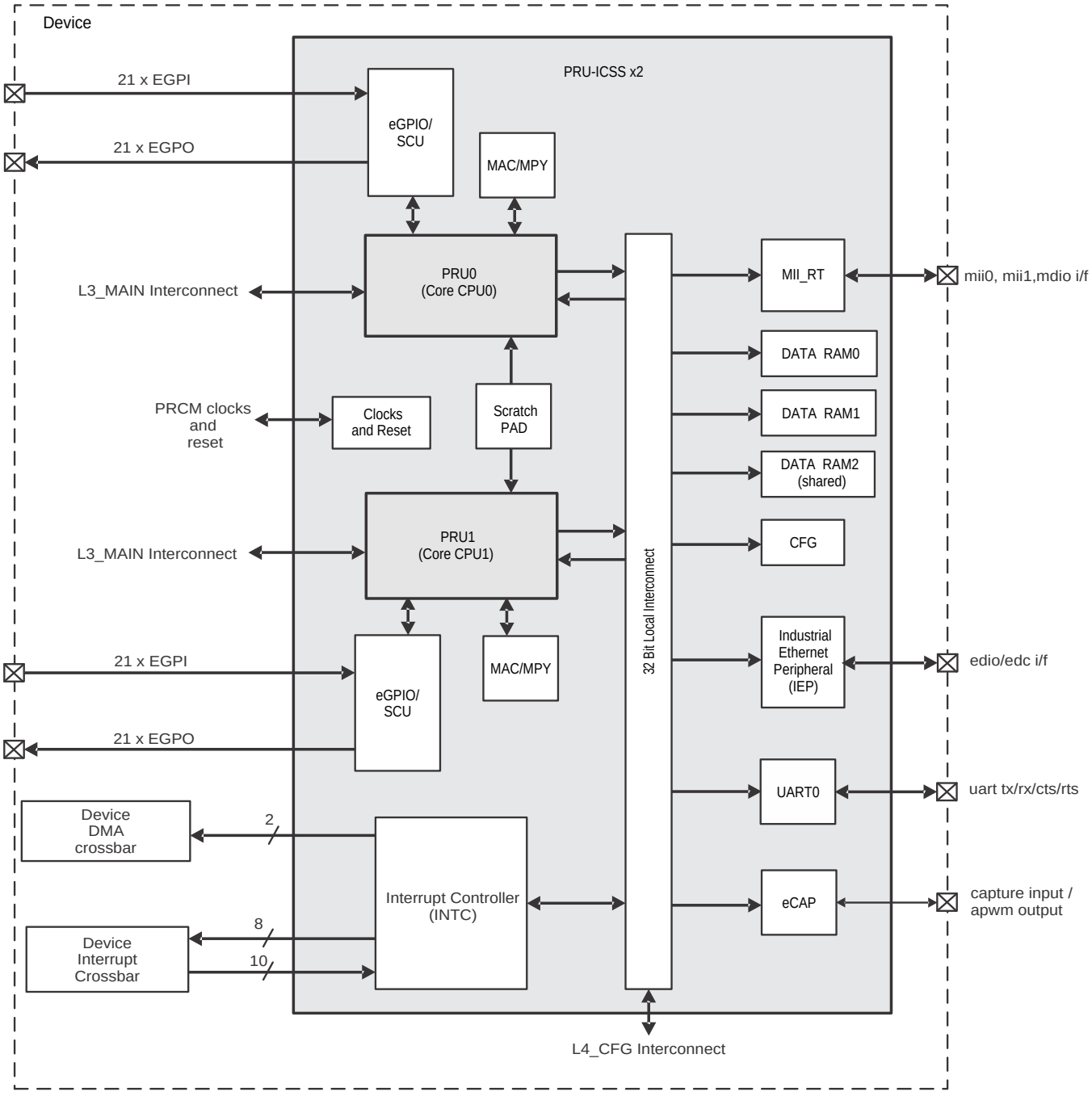

Figure 2. AM57x PRU-ICSS Block Diagram

2.2.1 PRU-ICSS Memory Map Comparison

2.2.1.1 Local and Global Memory Maps

The AM57x PRU-ICSS local and global memory maps are backwards compatible with AM335x. However, the PRU-ICSS base address within the SoC memory map differs between devices. Table 1 compares these base addresses, which function as the starting address for the PRU-ICSS global memory map.

Table 1. PRU-ICSS Base Address Comparison for Global Memory Map

	AM335x (PRU-ICSS1)	AM57x (PRU-ICSS1)	AM57x (PRU-ICSS2)
Start Address	0x5440_0000	0x4B20_0000	0x4B28_0000

2.2.1.2 PRU-ICSS Submodules Register Content and Offsets

The register content and offsets of the following PRU-ICSS submodules are identical on AM335x and AM57x:

- PRU-ICSS INTC
- PRU-ICSS PRU<n> Control
- PRU-ICSS PRU<n> Debug
- PRU-ICSS UART
- PRU-ICSS eCAP

The register content and offsets of the following PRU-ICSS submodules are identical on AM572x SR1.1 but are backwards compatible on AM572x SR2.0, AM571x, and AM570x (difference listed below):

- PRU-ICSS IEP (for more details, see Section 2.2.5.3)
- PRU-ICSS CFG
  - GPCFG0/1 register uses different bitfield to enable MII_RT mode
  - PIN_MX register adds PWM remap functionality

2.2.2 Constants Table Differences

The PRU-ICSS constant table entries are partially backwards compatible, see Table 2.

Table 2. Constant Table Differences

Entry No.	Value [31:0]	AM335x Function	AM57x Function
		PRU-ICSS1	PRU-ICSS1 / PRU-ICSS2
0	0x0002_0000	PRU-ICSS INTC (local)	PRU-ICSS INTC (local)
1	0x4804_0000	DMTIMER2	Reserved
2	0x4802_A000	I2C1	Reserved
3	0x0003_0000	PRU-ICSS eCAP (local)	IRQ_CROSSBAR_21 (MAILBOX1_IRQ_USER0)
4	0x0002_6000	PRU-ICSS CFG (local)	PRU-ICSS CFG (local)
5	0x4806_0000	MMCHS 0	I2C3
6	0x4803_0000	MCSPI 0	Reserved
7	0x0002_8000	PRU-ICSS UART0 (local)	PRU-ICSS UART0 (local)
8	0x4600_0000	McASP0 DMA	McASP3 DAT
9	0x4A10_0000	GEMAC	Reserved
10	0x4831_8000	Reserved	Reserved
11	0x4802_2000	UART1	Reserved
12	0x4802_4000	UART2	Reserved
13	0x4831_0000	Reserved	Reserved
14	0x481C_C000	DCAN0	Reserved

Table 2. Constant Table Differences (continued)

Entry No.	Value [31:0]	AM335x Function	AM57x Function
		PRU-ICSS1	PRU-ICSS1 / PRU-ICSS2
15	0x481D_0000	DCAN1	Reserved
16	0x481A_0000	MCSPI 1	Reserved
17	0x4819_C0000	I2C2	Reserved
18	0x4830_0000	eHRPWM1/eCAP1/eQEP1	Reserved
19	0x4830_2000	eHRPWM2/eCAP2/eQEP2	Reserved
20	0x4830_4000	eHRPWM3/eCAP3/eQEP3	Reserved
21	0x0003_2400	Reserved	Reserved
22	0x480C_8000	Mailbox 0	Reserved
23	0x480C_A000	Spinlock	Reserved
24	0x0000_0n00, n = c24_blk_index[3:0]	PRU-ICSS PRU0/1 Data RAM (local)	PRU-ICSS PRU0/1 Data RAM (local)
25	0x0000_2n00, n = c25_blk_index[3:0]	PRU-ICSS PRU1/0 Data RAM (local)	PRU-ICSS PRU1/0 Data RAM (local)
26	0x0002_En00, n = c26_blk_index[3:0]	PRU-ICSS IEP (local)	PRU-ICSS IEP (local)
27	0x0003_2n00, n = c27_blk_index[3:0]	Reserved	Reserved
28	0x00nn_nn00, nnnn = c28_pointer[15:0]	PRU-ICSS Shared RAM (local)	PRU-ICSS Shared RAM (local)
29	0x49nn_nn00, nnnn = c29_pointer[15:0]	TPCC	OCMC_RAM2_CBUF
30	0x40nn_nn00, nnnn = c30_pointer[15:0]	L3 OCMC0	OCMC_RAM
31	0x80nn_nn00, nnnn = c31_pointer[15:0]	EMIF0 DDR Base	EMIF1_SDRAM_CS0

2.2.3 PRU Module Interface to PRU I/Os Differences

The functionality and structure of R30 and R31 is preserved on AM57x. The supported GPI/GPO modes are backwards compatible. The number of PRU I/Os pinned out on each device differs, but the AM57x is backwards compatible with AM335x. The PRU-ICSS_Feature_Comparison table shows what I/Os are pinned out on each device.

2.2.4 Interrupt Controller Differences

The basic structure of the interrupt controller is the same in both devices. The basic INTC mapping of system events to channels to hosts is still the same. Both devices support the same number of total system events (64), channels (16), and hosts (10).

The INTC system events from modules inside the PRU-ICSS (System Event 0-31) are identical. The INTC system events from external sources (System Event 32-63) are not backwards compatible by default. However, AM57xx implements an Interrupt Controller Crossbar that provides flexibility in configuring the INTC system event source. At boot, the INTC can be configured to match the AM335x System Events. Table 2 shows which AM57xx IRQ_CROSSBAR events match the the AM335x external system events.

The ARM interrupt numbers mapped to the PRU-ICSS source interrupts have also been updated on AM57, see Table 3.

Table 3. INTC Event Differences

Event	AM335x Function	AM57x Function
	PRU-ICSS1	PRU-ICSS1 / PRU-ICSS2
63	TPCC (EDMA) - tpcc_int_pend_po1	IRQ_CROSSBAR_361 (EDMA_TPCC_IRQ_REGION0)
62	TPCC (EDMA) - tpcc_errint_pend_po	IRQ_CROSSBAR_359 (EDMA_TPCC_IRQ_ERR)
61	TPTC0 (EDMA) - tptc_erint_pend_po	IRQ_CROSSBAR_370

Table 3. INTC Event Differences (continued)

Event	AM335x Function	AM57x Function
	PRU-ICSS1	PRU-ICSS1 / PRU-ICSS2
		(EDMA_TC0_IRQ_ERR)
60	Mailbox0 - mail_u1_irq	IRQ_CROSSBAR_21 (MAILBOX1_IRQ_USER0)
59	Mailbox0 - mail_u2_irq	IRQ_CROSSBAR_135 (MAILBOX1_IRQ_USER1)
58	Debugss	N/A
57	GPIO0	IRQ_CROSSBAR_24 (GPIO1_IRQ_1)
56	eHRPWM0-2 Trip Zone	IRQ_CROSSBAR_204 (1) (PWMSS1_IRQ_ePWM0_TZINT)
55	McASP0 Tx	IRQ_CROSSBAR_104 (McASP1_IRQ_AXEVT)
54	McASP0 Rx	IRQ_CROSSBAR_103 (McASP1_IRQ_AREVT)
53	ADC_TSC	N/A
52	UART2	IRQ_CROSSBAR_69 (UART3_IRQ)
51	UART0	IRQ_CROSSBAR_67 (UART1_IRQ)
50	CPSW (c0_rx_thresh_pend)	IRQ_CROSSBAR_334 (GMAC_SW_IRQ_RX_THRESH_PULSE)
49	CPSW (c0_rx_pend)	IRQ_CROSSBAR_335 (GMAC_SW_IRQ_RX_PULSE)
48	CPSW (c0_tx_pend)	IRQ_CROSSBAR_336 (GMAC_SW_IRQ_TX_PULSE)
47	CPSW (c0_misc_pend)	IRQ_CROSSBAR_337 (GMAC_SW_IRQ_MISC_PULSE)
46	eHRPWM1	IRQ_CROSSBAR_208 (PWMSS2_IRQ_ePWM1INT)
45	eQEP0	IRQ_CROSSBAR_210 (PWMSS1_IRQ_eQEP0INT)
44	McSPI0	IRQ_CROSSBAR_60 (MCSPI1_IRQ)
43	eHRPWM0	IRQ_CROSSBAR_207 (PWMSS1_IRQ_ePWM0INT)
42	eCAP0	IRQ_CROSSBAR_213 (PWMSS1_IRQ_eCAP0INT)
41	I2C0	IRQ_CROSSBAR_51 (I2C1_IRQ)
40	DCAN0 (dcan_intr)	IRQ_CROSSBAR_222 (DCAN1_IRQ_INT0)
39	DCAN0 (dcan_int1)	IRQ_CROSSBAR_223 (DCAN1_IRQ_INT1)
38	DCAN0 (dcan_uerr)	IRQ_CROSSBAR_224 (DCAN1_IRQ_PARITY)
37	eHRPWM2	IRQ_CROSSBAR_209

Table 3. INTC Event Differences (continued)

Event	AM335x Function	AM57x Function
	PRU-ICSS1	PRU-ICSS1 / PRU-ICSS2
		(PWMSS3_IRQ_ePWM2INT)
36	eCAP2	IRQ_CROSSBAR_215 (PWMSS3_IRQ_eCAP2INT)
35	eCAP1	IRQ_CROSSBAR_214 (PWMSS2_IRQ_eCAP1INT)
34	McASP1 RX	IRQ_CROSSBAR_148 (McASP2_IRQ_AREVT)
33	McASP1 TX	IRQ_CROSSBAR_149 (McASP2_IRQ_AXEVT)
32	UART1	IRQ_CROSSBAR_68 (UART2_IRQ)

(1) Note that the AM335x PWM TZ event is associated with three PWM instances (PWM0-2), but the AM57xx event is only associated with one PWM instance.

Table 4. ARM Mapping of Source Interrupt to Event Number Comparison

Source	AM335x Event Number	AM57x Event Number	
	PRU-ICSS1	PRU-ICSS1	PRU-ICSS2
PRU_ICSS<k>_EVTOUT0	20	186	196
PRU_ICSS<k>_EVTOUT1	21	187	197
PRU_ICSS<k>_EVTOUT2	22	188	198
PRU_ICSS<k>_EVTOUT3	23	189	199
PRU_ICSS<k>_EVTOUT4	24	190	200
PRU_ICSS<k>_EVTOUT5	25	191	201
PRU_ICSS<k>_EVTOUT6	26	192	202
PRU_ICSS<k>_EVTOUT7	27	193	203

2.2.5 Peripheral Differences

2.2.5.1 PRU-ICSS UART

The PRU-ICSS UART is identical on AM335x and AM57x.

2.2.5.2 PRU-ICSS eCAP

The PRU-ICSS eCAP is identical on AM335x and AM57x. However, AM57x implements debug suspend for the PRU-ICSS eCAP. To run the PRU-ICSS eCAP during emulation suspend, the ECCTL1 register's FREE_SOFT bit will need to be configured.

2.2.5.3 PR-ICSS Industrial Ethernet Peripheral (IEP)

The PRU-ICSS IEP is identical on AM335x and AM572x SR1.1, but backwards compatible on AM335x, AM572x SR2.0, AM571x, and AM570x.

AM572x SR2.0, AM571x, and AM570x implement a 64-bit IEP Timer, where the AM335x IEP Timer is 32-bit. The AM572x 2.0, AM571x, and AM570x IEP Timer also supports more compare registers (16 on AM572x SR2.0 / AM571x / AM570x vs 8 on AM335x) and adds support for a programmable reset value within the IEP_TMR_CNT_RST register.

2.2.6 Instruction Set and Format Compatibility

The instruction set and format on AM57x is identical with AM335x.

3 Porting AM335x PRU Software to AM57x

The software changes required to port legacy code from AM335x to AM57x are based on the hardware differences between the two devices. This section details the key differences in software and describes how legacy code can be modified for the AM57x PRU-ICSS. Note that additional modifications may be required relating to other SoC differences that are external to the PRU-ICSS. Some of these modifications are discussed in the modifying software for SoC related differences section.

A checklist of changes required for both legacy PRU firmware and ARM code is provided in Table 5 and Table 6.

Table 5. PRU Firmware Checklist

1	PRU addresses within global memory map
2	PRU INTC system event numbers
3	PRU IEP registers
4	PRU constant table values
5	SoC related changes (peripheral addressing or registers, and so forth)

Table 6. ARM Code Checklist

1	PRU addresses within global memory map
2	PRU INTC system event numbers
3	SoC related changes (peripheral addressing or registers, pinmux configuration, ARM Interrupt Controller, and so forth)

3.1 Updating Global Memory Map References

When porting the legacy software to AM57x, the PRU-ICSS base address needs to be udpated in both the PRU firmware and ARM code. Note that most PRU firmware code should use the local memory map to reduce latencies and would not require any modification. Only firmware that accesses the global memory map requires updates. No change is required for any offsets within the PRU-ICSS global memory map.

3.2 Configuring PRU INTC System Events

AM57xx implements an Interrupt Controller Crossbar that provides flexibility in configuring the INTC system event source. At boot, the PRU INTC can be configured to match the AM335x System Events. This pre-configuration step can be placed in the ARM or PRU code.

3.3 Updating PRU IEP Registers

For AM572x SR2.0, AM571x, and AM570x, the IEP Timer register offsets needs to be updated. (The 64-bit IEP Timer feature of these AM57x devices breaks register offset compatibility with AM335x's 32-bit IEP Timer).

For AM572x SR1.1, no software change is required for the IEP Timer register offsets.

3.4 Updating PRU Constant Table References

Differences in the PRU constant table require changes to the PRU firmware code.

The PRU constant table entries are partially backwards compatible, as some peripherals and features maintain the same entry numbers. However, other peripherals and features have been removed, added, or remapped to different entry numbers in the AM57x table.

For a comparison between the constant tables on both devices, see Section 2.2.2.

3.5 Modifying Software for SoC Related Differences

AM335x and AM57x devices have additional differences at the SoC level that also require changes in both PRU firmware and ARM code. Below is a list of some key differences that require code updates. However, this is not an exhaustive list.

Key differences between AM335x and AM57x devices require PRU legacy code updates include:

- Global device memory map
  - Start addresses of peripherals and features
  - Base addresses of modules
  - Register addresses and offsets
- Peripherals
  - For peripherals supported on each device, see .
  - Peripherals may have new memory or register maps. The functionality of registers may also change.
- Pinmuxing

4 References

1. *AM3358*
2. *AM572x Sitara™ Processors Silicon Revision 2.0, 1.1 Technical Reference Manual*
3. *AM571x (SR2.0, SR1.0) and AM570x (SR2.0) Sitara™ Processors Technical Reference Manual*
4. AM3358
5. *AM5728*
6. *AM5718*
7. *AM570x*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2017) to A Revision	Page
• Update was made in Section 1.	2
• Updates were made in Section 2.1.	2
• Figure 2 was updated.	2
• Updates were made in Section 2.2.1.2.	4
• Updates were made in Section 2.2.5.3.	7
• Update was made in Section 3.3.	8
• Added information to Section 4.	9

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265