Application Report
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Calculating Useful Lifetimes of Embedded Processors

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ABSTRACT

This application report provides a methodology for calculating the useful lifetime of TI embedded processors (EP) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

Contents

List of Figures

List of Tables

1 Introduction

This document introduces the three stages of reliability and shows the current generation of TI industrial grade EP product is designed to support a useful lifetime of 10 year operating at 105°C junction temperature (T_J).

Based on the physics of failure approach, it shows useful life scales with temperature and decreasing the effective temperature below 105°C T_J, can extend the useful lifetime of the silicon beyond 10 years. Similarly, increasing the effective temperature above the 105°C T_J will shorten lifetime.

Using a case study of an actual system level mission profile, it shows how to calculate if the EP will be operating within its target useful lifetime for which it was designed.

2 Stages of Reliability and Useful Life Period

When considering 'reliability', three phases of lifetimes are considered:

- Early life – declining failure rate where failures are due to random defects.
- Useful life – the steady state period where failure rate is relatively constant.
- Wear-out – stage where end of life mechanisms start to occur and failure rate increases.

Figure 1 illustrates this as a “bathtub curve” profile where the edges of the curves reflect the shape of a bath.

The focus of electronics reliability is the useful life period and also referred to as steady-state period where it is expressed in Failure in Time (FIT): # of failures/109 hours.

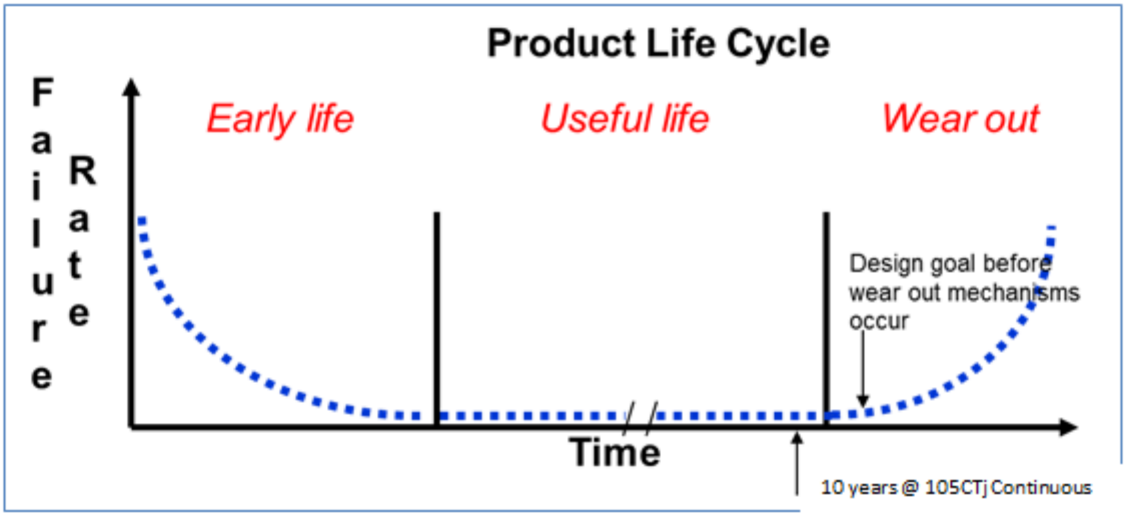

Figure 1. Bathtub Curve Showing Different Stages of Reliability

Many industrial systems require useful lifetimes of 10 years or less but recent examples of reliability profiles modeled by TI that go above that include:

- Telecommunication equipment: 15 years continuous operation
- Industrial controllers in factory electrical supply system: 15 years continuous operation
- Solar invertor: 15 years continuous operation
- Water meter: 15 years continuous operation
- Electronic Meter: 20 years continuous operation

3 CMOS Wear Out Mechanisms and IC Design

The current generation of TI industrial grade embedded processor products is designed to support a useful lifetime of 10 year operating at 105°C junction temperature T_J.

The 10 year lifetime assumes a worst case situation of 100% powered on and run at a constant 105°C T_J temperature.

TI EP products are designed for reliability so that the onset of the wear out mechanisms occurs beyond the useful life period. This is illustrated in Figure 1.

Robustness to prominent silicon wear-out mechanisms that are designed for include:

- Gate oxide integrity (GOI)
- Electro-migration (EM)
- Time dependent di-electric breakdown (TDDB)

In addition, mechanisms that cause parametric shift over lifetime, such as Negative Bias Temperature Instability (NBTI) and Channel Hot Carriers (CHC), are also considered within the product design.

For most silicon technologies, the critical wear out mechanism is EM.

Figure 2 shows how the onset of EM changes with T_J on a TI proprietary silicon node. Note that EM performance may differ per technology but the principle of fail rate vs temperature will apply: running at temperature extremes for long durations above 105°C will shorten the lifetime.

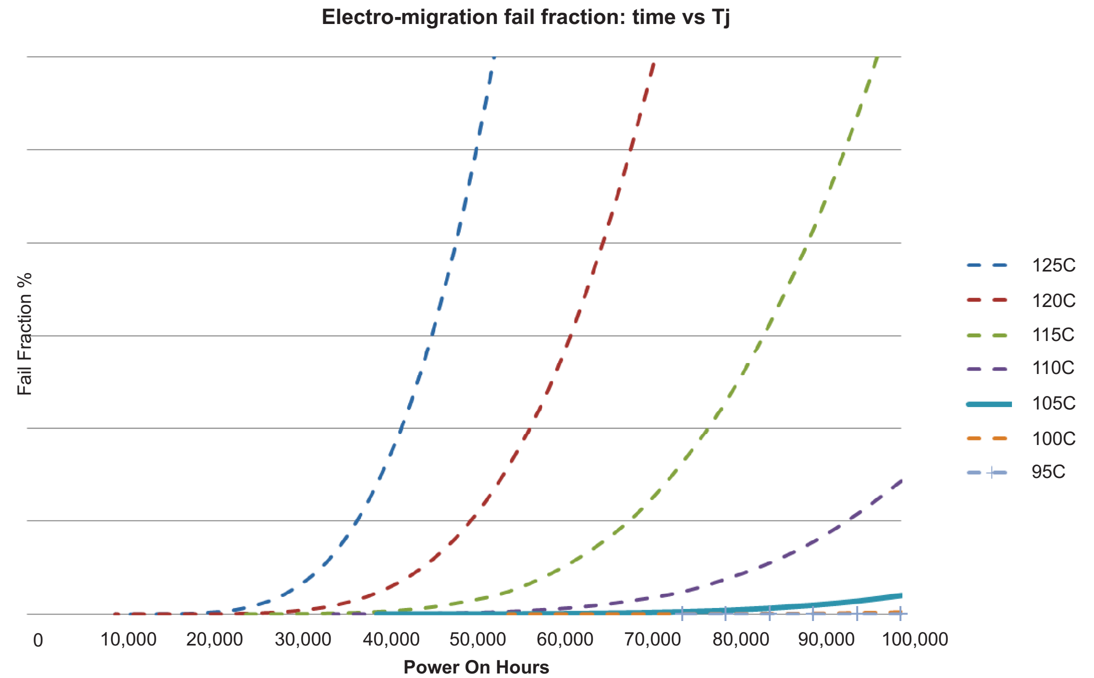

Figure 2. Impact of Electro-Migration on a TI Embedded Processor Over Temperature

4 Reliability and Temperature

Assuming the device is operating within the specified data sheet voltage, the critical variable influencing silicon lifetime under electrical bias is the junction temperature (T_J) of the silicon.

An often quoted rule of thumb in electronics reliability for capacitors is that every 10°C increase, the lifetime approximately halves. For semiconductors, it is a similar change but there is slippage at higher temperatures.

Because of this, it is recommended looking at two situations of power on conditions: at or below 105°C and above 105°C.

4.1 Operating Below 105°C T_J

When operating at 105°C T_J or below, apply the Arrhenius equation to determine the accelerating factor (AF) (see Figure 3).

$$AF = \exp\left(\frac{Ea}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right)$$

Figure 3. Arrhenius Equation

Where,

AF = Acceleration factor

Ea = Activation energy in eV

k = Boltzmann's' constant (8.63 x 10-5 eV/K)

Tuse = Use temperature in K (C + 273)

Tstress = Stress temperature in K (C+273)

Figure 4 plots the AFs for every 5°C below 105°C using a thermal activation energy Ea of 0.7eV (a common Ea for assessing silicon reliability).

It shows that if the processor runs at 90°C effective temperature instead of the 105°C, x2 increase is useful lifetime can be projected. In other words, a 20 year useful lifetime of the silicon can be achieved provided the application manages the thermal performance to be at an 'effective' T_J of 90°C or below.

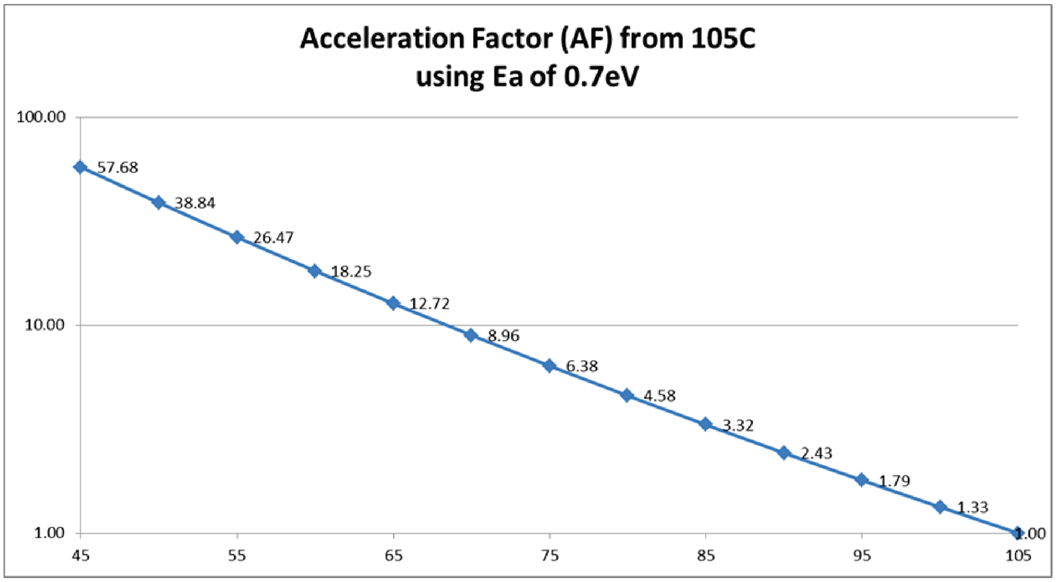

Figure 4. Acceleration Factor (AF) From 105°C

4.2 *Operating Above 105°C T_J*

For extended temperature devices rated above 105°C T_J, Figure 2 showed that running hotter temperatures shortens lifetime.

To facilitate a high-level calculation that does not involve a complex calculation of wear out mechanisms, Table 1 shows a guard banded AF for situations 105°C.

Table 1. Table 1. De-Rating Above 105°C T_J

Temperature	Acceleration Factor
105°C	1.00
110°C	0.50
115°C	0.40
120°C	0.30
125°C	0.20

Table 1 shows that if the embedded processor designed to 10 years and 105°C T_J is instead operated continuously at 125°C T_J, then 2 years useful life should be its reliability budget.

NOTE: The guard banded AF is sufficient to satisfy for most applications. If more precise modeling is required for extended temperature applications, contact TI for reliability assistance.

NOTE: For automotive grade products that are specified above 105°C T_J, their reliability mission profile is targeted for an AEC-Q100 mission profile of 15 years on with ~12% duty cycle. The total time at T_{max} is usually a small subset of their total power on time.

5 Assessing a System Mission Profile

It is rare that an application runs 100% at one temperature. More practical situations run at a distributed temperature ranges over its lifetime. The mapping of Temperature vs time for an application is known as a *mission profile*.

In most cases, the mission profile imparts a time on vs time off, known as a duty cycle. The duty cycle has importance in that power off stops the clock for the reliability mechanisms that require bias (traditional CMOS wear out).

Figure 5 shows a real life example of a mission profile for a solar invertor application which required a 15 year useful lifetime with 100% on time. In this example, the delta between T_A and T_J was 20°C. To calculate the Junction temperature from ambient or case temperatures, see the device-specific data sheet.

The end result showed that the mission profile would subject the EP to be running at an equivalent to 3.4 years @ 105°C T_J and comfortably within the 10 years @ 105°C T_J that it was designed for.

Solar Invertor Profile

1. Convert days to Power on Hours/ year

2. PoH / year x years x duty cycle

3. convert Ta -> Tj (+20C in this example but will vary per device)

4. Derating from 105C Tj to actual Tj - see table below

5. Calculate PoH per Tj interval x AF

CUSTOMER MISSION PROFILE

LIFETIME 15 YEARS

DUTY CYCLE : 100% ON

Days/year	Ambient temperature	PoH / yr	**Total PoH**		**Tj**	**AF from 105C ***	**Equiv to 105C Tj hrs**	
15	+30° C	360	5400		50	38.84	139	
25	+45° C	600	9000		65	12.72	708	
90	+55° C	2160	32400		75	6.38	5,078	
185	+60° C	4440	66600		80	4.58	14,541	
35	+70° C	840	12600		90	2.43	5,185	
15	+80° C	360	5400		100	1.33	4,060	
		8,760	**131,400**	hrs			**29,712**	**hours**
							3.4	**Years**

*Derating 105C to lower temperatures

Temperature	Acceleration Factor using 0.7eV
45	57.68
50	38.84
55	26.47
60	18.25
65	12.72
70	8.96
75	6.38
80	4.58
85	3.32
90	2.43
95	1.79
100	1.33
105	**1.00**

Summary: The customer profile is equivalent to 3.4 years @ 105C Tj.

Since it was designed to have 10 years @ 105C Tj lifetime, It will still be operating within its useful lifetime (ie/ it has only consumed 34% of it's useful lifetime).

Figure 5. Example of Assessing a System Level Mission Profile and Component Reliability

6 Useful Life and MTTF Values

There may be confusion in useful lifetime and mean time to failure (MTTF) values, but they refer to different aspects of reliability.

The useful life calculations shown here assess if the component will outlast the system reliability requirement. With respect to end industries, the longest requirement for system useful life TI modeled was 20 years useful life for metering applications. (In such outdoor applications, the ambient temperatures assisted in lowering the effective temperatures.)

MTTF on the other hand, is a projection of when the arithmetic mean time between failures of the whole population where it is an inverse of the FIT rate. The MTTF is orders of magnitudes higher than the useful life.

7 Limitations of This Document

- Not all TI's embedded products support a 10 year and 105°C T_J useful life. Devices with limited POH/useful life will specifiy this in their device-specific data sheets.
- The reliability discussed in this document is limited to semiconductor reliability under power on conditions only (silicon lifetime). It does not include assessment of package reliability conditions, which needs separate reliability assessments.
- Data retention periods of non-volatile memory are not considered in this application report. For more information regarding these values, see the device-specific data sheets.

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