UCD3138 Family - Practical Design Guideline

Application Report

Literature Number: SLUA779A
August 2016–Revised January 2017

Contents

List of Figures

Introduction

Sean Xu

There are multiple grounds and bias power pins for a digital controller, such as the UCD3138 family products. They are separated from each other because of the digital circuitry and analog circuitry inside the device. Normally, digital circuit draws more current and generates more noise, but the digital signal is not sensitive to the noise; while the analog circuit needs a quiet power and grounding. A deliberate grounding and power separation outside the controller can reduce the interference between analog circuit and digital circuit, and therefore, the controller can have better performance. When they are separated from each other, take care of how the analog circuit and digital circuit are grouped, respectively, and then how and where they are tied together. With improper grounding, the device performance can be negatively impacted including DPWM abnormal, device reset, ADC results, output voltage ripple, and so on.

In the PCB design, there are two options. One is to have two separate grounds - digital ground and analog ground. The other is to use a single ground plane for both digital ground and analog ground. With two separate ground planes, how to connect digital ground and analog ground is very important, and the PCB must be designed very carefully. With a single ground plane, there is no concern regarding where two grounds are tied together, and it makes the PCB design easier. Here, TI recommends using a single ground plane.

In this document, digital ground is denoted as DGND; analog ground is denoted as AGND; a single ground plane is denoted as SGND. This document covers the UCD3138 family including non-A version UCD family, for example, UCD3138, UCD3138064, and UCD3138128; and A version-UCD family, for example, UCD3138A, UCD3138064A, and UCD3138128A.

UCD3138 Pin Connection Recommendation

The UCD3138 device is a highly integrated controller with a large number of mixed signals. It is important to group each pin, select good components, have appropriate connections to each pin, and make good component placement on the PCB to reduce noise coupling and to prevent chip mal-function. First, group all digital circuitry and analog circuitry. Second, place digital circuitry close to each other, place analog circuitry close to each other, and then make connections among them by a solid plane. To achieve a robust design, TI recommend's at least a 4-layer board.

Next, layout considerations and examples are provided for some critical pins or signals.

2.1 $\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ pin must have one at least 2.2-µF low ESL capacitor locally decoupled with DGND plane or SGND plane. As shown in Figure 2-1, this capacitor must be placed very close to the device $\overline{\text{RESET}}$ pin. TI highly recommends using a small resistance (such as 220 Ω) to connect the $\overline{\text{RESET}}$ pin (pin 11 for UCD3138RGC) with V33DIO (pin 9 for UCD3138RGC). The resistor must be placed close to the $\overline{\text{RESET}}$ pin, as well. The grounding point of the capacitor must be tied to DGND plane or SGND plane locally by a ground via, which is generally larger than a signal via.

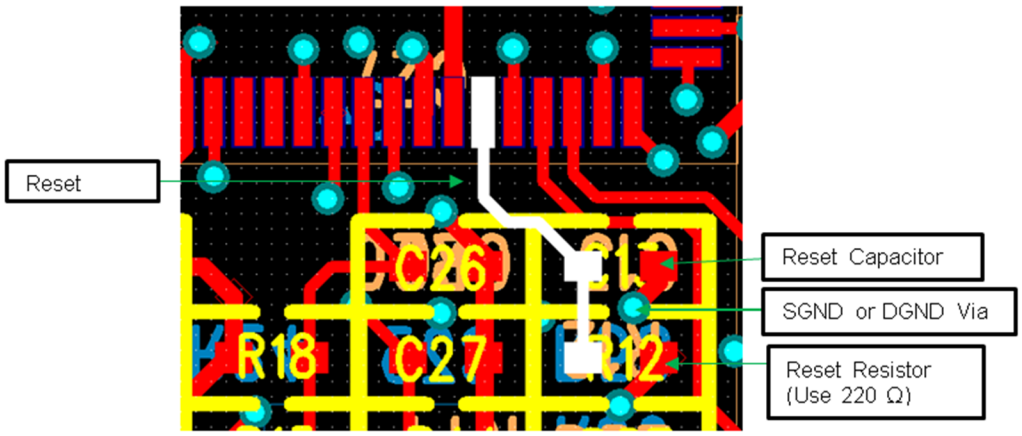


Figure 2-1. $\overline{\text{RESET}}$ Pin Connection

2.2 ADC Pins

Use low ESL and ESR ceramic capacitors on ADC pins to decouple with AGND or SGND. The capacitor value is selected such that the cut-off frequency is at least one tenth the sampling frequency if there is no dynamic requirement. This can help reduce noise coupled during signal transmission.

ADC input is a single-ended signal. If the sensing trace is long, move it away from radiation sources and add ground shielding between the signal and radiation sources. If there exists a resistor between signal output and ADC input, the resistor should be located close to the ADC pin. The resistance needs to be less than 1 kΩ.

For example, the sampling frequency is 10 kHz. The cut off frequency of LPF is 1 kHz. With a 1-kΩ equivalent resistor, select a 0.15-µF capacitor.

2.3 EAP and EAN Pins

There are three front-end ADCs to sense the feedback signals in the UCD family. These ADCs are dual-ended sensing input circuitry with good common mode noise rejection. Keep the distance between the two traces as short as possible when the differential sensing method is used. A local filter close to the EAP and EAN pins is required as shown in Figure 2-2. Because EAP and EAN are used for feedback loop, C must be selected from the range of 100 pF to 1000 pF. R is preferred to use low resistance.

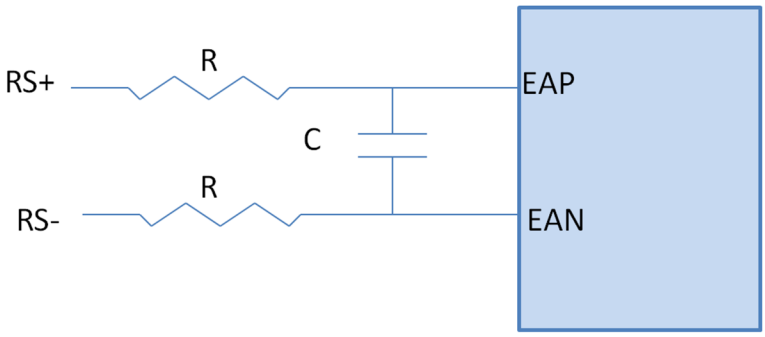


Figure 2-2. Local Filter on EAPx and EANx Pins

2.4 Current Amplifier With EADC Connection

As shown in Figure 2-3, if a current amplifier is used for current sensing, it is referenced to AGND. If there are separate AGND and DGND, and then is followed by a local low-pass filter (LPF), LPF should be placed close to the EAP and EAN pins of the UCD device. If a single plane is used, both filters must be connected to the same ground plane (SGND).

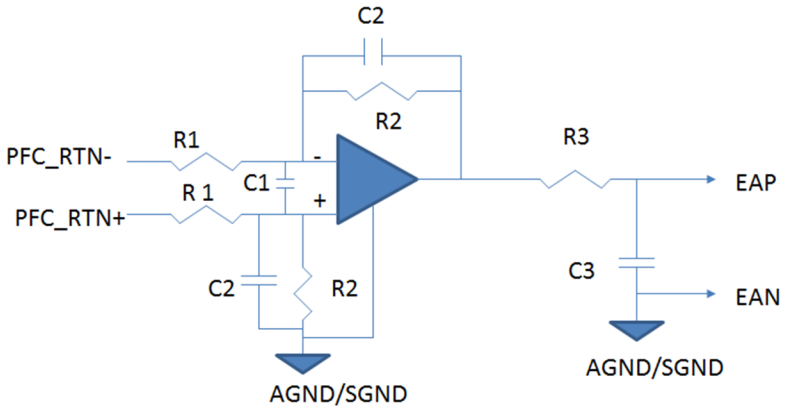


Figure 2-3. Current Amplifier Connected With EADC

2.5 UART Communication Port

UART is used for communicating between the primary side and secondary side with isolation boundary. Normally, the communication wires are long. These wires can easily be interfered by EMI and pick up noise of switching power supplies. First, the wires must be routed without directly exposing the traces to the switching noise source, and then a termination is needed at the end of the trace, as shown in Figure 2-4. For example, R = 50 Ω, C = 47 pF if they don't significantly slow down the slew rate of the signals. When the pins are not used, tie them to a single ground plane SGND or DGND if there are two separate ground planes.

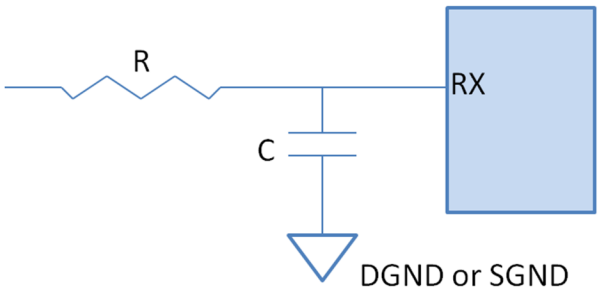


Figure 2-4. Termination for Communication Port (UART)

2.6 DPWM PINS

If DPWMs travel for a longer distance than 3 inches from the control card to a main power stage, a Schottky clamping diode may be needed as shown in Figure 2-5 to prevent electrical overstress on the device during lightning test. The long trace may also pick up the noise from other switching sources. Avoid DPWM signals to cross switching nodes. DPWM is referenced to DGND or SGND.

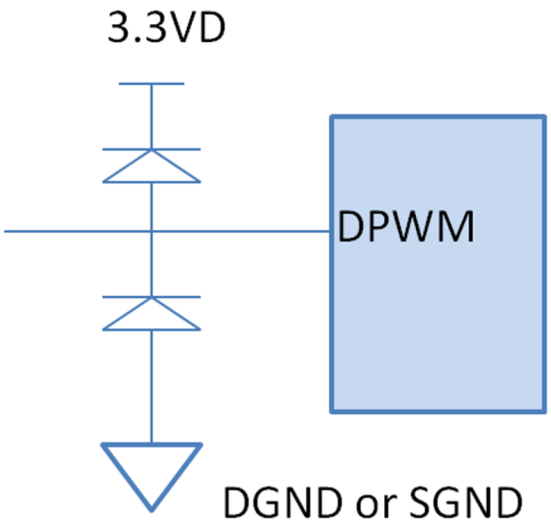


Figure 2-5. Clamping Diodes for DPWM

2.7 GPIOS

GPIO is referenced to DGND internally. When GPIO pins are not used (ensure they stay at or are configured as input pins), connect the pins to DGND and SGND. Alternatively, they can be configured as output pins and set as low in the firmware. When GPIOs are used to drive other circuit like LED, be aware that traces can pick up noise. A local resistor close to the signal receiver (like LED) is used to terminate the coupled noise. If the big voltage swings, clamping diodes are needed for GPIO inputs, as shown in Figure 2-6.

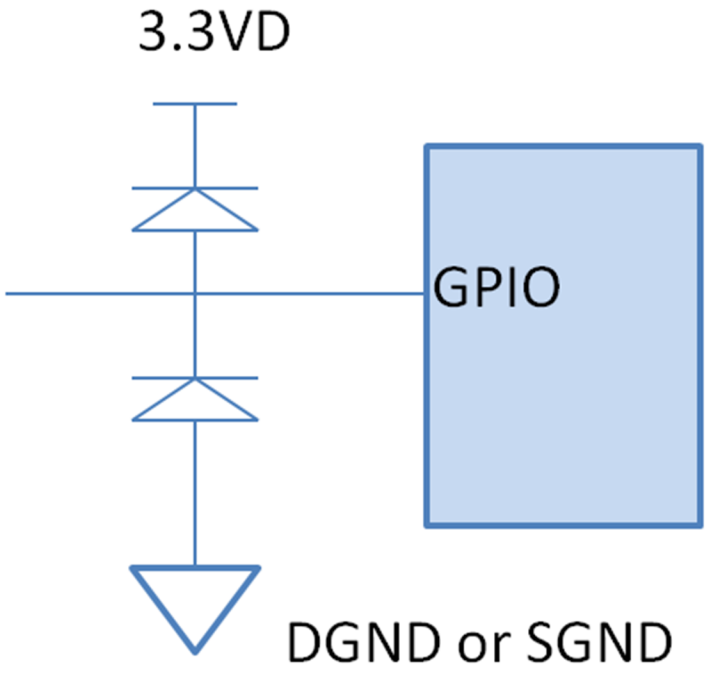


Figure 2-6. Clamping Diodes for GPIO

2.8 Bias Supply and Grounding

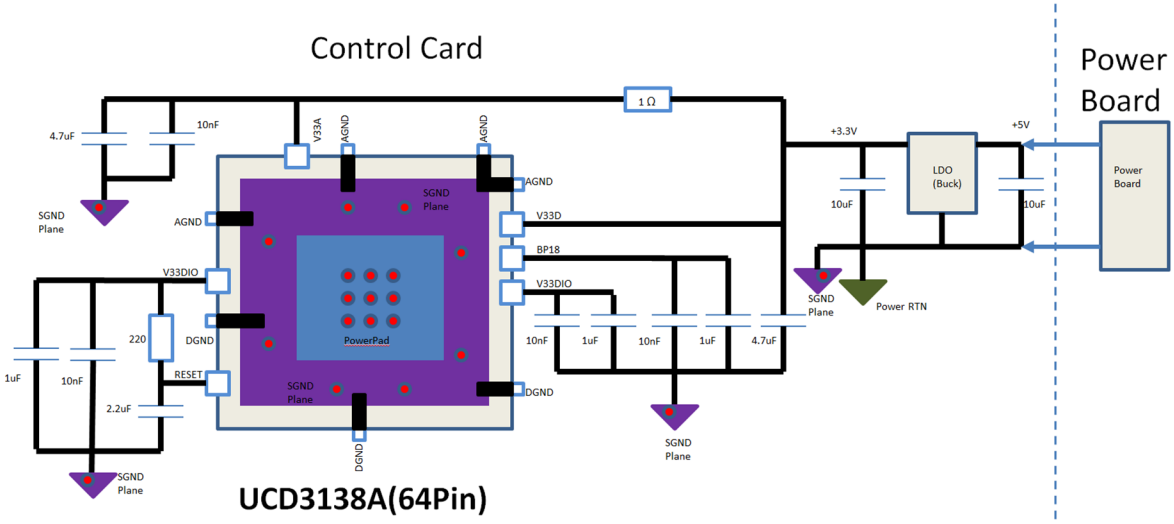


Figure 2-7. 3.3-V and Ground Connection Diagram for UCD3138A (64-Pin)

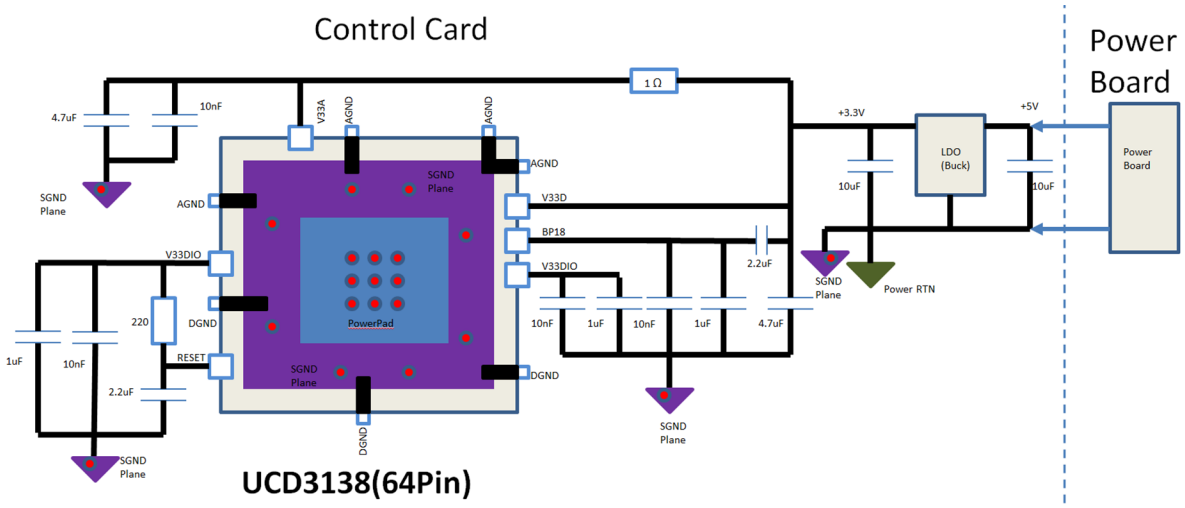


Figure 2-8. 3.3-V and Ground Connection Diagram for UCD3138 (64-Pin)

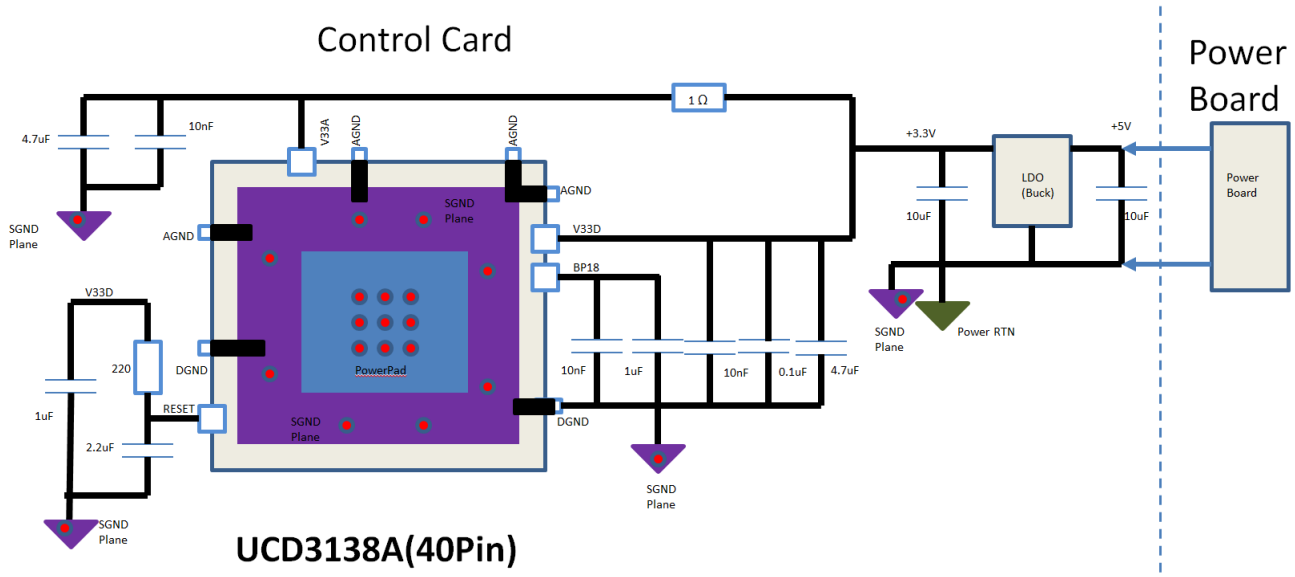


Figure 2-9. 3.3-V and Ground Connection Diagram for UCD3138A (40-Pin)

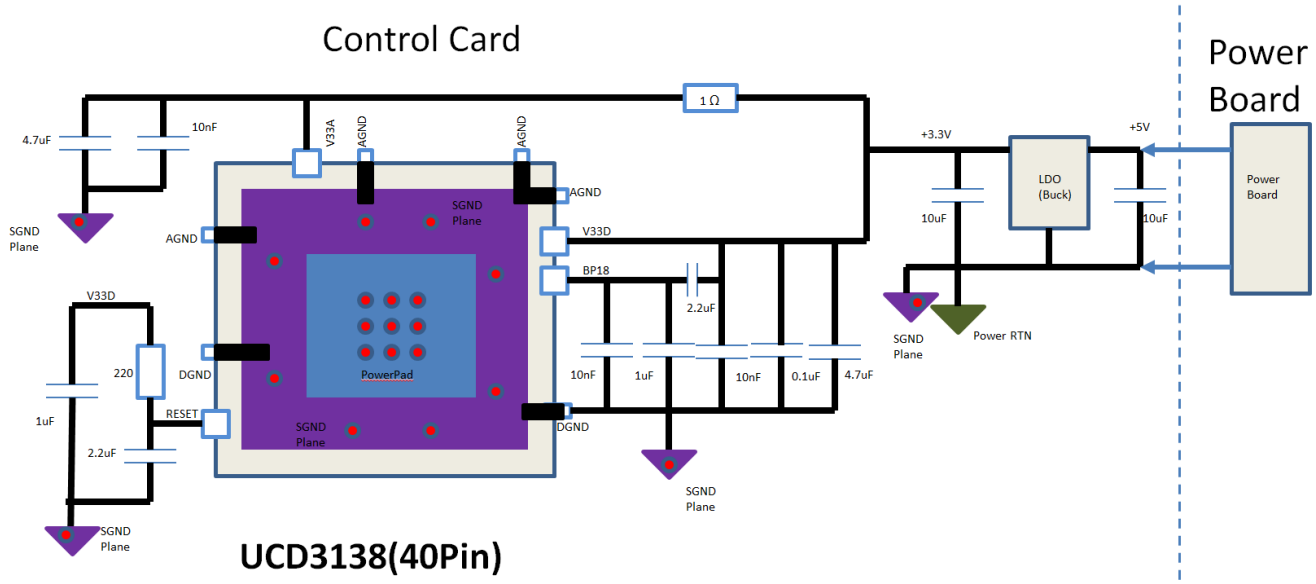


Figure 2-10. 3.3-V and Ground Connection Diagram for UCD3138 (40-Pin)_change

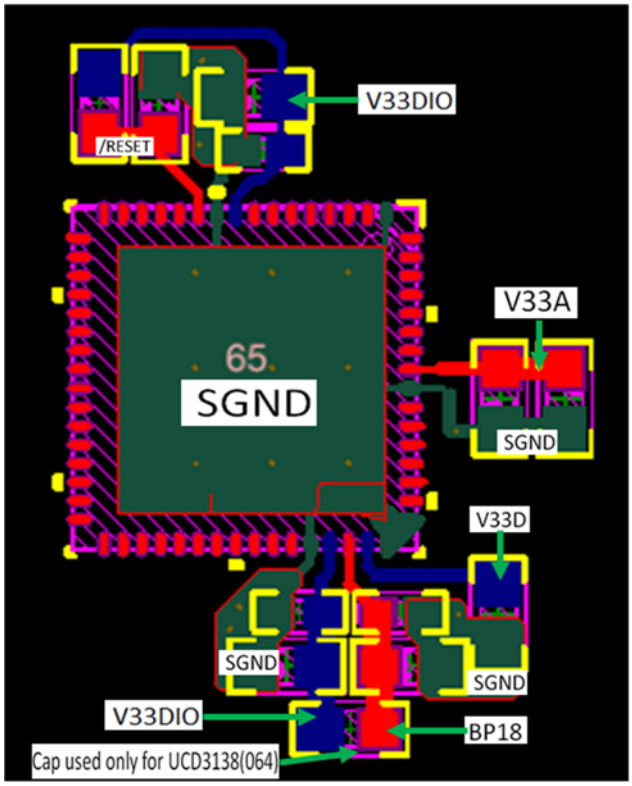
A +3.3-V bias normally is produced by a LDO or Buck converter. Figure 2-7 and Figure 2-8 are simplified block diagrams of the UCD3138RGC A and non-A devices (64-pin) to depict how the pins are connected. Figure 2-9 and Figure 2-10 are simplified block diagrams of the UCD3138A and non-A devices (40-pin) to depict how the pins are connected. +5 V or +12 V normally are generated by a flyback converter, and it is referenced to the Power Return. A 10-µF capacitor is locally used for LDO or buck between +3.3 V and Power Return. From there, use a single plane (SGND) for both digital ground and analog ground. A 1-Ω resistor is needed between V33D and V33A. As an example, a 4.7-µF decoupling capacitor is used for V33A and V33D respectively, and these decoupling capacitors must be placed close to the device pins. In addition, a 10-nF capacitor is used for V33A and V33D respectively to filter out the high frequency noise. One 1-µF decoupling capacitor is used for each V33DIO. If DGND and AGND are separated, then the decoupling capacitor of V33A must be connected to AGND, and the decoupling capacitor of V33D should be connected to DGND. A small current return loop is important to reduce return impedance. There must not be any voltage level shift between the internal DGND and internal AGND. Multiple vias are required to connect the extended power pad (that is, copper plane under the device power pad) to the internal single ground (SGND) plane layer. All digital or analog ground pins can be directly connected to the extended power pad or connected to the internal SGND plane through vias. If DGND and AGND planes are separated, extended power pad needs to be connected to AGND plane. The pins of V33D and V33DIO should be connected externally.

2.9 BP18

Paralleled 1-µF and 10-nF capacitors are used between BP18 and SGND or DGND if DGND and SGND are separated, as shown in Figure 2-8. TI also recommends having a 2.2-µF decoupling capacitor between V33D to BP18 for UCD family non-A version, for example, UCD3138 and UCD3138064. The 2.2 uF helps BP18 ramp up at the same time as V33D ramp up. The internal logic level shifter is powered on to eliminate initial pulses on GPIO pins. The caps must be placed close to the device pins, and keep the return loop as small as possible. For all A-version devices and UCD3138128, there is no need for this 2.2 µF between V33D and BP18 due to internal circuit enhancement which eliminates the GPIO short pulses during V33D ramp up.

2.10 Layout Example for UCD3138ARGC by Using a Single Ground

Figure 2-11 to Figure 2-16 are layout examples of device supplies and ground for UCD3138 families. In these examples, a single ground (SGND) is used.



Note: V33D and V33DIO are connected to the same net

Figure 2-11. Layout Example for UCD3138ARGC on Top Layer

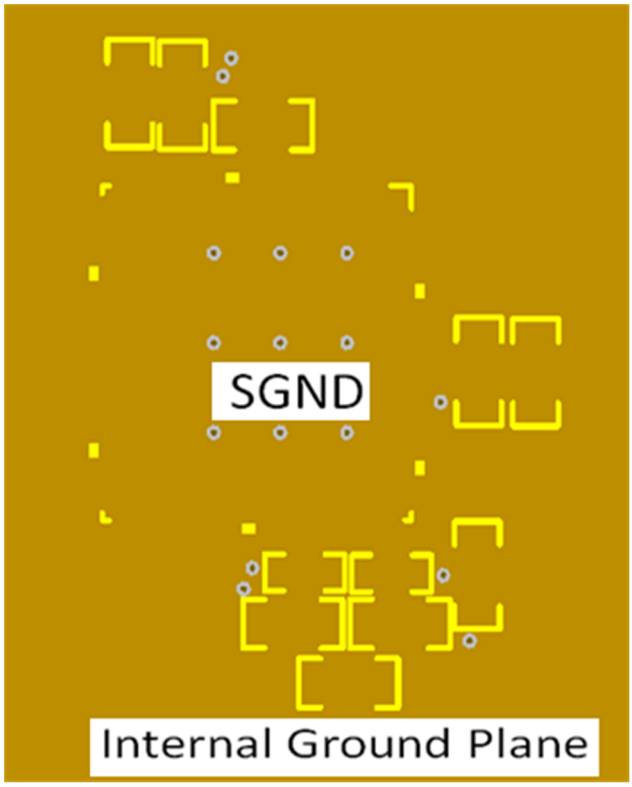


Figure 2-12. Layout Example for UCD3138ARGC on Internal Ground Layer

2.11 Layout Example for UCD3138ARGC by Using a Single Ground

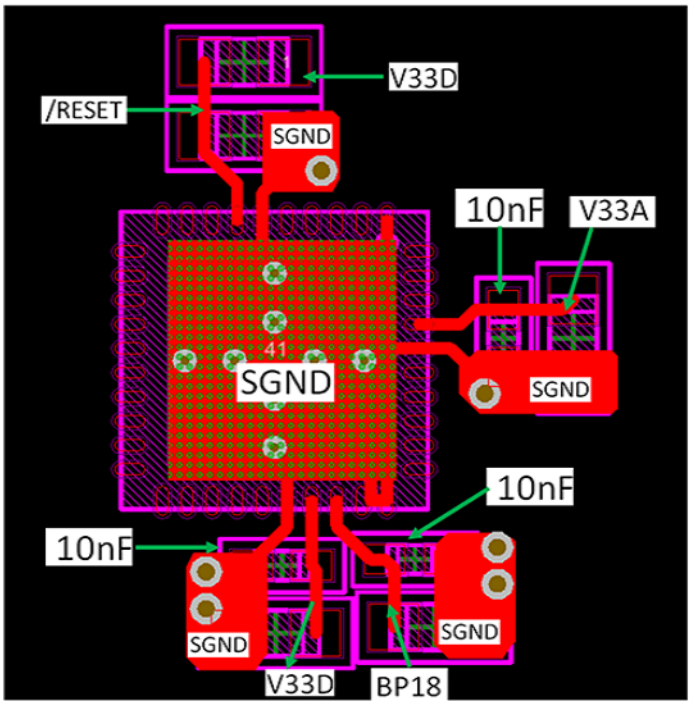


Figure 2-13. Layout Example for UCD3138A (40-Pin) on Top Layer

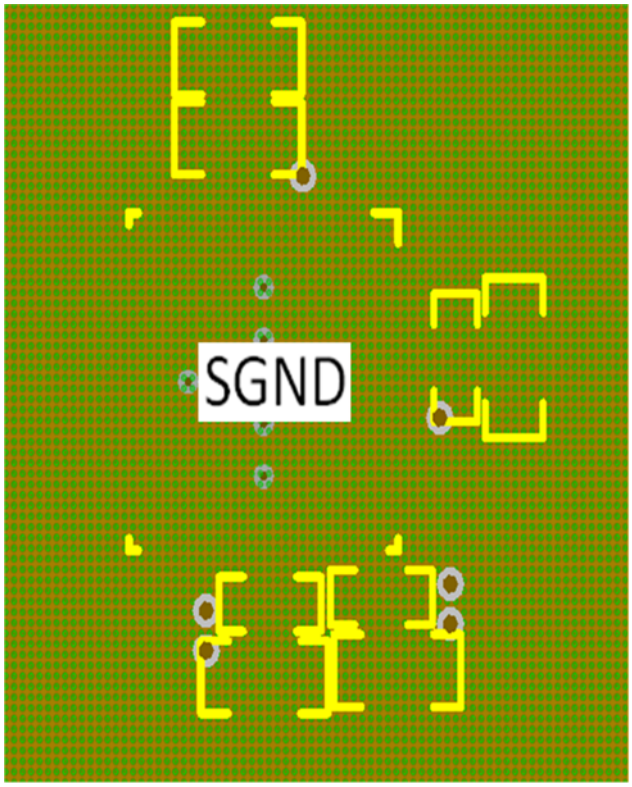


Figure 2-14. Layout Example for UCD3138A (40-Pin) on Internal Ground Layer

2.12 Layout Example for UCD3138128A by Using a Single Ground

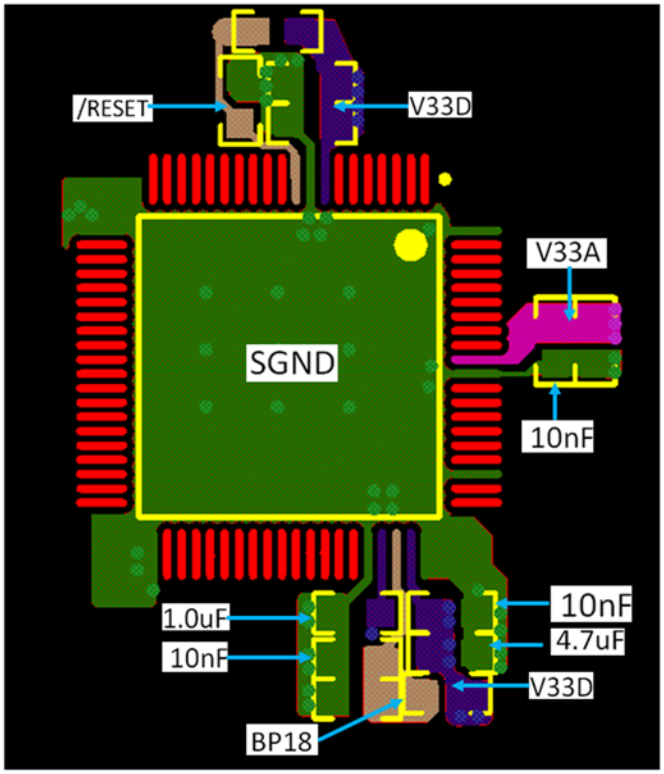


Figure 2-15. Layout Example for UCD3138128A on Top Layer

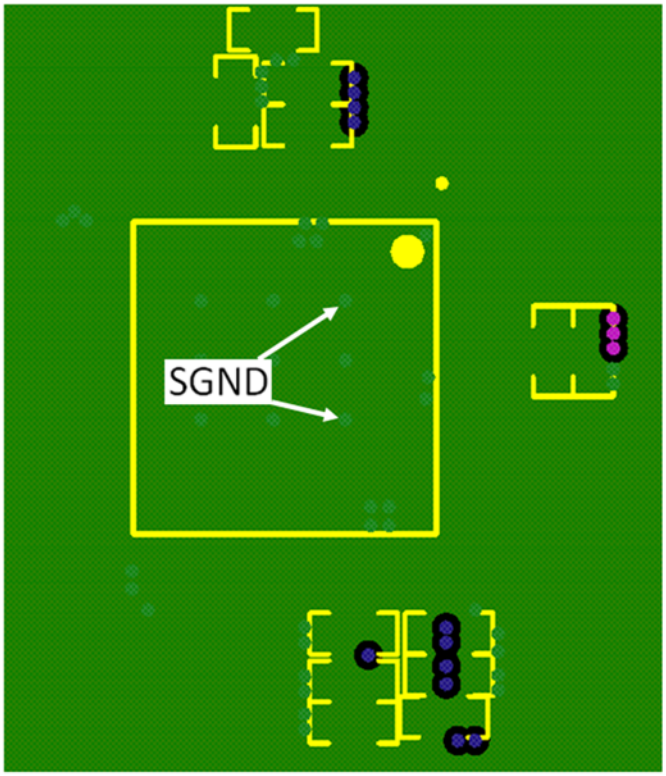


Figure 2-16. Layout Example for UCD3138128A on Internal Ground Layer

2.13 DPWMS Synchronization

For a half-bridge or full-bridge converter, where more than one DPWM modules are used to drive multiple pairs of MOSFETs, TI strongly recommends the synchronization between DPWM modules. The synchronization can be achieved by using Master-Slave mode. A slaved DPWM can be synchronized with other Master DPWM or Slave DPWM. Without synchronization, the DPWM could go out of synchronization at large currents which can cause catastrophic damage.

2.14 External Clock

In the device UCD3138128A, if the XTAL_IN (pin 61) and XTAL_OUT (pin 62) are not used for external clock, tie them to 1.8 V (pin BP18) through a 1-kΩ resistor respectively.

Recommendation for V33 Ramp up Slew Rate and nRESET Pin RC Time Constant

3.1 Recommendation for V33 Ramp up Slew Rate for UCD3138 and UCD3138064

UCD3138 and UCD3138064 need a 2.2 uF pullup capacitor from BP18 to V33 as described before. 2.2 uF and 1 uF create a capacitor divider which will pull BP18 up as V33 rises. Ensure that as V33 rises, the slew rate is not fast enough to cause BP18 to overshoot, resulting in a reliability issue. TI requires that the maximum voltage of BP18 does not exceed 1.95 V. By calculation, if V33 ramps up linearly, the maximum V33 slew rate should be less than 6 V/ms.

Also, the internal BP18 regulator is enabled when V33 is higher than V_{GH} and POR is activated. V33 charges the capacitor of BP18 through the internal regulator. This charge will cause voltage dip of V33 as shown in Figure 3-1, and the charge may trigger a V33 undervoltage (POR) event, causing a chip reset. To prevent POR trigger signal oscillation and successive chip resets, TI recommends a minimum slew rate of 2.6 V/ms.

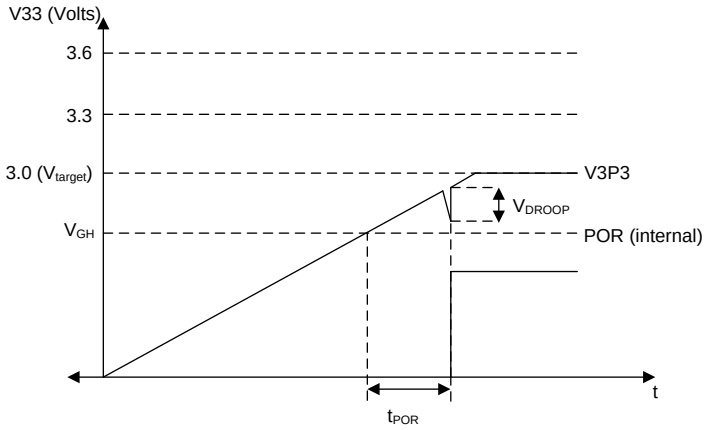


Figure 3-1. V33 Voltage Dip When POR is Activated

From the Figure 3-1 recommendations, the slew rate using the 2.2 uF/1uF capacitor combination requires that the slew rate must be as follows:

$$6\,V/ms \geq SR \geq 2.6\,V/ms \quad (1)$$

3.2 Recommendation for V33 Ramp up Slew Rate for UCD3138A, UCD3138064A, UCD3138A64, UCD3138128, UCD3138A64A, and UCD3138128A

In this group of UCD3138x, a 2.2 uF/1uF capacitor divider is unnecessary. Fast ramp up of V33 will not cause the voltage overshoot on BP18. Therefore, there is no requirement for maximum V33 slew rate.

These devices have the same minimum slew rate requirement as UCD3138 to avoid multiple chip resets given as follows:

$$SR \geq 2.6\,V/ms \quad (2)$$

If the minimum slew rate requirement cannot be met, use the nRESET pin to delay the reset of the digital logic so that a clean power up is achieved. This process is described in the following sections.

3.3 Recommendation for RC Time Constant of nRESET Pin for UCD3138 and UCD3138064

Ideally, the ARM core should begin execution of ROM code only after V33>3V. The ROM code reads trim values and loads trim registers. Lack of sufficient voltage during this operation can result in unexpected device functioning. Depending on V33 slew rate, the duration for which there is insufficient voltage on V33 is varied. During this time, a reliable trim operation is not ensured. Applying an RC filter between V33 and the nRESET pin can increase the delay from V33 power up to the device coming out of reset.

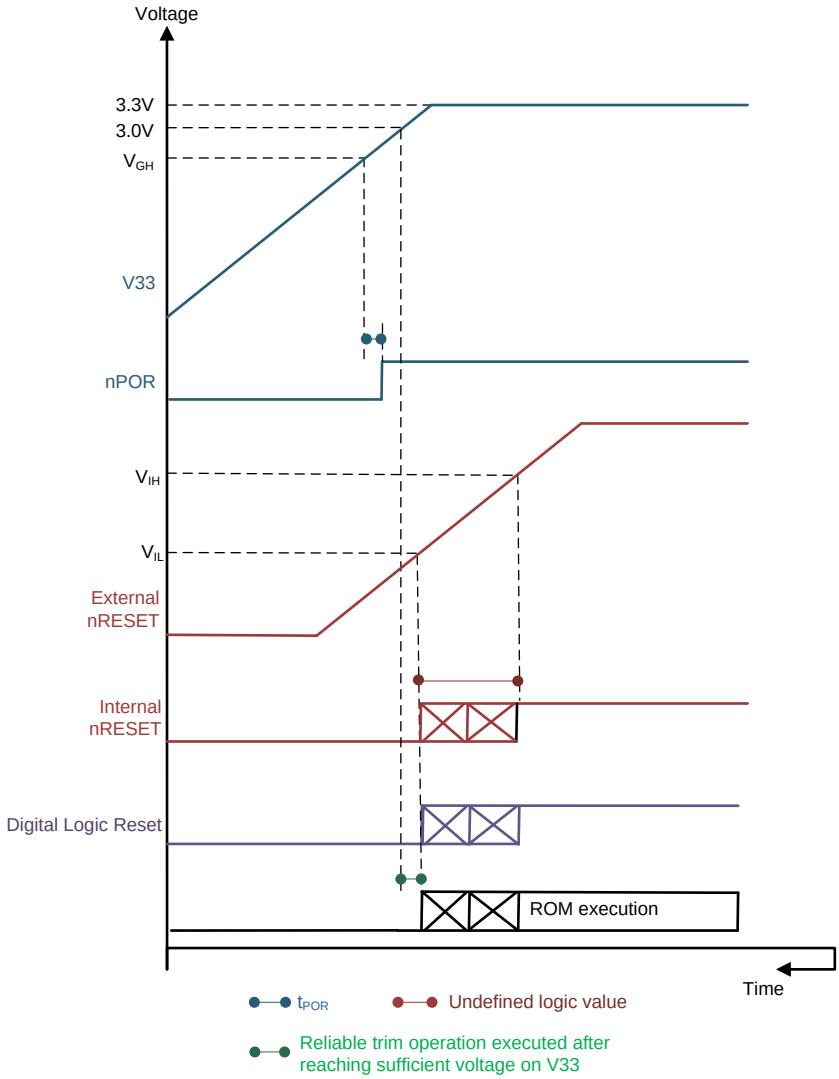


Figure 3-2. Recommended Timing Diagram of V33 and nRESET for UCD3138 and UCD3138064

Example Solution:

If the V33 supply slew rate is 0.6 V/ms, then the minimum τ required is calculated as follows:

$$\tau_{RESET} = \frac{V_{target} - V_{IL}}{SR} \tag{3}$$

$$\tau_{RESET\_min} = \frac{3V - 1.1V}{0.6V/ms} \approx 3.16\ ms \tag{4}$$

If R and C are 2.21 k and 2.2 uF, then τ evaluates as:

$$\tau = R \times C \approx 2.21\,k\Omega \times 2.2\,\mu F = 4.862\ ms \quad (5)$$

These values of 2.21 kΩ and 2.2 µF will ensure that the nRESET will be a logic-0 until V33 crosses 3V. [τ > τRESET_MIN]

3.4 Recommendation for RC Time Constant of nRESET Pin for UCD3138A, UCD3138064A, UCD3138A64, UCD3138128, UCD3138A64A, and UCD3138128A

The timing diagram in Figure 3-3 is slightly changed from what was described in Section 3.3 The difference is due to the nRESET pin being held low until the V33 voltage is higher than V_{GH} when POR is activated. Because the nRESET pin is not allowed to ramp up until a later time, the recommended RC time constant of the external nRESET filter changes.

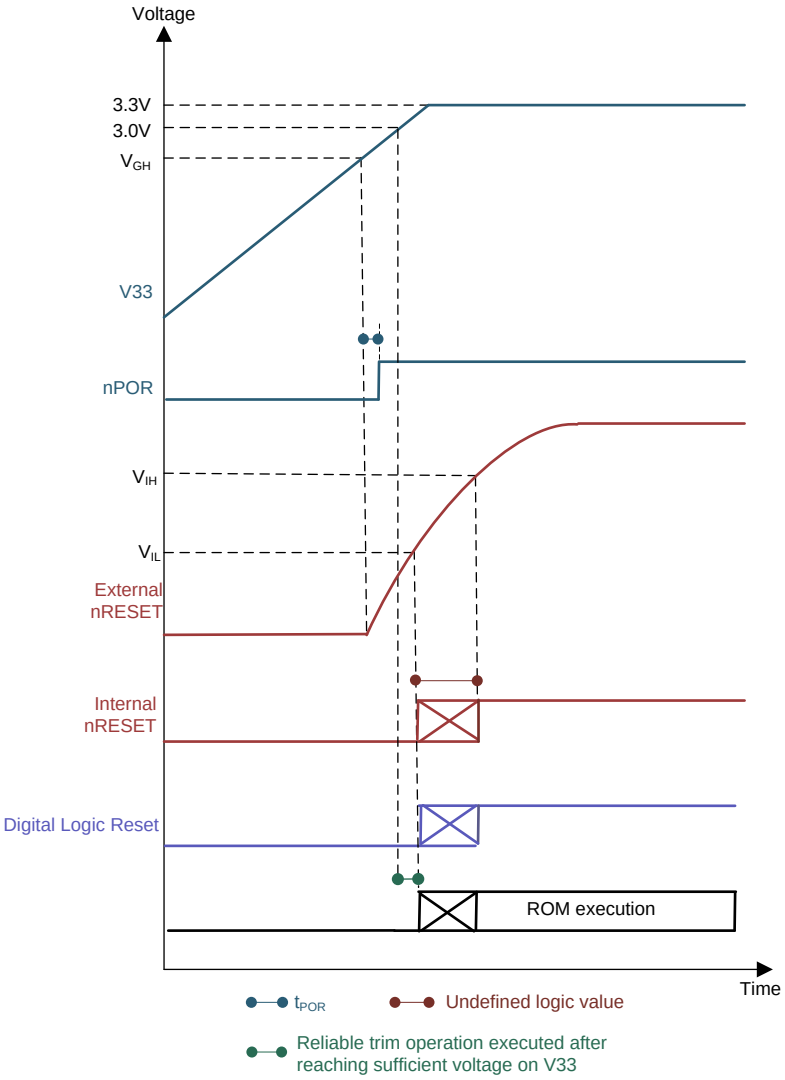


Figure 3-3. Recommended Timing Diagram of V33 and nRESET

Example Solution:

If the V33 supply slew rate is 0.6 V/ms, then the minimum τ required is calculated as follows:

$$\tau_{RESET} = \frac{V_{target} - V_{POR}}{SR} \tag{6}$$

$$\tau_{RESET} \cong \frac{V_{POR} - V_{target}}{SR \times \ln\left(1 - \frac{V_{IL}}{V_{POR}}\right)} \cong \frac{1\,V}{SR} \tag{7}$$

If SR=0.6 V/ms, then:

$$\tau_{RESET\_min} \cong 1.67\ ms \tag{8}$$

If R and C are 2.21 k and 2.2 uF, then τ evaluates as:

$$\tau = R \times C \approx 2.21\,k\Omega \times 2.2\,\mu F = 4.862\ ms \tag{9}$$

These values of 2.21 kΩ and 2.2 µF will ensure that the nRESET will be a logic-0 until V33 crosses 3V. [$\tau > \tau$RESET_MIN]

If the V33D does not ramp up linearly, the RC time constant is selected to ensure that the voltage of nRESET is less than V_{IL} when V33D approaches 3.0 V. TI recommends to use scope to check the time sequence.

EMI and EMC Mitigation Guideline

Every design is different in terms of EMI and EMC mitigation, and all designs require their own solution.

- Apply multiple different capacitors for different frequency range on decoupling circuits. Each capacitor has different ESL, capacitance and ESR, and different frequency responses.
- Avoid long traces close to radiation sources, and place them into an internal layer. It is preferred to have ground shielding and add a termination circuit at the end of the trace.
- TI recommends single ground: SGND. A multilayer such as 4 layers board is recommended so that one solid SGND is dedicated for return current path.
  - Use one whole layer (L3) for SGND plane as shown in Figure 4-1. Use many vias (such as 9 vias) to connect the extended power pad to the internal SGND plane layer. It is preferred to have the vias close to AGND pins and DGND pins of the device. For the 80-pin device, TI still recommneds a ground plane under the device even though there is no power pad on the device.
  - Place the UCD3138 controller away from radiation or switching components, then use layer 2 for trace routing to achieve good shielding from the ground layer (L3).

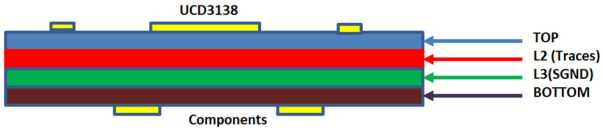


Figure 4-1. Optional Ground Layer Assignment

- Add LPF on analog signals close to the header connecting the control card and the power board.
- Analog circuit such as ADC sensing lines need a return current path into the analog plane; digital circuit, such as GPIO, PMBus and PWM, has a return current path into the digital plane; Even with a single plane, avoid mixing analog current and digital current.
- Do not use a ferrite bead to connect V33A and V33D instead of using 1-Ω resistor.
- Avoid negative current and negative voltage on all pins. Schottky diodes may be needed to clamp the voltage; avoid the voltage spike on all pins to exceed 3.8 V or below –0.3 V; add Schottky diodes on the pins which could have voltage spikes during surge test; be aware that Schottky diode has relatively higher leakage current, which can affect the voltage sensing at high temperatures. The need for external Schottky diodes are conditional. For example, the DPWM pins only need external Schottky diodes when there is a long distance, for example, more than 3 inches, between the control card and main power stage because in this case, the trace can pick up noises and cause electrical overstress on the device pins. The same is true for GPIO and PMBus pins.
- Auxiliary supply normally adopts a flyback converter, and its power transformer can generate a large electromagnetic field which can interfere with other electronic circuitry. By shielding the primary side windings, the EMI can be effectively reduced so that the surrounding circuit can have quieter working environment.

Special Consideration

- The first thing that must be done in any layout is to set up the basic grounding strategy and the placement of the decoupling capacitors. This needs to be prioritized over anything else even for the routing of sensitive feedback signals.
- If there are separate AGND or DGND planes, they must be tied together underneath the chip.
- If a gate driver device such as UCC27524 or UCC27511 is on the control card and there is a PGND connection, a net-short resistor or large copper trace must be used to tie the PGND to the Power RTN by multiple vias. Also, the net-short element between Power RTN and PGND must be close to the driver IC.
- Unused ADC pins must be tied to SGND.
- Avoid V33D and V33A long trace or plane close to radiation components and place them into an internal layer. It is preferred to have ground shielding.
- Avoid bias supplies or SGND or Power RTN directly to cross switching power train where they can couple switching noises. If the grounds are coupled with noises, the decoupling capacitors may not be effective to filter the noise out.
- Local capacitors are preferred to provide a short path for switching current, and be careful to select a quiet RETURN point to connect.
- In power module or a tiny PCB design, a single solid plane without the grounding separation is shown in Figure 5-1 and has a single point connection with power RTN or SGND near the connector. Ensure there is no current flow from power train into the signal ground plane.

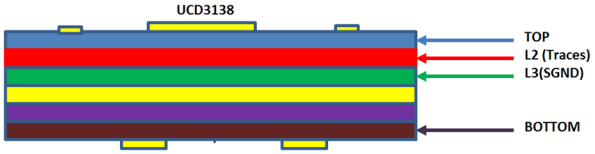


Figure 5-1. Single Ground Plane for a Power Module Design

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265