LC450210PCH

Application Note

Design method of the LCD system using 1/8-duty LCD panel

ON Semiconductor®

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Overview

This application note explains the design method of the LCD (Liquid Crystal Display) system using LCD driver LSI (LC450210PCH). The LC450210PCH is the 1/8 to 1/16 duty dot matrix LCD controller driver. By controlling this driver with a microcontroller, it is used in applications such as character display and simple graphic display etc.

The LC450210PCH can drive an LCD panel of up to 3,200 dots (16x16 dot font : 1-line display of up to 12 digits and 128 segments, 5x7 dot font : 2-line display of up to 40 digits).

LCD System Configuration Example

This application note explains various function explanations and setting method example of serial data in the LCD system configuration using LCD driver LSI (LC450210PCH) as shown below.

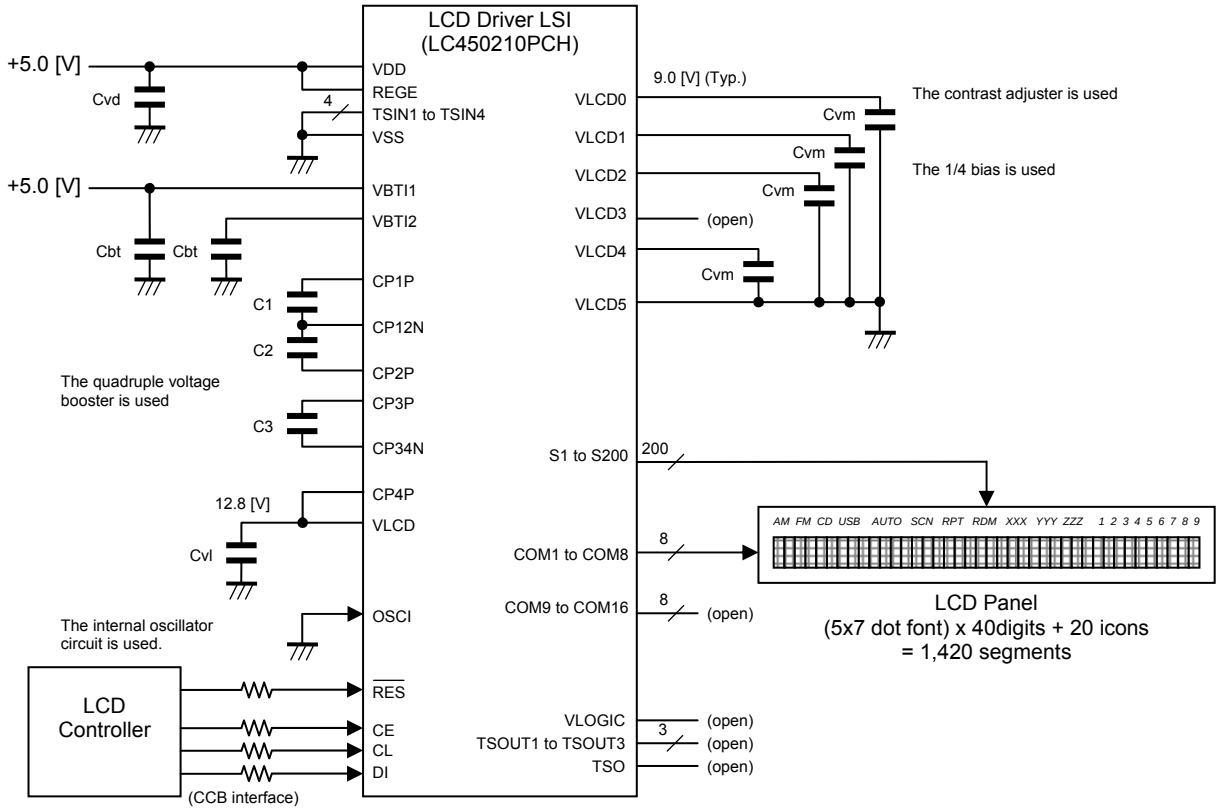

Figure 1. LCD system configuration using LCD driver LSI (LC450210PCH)

- CCB is ON Semiconductor® 's original format. All addresses are managed by ON Semiconductor® for this format.

- CCB is a registered trademark of Semiconductor Components Industries, LLC.

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< Operation specifications of the LCD system >

LCD driver LSI (LC450210PCH) specifications	LCD system specifications of Figure 1.
Selectable duty ratio by serial data: 1/8 duty to 1/16 duty	The LCD panel to use has 200 segments and 8 commons. Total display segments are 1,420 segments. Therefore, LCD drive duty ratio is 1/8 duty.
Selectable LCD bias voltage ratio by serial data: 1/4 bias or 1/5 bias	The 1/4 bias is used.
Selectable inversion drives of LCD drive waveforms by serial data: line inversion or frame inversion.	The frame inversion is used.
Adjustable frame frequency and clock frequency of voltage booster by serial data.	Used. (Controlled by LCD controller)
Selectable operation modes by serial data: power-saving mode (maintains display data), the state of display (ON, all ON, all OFF, all forced OFF).	Used. (Controlled by LCD controller)
Built-in oscillator circuit.	The internal oscillator circuit is used.
Selectable fundamental clock operating modes by serial data: internal oscillator operating mode or external clock operating mode.	The internal oscillator operating mode is used.
Input of serial data supports CCB* format (for 5V and 3V).	Used. (Controlled by LCD controller)
Selectable voltage range of power supply for logic block by setting REGE pad.	5V power supply. (REGE=VDD)
Built-in quadruple and quintuple voltage booster with discharge function.	The internal quadruple voltage booster is used. (VDD=5V)
Power supply for LCD driver block (VLCD).	VLCD=3.2 [V] x 4 = 12.8 [V](Typ.)
Built-in contrast adjuster for LCD drive bias voltage (VLCD0).	The internal contrast adjuster circuit is used.
The initialization of this driver and the prevention of an unintended display are controllable by setting $\overline{RES}$ pad.	Used. (Controlled by LCD controller)

Pad Assignment

The following figure shows the pin assignment of LCD driver LSI (LC450210PCH).

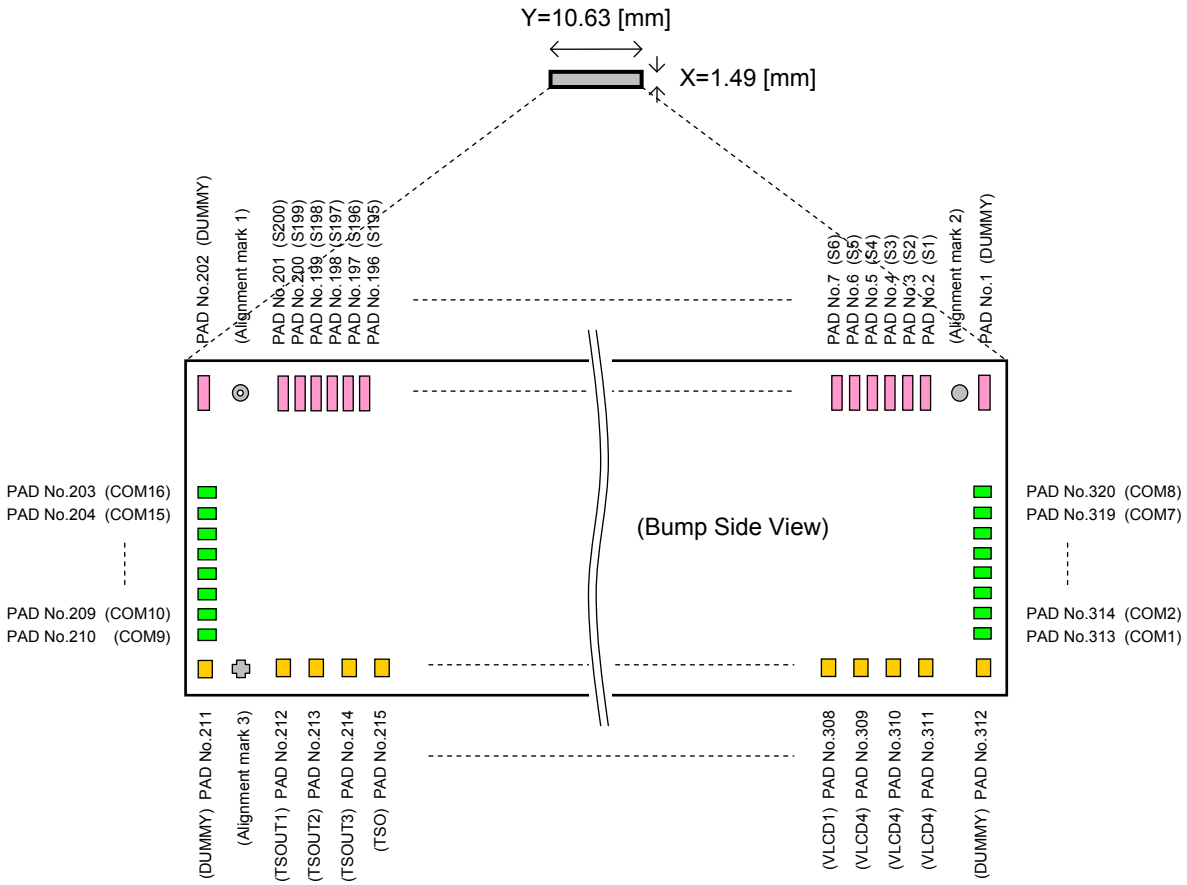


Figure 2. Pad Assignment of LCD driver LSI (LC450210PCH)

Table 1. Pad function of LCD driver LSI (LC450210PCH)

Pad name	Pad functions
VDD	Logic block power supply pad REGE=VDD : Supply a voltage from 4.5 [V] to 5.5 [V] to VDD. REGE=VSS : Supply a voltage from 2.7 [V] to 3.6 [V] to VDD. In addition, make sure to connect a capacitor between VDD and VSS.
VSS	Ground pad Make sure to connect VSS to ground.
VLOGIC	Regulator voltage monitor output pad Do not use VLOGIC with an external circuit.
REGE	Logic power supply regulator and voltage booster regulator control input pad Depending on specification of power supply, make sure to connect REGE to VDD or VSS. REGE=VDD : The 5V power supply is used. The regulator of logic power supply and the regulator of voltage booster run. REGE=VSS : The 3V power supply is used. The regulator of logic power supply and the regulator of voltage booster stop.
S1 to S200	Segment drive output pads
COM1 to COM16	Common drive output pads
VBTI1	Voltage booster base voltage input pad < When voltage booster is used > Make sure to connect a capacitor between VBTI1 and VSS. REGE=VDD : Input the voltage from 4.5V to VDD [V] to VBTI1. REGE=VSS : Connect VBTI1 to VBTI2, and Input the voltage from 2.7 [V] to VDD [V] to VBTI1. (When quadruple booster is used : VBTI1 ≤ 3.6 [V], When quintuple booster is used : VBTI1 ≤ 3.3 [V]) < When voltage booster is not used > Make sure to open VBTI1.
VBTI2	Voltage booster base voltage input-output pad < When voltage booster is used > Make sure to connect a capacitor between VBTI2 and VSS. REGE=VDD : VBTI2 outputs the base voltage for voltage booster. REGE=VSS : Connect VBTI1 to VBTI2, and Input the voltage from 2.7 [V] to VDD [V] to VBTI1. (When quadruple booster is used : VBTI1 ≤ 3.6 [V], When quintuple booster is used : VBTI1 ≤ 3.3 [V]) < When voltage booster is not used > Make sure to open VBTI2.
CP1P, CP12N, CP2P, CP3P, CP34N, CP4P	Voltage booster input-output pads < When quadruple voltage booster is used > Make sure to connect a capacitor between CP1P(+) and CP12N(-). Make sure to connect a capacitor between CP2P(+) and CP12N(-). Make sure to connect a capacitor between CP3P(+) and CP34N(-). Make sure to connect CP4P and VLCD. < When quintuple voltage booster is used > Make sure to connect a capacitor between CP1P(+) and CP12N(-). Make sure to connect a capacitor between CP2P(+) and CP12N(-). Make sure to connect a capacitor between CP3P(+) and CP34N(-). Make sure to connect a capacitor between CP4P(+) and CP34N(-). < When voltage booster is not used > Make sure to open CP1P, CP12N, CP2P, CP3P, CP34N and CP4P.
VLCD	LCD driver block power supply pad Make sure to connect a capacitor between VLCD and VSS. < When quadruple voltage booster is used > VLCD outputs the booster voltage (VBTI2 x 4). < When quintuple voltage booster is used > VLCD outputs the booster voltage (VBTI2 x 5). < When voltage booster is not used > Supply a voltage from 4.5 [V] to 16.5 [V] to VLCD. When contrast adjuster is used, follow a condition of VLCD ≥ VLCD0 + 2.4 [V].
VLCD0	LCD drive bias voltage (High level) input-output pad Make sure to connect a capacitor between VLCD0 and VLCD5. < When contrast adjuster is used > VLCD0 outputs the LCD drive bias voltage (High level) set by control data from CT0 to CT5 of the “Set of display contrast” instruction. However, follow a condition of VLCD0 ≤ VLCD - 2.4 [V]. < When contrast adjuster is not used > Input the LCD drive bias voltage (High level) to VLCD0 from the outside, and follow a condition of VLCD1 < VLCD0 ≤ VLCD.

Pad name	Pad function
VLCD1	LCD drive bias voltage (3/4 level, 4/5 level) input-output pad Make sure to connect a capacitor between VLCD1 and VLCD5. <u>< When LCD drive bias voltage generator is used></u> When 1/4 bias is used, VLCD1 outputs the LCD drive bias voltage (3/4 VLCD0). When 1/5 bias is used, VLCD1 outputs the LCD drive bias voltage (4/5 VLCD0). <u>< When LCD drive bias voltage generator is not used ></u> When 1/4 bias is used, Input the LCD drive bias voltage (3/4 VLCD0) to VLCD1 from the outside, and follow a condition of VLCD2 < VLCD1 < VLCD0. When 1/5 bias is used, Input the LCD drive bias voltage (4/5 VLCD0) to VLCD1 from the outside, and follow a condition of VLCD2 < VLCD1 < VLCD0.
VLCD2	LCD drive bias voltage (2/4 level, 3/5 level) input-output pad Make sure to connect a capacitor between VLCD2 and VLCD5. <u>< When LCD drive bias voltage generator is used></u> When 1/4 bias is used, VLCD2 outputs the LCD drive bias voltage (2/4 VLCD0). When 1/5 bias is used, VLCD2 outputs the LCD drive bias voltage (3/5 VLCD0). <u>< When LCD drive bias voltage generator is not used ></u> When 1/4 bias is used, Input the LCD drive bias voltage (2/4 VLCD0) to VLCD2 from the outside, and follow a condition of VLCD4 < VLCD2 < VLCD1. When 1/5 bias is used, Input the LCD drive bias voltage (3/5 VLCD0) to VLCD2 from the outside, and follow a condition of VLCD3 < VLCD2 < VLCD1.
VLCD3	LCD drive bias voltage (2/5 level) input-output pad <u>< When LCD drive bias voltage generator is used></u> When 1/4 bias is used, make sure to open VLCD3. When 1/5 bias is used, VLCD3 outputs the LCD drive bias voltage (2/5 VLCD0). Make sure to connect a capacitor between VLCD3 and VLCD5. <u>< When LCD drive bias voltage generator is not used ></u> When 1/4 bias is used, make sure to open VLCD3. When 1/5 bias is used, Input the LCD drive bias voltage (2/5 VLCD0) to VLCD3 from the outside, and follow a condition of VLCD4 < VLCD3 < VLCD2. Make sure to connect a capacitor between VLCD3 and VLCD5.
VLCD4	LCD drive bias voltage (1/4 level, 1/5 level) input-output pad Make sure to connect a capacitor between VLCD4 and VLCD5. <u>< When LCD drive bias voltage generator is used></u> When 1/4 bias is used, VLCD4 outputs the LCD drive bias voltage (1/4 VLCD0). When 1/5 bias is used, VLCD4 outputs the LCD drive bias voltage (1/5 VLCD0). <u>< When LCD drive bias voltage generator is not used ></u> When 1/4 bias is used, Input the LCD drive bias voltage (1/4 VLCD0) to VLCD4 from the outside, and follow a condition of VLCD5 < VLCD4 < VLCD2. When 1/5 bias is used, Input the LCD drive bias voltage (1/5 VLCD0) to VLCD4 from the outside, and follow a condition of VLCD5 < VLCD4 < VLCD3.
VLCD5	LCD drive bias voltage (Low level) input-output pad Make sure to connect VLCD5 to VSS even if the LCD drive bias generator is not used.
OSCI	External clock input pad (When external clock operating mode was set) When internal oscillator operating mode is set (OC="0"), make sure to connect OSCI to VSS. When external clock operating mode is set (OC="1"), the OSCI is used to input the external clock.
CE	Serial data transfer chip enable input pad
CL	Serial data transfer synchronization clock input pad
DI	Serial data transfer data input pad
$\overline{\text{RES}}$	Reset input pad $\overline{\text{RES}}$=VSS : The state of this LSI is reset. $\overline{\text{RES}}$=VDD : Normal state.
TSIN1, TSIN2, TSIN3, TSIN4	Test input pads Make sure to connect these pads to VSS.
TSOUT1, TSOUT2, TSOUT3	Test output pads Make sure to open these pads.
TSO	Test output pad Make sure to open this pad.
DUMMY	Dummy pads These pads are not available. Don't connect between dummy pads. Moreover, don't use them by an external circuit.

Explanation of the Serial Data Transfer

(1) Basic Timing

The LC450210PCH has several internal registers. These internal registers are written by CCB interface (Serial interface). Structure of transfer bits consists of CCB address and instruction data. First eight bits are CCB address (B2h). The bit number of instruction data is different depending on an instruction, and this is from 16 bits to 272 bits. The serial data is taken by the positive edge of the CL signal, which is latched by the negative edge of the CE signal. When the number of data in CE="High level" period is different from the defined number, LSI does not execute the instruction and holds the old state. Even when CL signal stops at high level, the CCB interface can be received. However, serial data transfer timing (transfer form) is different. Therefore, when designing equipment, refer to the "Delivery specification for the LC450210PCH".

For more information about the number of instruction data, refer to "(3) Explanation of Instruction Data".

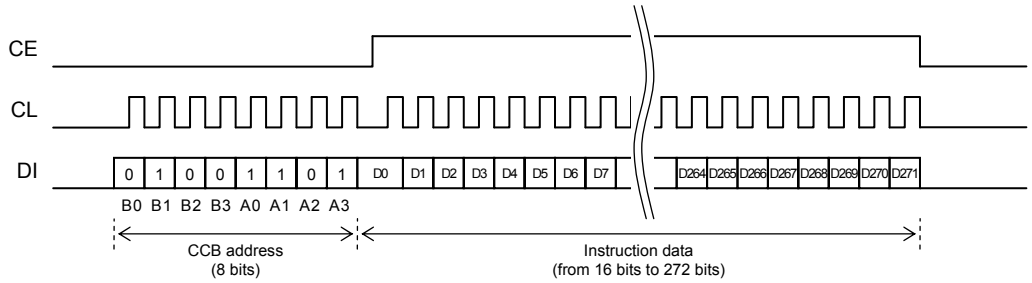


Figure 3. Basic timing when CL signal is stopped at the Low Level

(2) Allowable Operating Ranges of the Serial Data Transfer

The following figure shows the specifications of the allowable operating ranges when CL signal is stopped at the low level.

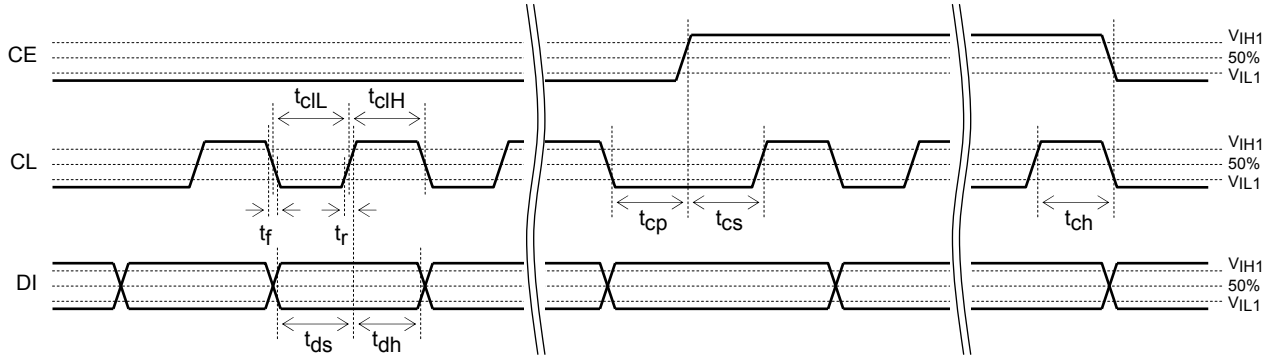


Figure 4. Allowable operating ranges of serial data transfer

Table 2. Allowable operating ranges at Ta= -40 to +105 [°C], VSS=0 [V]

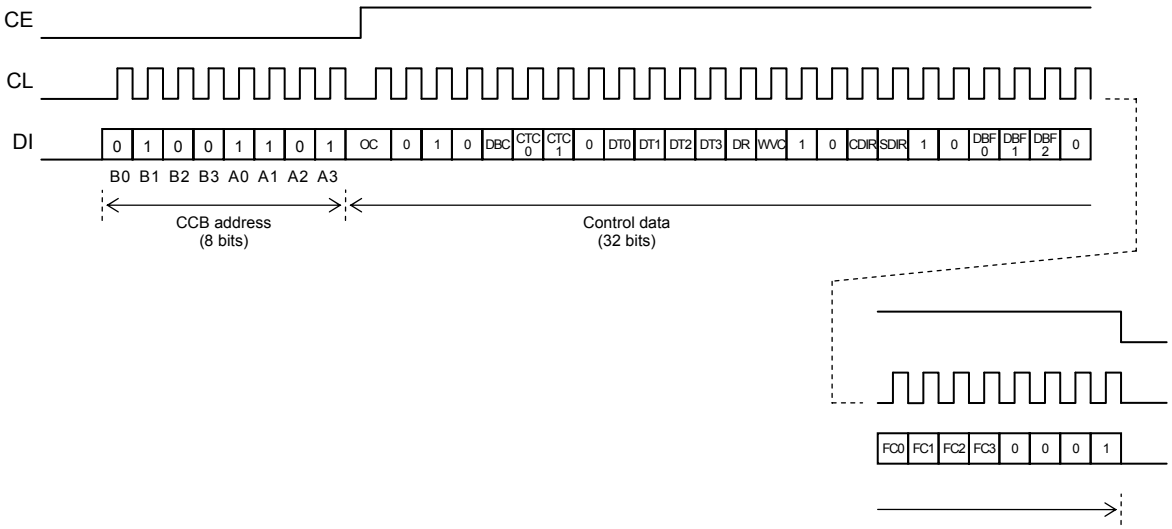
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	VDD, REGE=VDD	4.5		5.5	V
		VDD, REGE=VSS	2.7		3.6	V
Input High Level Voltage	V_{IH1}	CE, CL, DI, VDD=4.5V to 5.5V (REGE=VDD)	0.5 V_{DD}		5.5	V
		CE, CL, DI, VDD=2.7V to 3.6V (REGE=VSS)	0.8 V_{DD}		3.6	V
Input Low Level Voltage	V_{IL1}	CE, CL, DI, VDD=4.5V to 5.5V (REGE=VDD)	0		0.2 V_{DD}	V
		CE, CL, DI, VDD=2.7V to 3.6V (REGE=VSS)	0		0.2 V_{DD}	V
Serial Data Transfer Synchronization Clock Frequency	f_{cl}	CL, $1/(t_{clL}+t_{clH})$			3.125	MHz
Data Setup Time	t_{ds}	CL, DI	160			ns
Data Hold Time	t_{dh}	CL, DI	160			ns
CE Wait Time	t_{cp}	CE, CL	160			ns
CE Setup Time	t_{cs}	CE, CL	160			ns
CE Hold Time	t_{ch}	CE, CL	160			ns
High Level Clock Pulse Width	t_{clH}	CL	160			ns
Low Level Clock Pulse Width	t_{clL}	CL	160			ns
Rise Time	t_r	CE, CL, DI		160		ns
Fall Time	t_f	CE, CL, DI		160		ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

(3) Explanation of Instruction Data

(3-1) “Set of display method” instruction

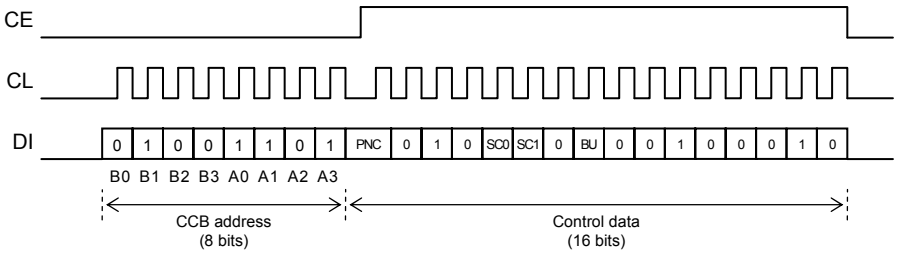
The display method is set by “Set of display method” instruction. After having reset a system by $\overline{RES}$=“Low level”, make sure to execute “Set of display method” first.



B0 to B3, A0 to A3	: CCB address. (=B2h)
OC	: Control data to set a fundamental clock operating mode.
DBC	: Control data to set a state of voltage booster circuit.
CTC0, CTC1	: Control data to set a state of contrast adjuster circuit and LCD drive bias voltage generator circuit.
DT0 to DT3	: Control data to set duty from 1/8 to 1/16.
DR	: Control data to set 1/4 bias or 1/5 bias.
WVC	: Control data to set inversion drive of LCD drive waveforms.
CDIR	: Control data to set scan direction of common outputs.
SDIR	: Control data to set a correspondence of a segment output and a column address of RAM.
DBF0 to DBF2	: Control data to set clock frequency of voltage booster.
FC0 to FC3	: Control data to set frame frequency of common and segment output waveforms.

(3-2) “Control of display ON / OFF” instruction

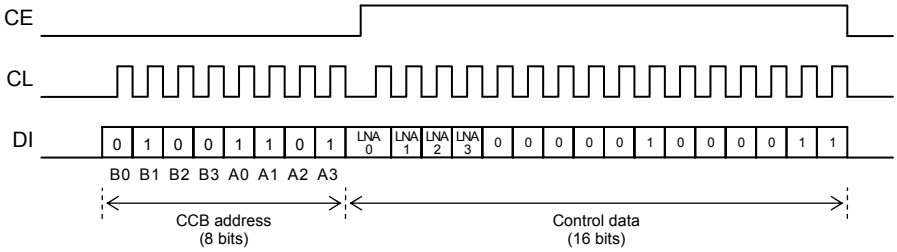
A state of display is set by “Control of display ON / OFF” instruction.



B0 to B3, A0 to A3	: CCB address. (=B2h)
PNC	: Control data to set normal display or reversed display.
SC0, SC1	: Control data to set a state of display.
BU	: Control data to set normal mode or power-saving mode.

(3-3) “Set of line address” instruction

A line address of RAM to appoint a start display position is set by “Set of line address” instruction.

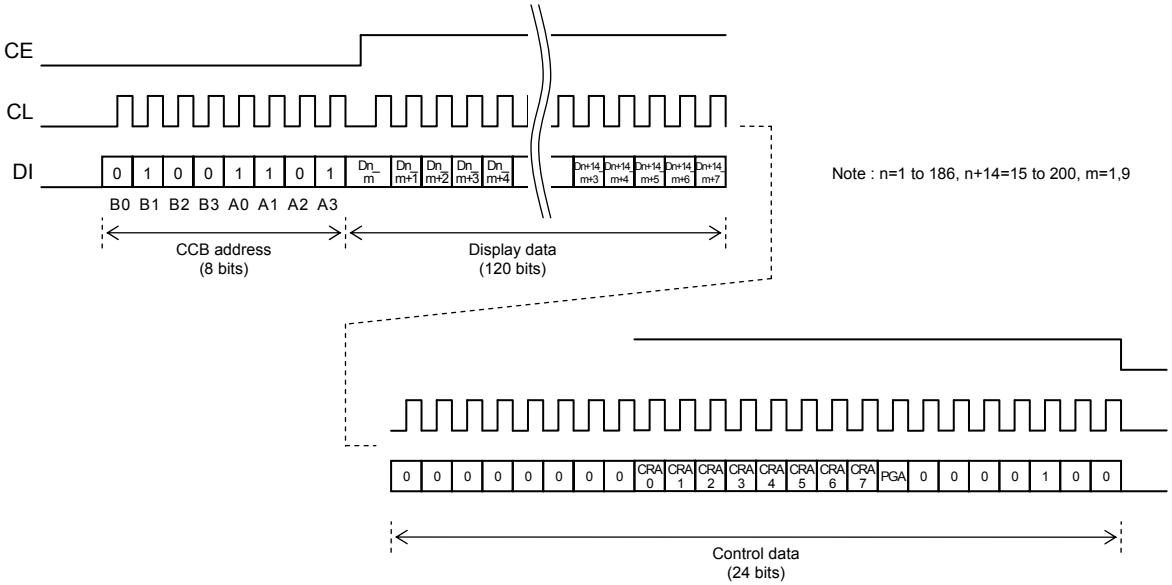


B0 to B3, A0 to A3 : CCB address. (=B2h)

LNA0 to LNA3 : Control data to set a line address of RAM.

(3-4) “Write display data to RAM (8 x 15 bits in a lump)” instruction

The display data of “8 x 15 bits (8 common outputs x 15 segment outputs)” is written to RAM in a lump by setting of page address and column address of RAM.



B0 to B3, A0 to A3 : CCB address. (=B2h)

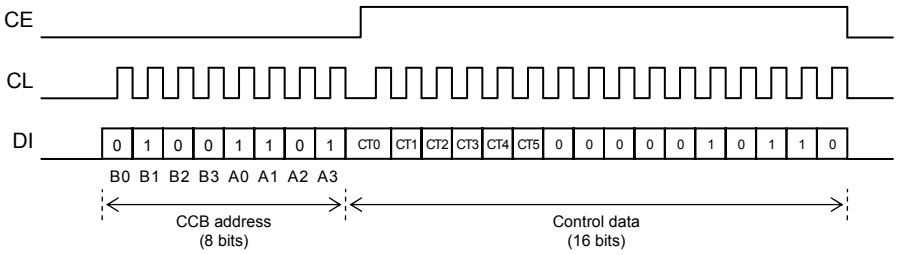
Dn_m, Dn_m+1 to Dn+14_m+7 : A display data which are written to RAM.
CRA0 to CRA7 : Control data to set a column address of RAM.
PGA : Control data to set a page address of RAM.

(3-5) “Write display data to RAM (16 x 16 bits in a lump)” instruction

The display data of “16 x 16 bits (16 common outputs x 16 segment outputs)” is written to RAM in a lump by setting of page address and column address of RAM. This LCD system configuration example does not use this serial data to use the LCD panel of 1/8 duty.

(3-6) “Set of display contrast” instruction

When contrast adjuster is used, LCD drive bias voltage VLCD0 (High level) is set by “Set of display contrast” instruction.



B0 to B3, A0 to A3 : CCB address. (=B2h)

CT0 to CT5 : Control data to set a display contrast.

Correspondence relation between the display data RAM and segment outputs

The customer can write display data to the display data RAM in a lump by setting a page address and a column address of the RAM by control data. The display data of 120 bits (for 8 common outputs x 15 segment outputs) are written to the display data RAM in a lump by “Write display data to RAM (8 x 15 bits in a lump)” instruction. Besides, the display data of 256 bits (for 16 common outputs x 16 segment outputs) are written to the display data RAM in a lump by “Write display data to RAM (16 x 16 bits in a lump)” instruction.

For details, refer to “Explanation of How to Write a Display Data RAM”.

Table 3. Display data RAM address mapping

		Segment outputs										
Normal direction (SDIR=0)		S1	S2	S3	S4	·····	S197	S198	S199	S200		
Reverse direction (SDIR=1)		S200	S199	S198	S197	·····	S4	S3	S2	S1		
Page address	PGA=0	D1_1	D2_1	D3_1	D4_1	·····	D197_1	D198_1	D199_1	D200_1	0H	Line address LNA0 to LNA3
		D1_2	D2_2	D3_2	D4_2	·····	D197_2	D198_2	D199_2	D200_2	1H	
		D1_3	D2_3	D3_3	D4_3	·····	D197_3	D198_3	D199_3	D200_3	2H	
		D1_4	D2_4	D3_4	D4_4	·····	D197_4	D198_4	D199_4	D200_4	3H	
		D1_5	D2_5	D3_5	D4_5	·····	D197_5	D198_5	D199_5	D200_5	4H	
		D1_6	D2_6	D3_6	D4_6	·····	D197_6	D198_6	D199_6	D200_6	5H	
		D1_7	D2_7	D3_7	D4_7	·····	D197_7	D198_7	D199_7	D200_7	6H	
		D1_8	D2_8	D3_8	D4_8	·····	D197_8	D198_8	D199_8	D200_8	7H	
	PGA=1	D1_9	D2_9	D3_9	D4_9	·····	D197_9	D198_9	D199_9	D200_9	8H	
		D1_10	D2_10	D3_10	D4_10	·····	D197_10	D198_10	D199_10	D200_10	9H	
		D1_11	D2_11	D3_11	D4_11	·····	D197_11	D198_11	D199_11	D200_11	AH	
		D1_12	D2_12	D3_12	D4_12	·····	D197_12	D198_12	D199_12	D200_12	BH	
		D1_13	D2_13	D3_13	D4_13	·····	D197_13	D198_13	D199_13	D200_13	CH	
		D1_14	D2_14	D3_14	D4_14	·····	D197_14	D198_14	D199_14	D200_14	DH	
		D1_15	D2_15	D3_15	D4_15	·····	D197_15	D198_15	D199_15	D200_15	EH	
		D1_16	D2_16	D3_16	D4_16	·····	D197_16	D198_16	D199_16	D200_16	FH	
		00H	01H	02H	03H	·····	C4H	C5H	C6H	C7H		
		Column address CRA0 to CRA7										

Start

Common address	Normal direction (CDIR=0)	Reverse direction (CDIR=1)
0H	COM1	COM16
1H	COM2	COM15
2H	COM3	COM14
3H	COM4	COM13
4H	COM5	COM12
5H	COM6	COM11
6H	COM7	COM10
7H	COM8	COM9

Explanation of the Clock Control

(1) Setting of the Fundamental Clock Operating Mode (OC)

The control data of the OC can set the internal oscillator operating mode or external clock operating mode. When the internal oscillator operating mode is set, clock generator begins to run after power saving mode is canceled (BU="0"). This LCD system configuration example sets OC="0" to use the internal oscillator operating mode.

OC	Fundamental clock operating mode	The state of OSCI
0	**Internal oscillator operating mode**	**Make sure to connect OSCI to VSS**
1	External clock operating mode	Input the clock of 300 [kHz](Typ.)

The explanation mentioned above is used only to explain internal operation and how to use the LSI, and the characteristic of the products is uneven by a production variation and the terms of use of the LSI (Power supply voltage, temperature, etc.). Therefore, the customer should always evaluate and test devices mounted in the customer's products or equipment.

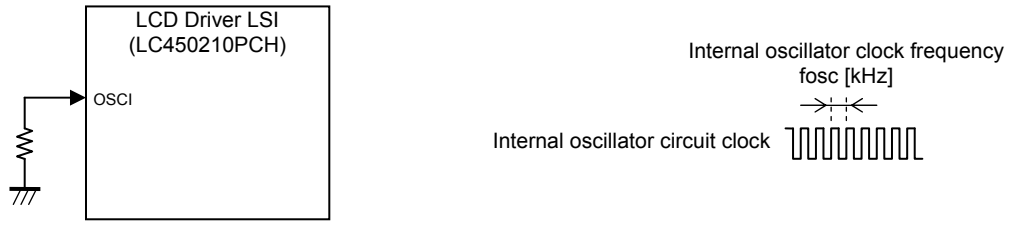


Figure 5. Peripheral circuits configuration example of the external clock input pad

(2) Setting of the Voltage Booster Clock Frequency (DBF0 to DBF2)

The control data from DBF0 to DBF2 can set the voltage booster clock frequency. It is easy to evade the interference of the frequency of other devices by this setting. This LCD system configuration example sets DBF0="0", DBF1="1" and DBF2="1" to operate voltage booster clock frequency at 13.63 [kHz].

DBF0	DBF1	DBF2	Voltage Booster Clock Frequency (fcp)	The voltage booster clock frequency when fosc is 300 [kHz]
0	0	0	fosc/12	25.00 [kHz]
0	0	1	fosc/14	21.43 [kHz]
0	1	0	fosc/18	16.66 [kHz]
0	**1**	**1**	**fosc/22**	**13.63 [kHz]**
1	0	0	fosc/26	11.54 [kHz]
1	0	1	fosc/28	10.71 [kHz]
1	1	0	fosc/30	10.00 [kHz]
1	1	1	fosc/34	8.82 [kHz]

(3) Setting of the Frame Frequency for LCD Drive Waveforms (FC0 to FC3)

The control data from FC0 to FC3 can set the LCD drive frame frequency (fo). There is a lot of flexibility for various LCDs (TN-LCD, VA/TN-LCD). VA (Vertical Alignment) type has the characteristic of high contrast and wants a high frequency. In addition, it is easy to evade the interference of the frequency of other devices by this setting. This LCD system configuration example sets FC0="0", FC1="1", FC2="0" and FC3="0" to operate LCD drive frame frequency at 101.9 [Hz].

FC0	FC1	FC2	FC3	LCD drive frame frequency (fo)								
				1/8duty	1/9duty	1/10duty	1/11duty	1/12duty	1/13duty	1/14duty	1/15duty	1/16duty
0	0	0	0	fosc/4352 <68.9[Hz]>	fosc/4320 <69.4[Hz]>	fosc/4320 <69.4[Hz]>	fosc/4400 <68.2[Hz]>	fosc/4320 <69.4[Hz]>	fosc/4264 <70.4[Hz]>	fosc/4256 <70.5[Hz]>	fosc/4320 <69.4[Hz]>	fosc/4352 <68.9[Hz]>
1	0	0	0	fosc/3712 <80.8[Hz]>	fosc/3744 <80.1[Hz]>	fosc/3760 <79.8[Hz]>	fosc/3784 <79.3[Hz]>	fosc/3744 <80.1[Hz]>	fosc/3744 <80.1[Hz]>	fosc/3808 <78.8[Hz]>	fosc/3720 <80.7[Hz]>	fosc/3712 <80.8[Hz]>
0	**1**	**0**	**0**	**fosc/2944 <101.9[Hz]>**	fosc/2952 <101.6[Hz]>	fosc/2960 <101.4[Hz]>	fosc/2992 <100.3[Hz]>	fosc/2976 <100.8[Hz]>	fosc/2964 <101.2[Hz]>	fosc/2968 <101.1[Hz]>	fosc/3000 <100.0[Hz]>	fosc/2944 <101.9[Hz]>
1	1	0	0	fosc/2368 <126.7[Hz]>	fosc/2376 <126.3[Hz]>	fosc/2400 <125.0[Hz]>	fosc/2376 <126.3[Hz]>	fosc/2400 <125.0[Hz]>	fosc/2392 <125.4[Hz]>	fosc/2408 <124.6[Hz]>	fosc/2400 <125.0[Hz]>	fosc/2368 <126.7[Hz]>
0	0	1	0	fosc/1984 <151.2[Hz]>	fosc/1944 <154.3[Hz]>	fosc/2000 <150.0[Hz]>	fosc/1936 <155.0[Hz]>	fosc/1968 <152.4[Hz]>	fosc/1976 <151.8[Hz]>	fosc/1960 <153.1[Hz]>	fosc/1980 <151.5[Hz]>	fosc/1984 <151.2[Hz]>
1	0	1	0	fosc/1696 <176.9[Hz]>	fosc/1692 <177.3[Hz]>	fosc/1720 <174.4[Hz]>	fosc/1672 <179.4[Hz]>	fosc/1728 <173.6[Hz]>	fosc/1716 <174.8[Hz]>	fosc/1708 <175.6[Hz]>	fosc/1710 <175.4[Hz]>	fosc/1696 <176.9[Hz]>

FC0	FC1	FC2	FC3	LCD drive frame frequency (fo)								
				1/8duty	1/9duty	1/10duty	1/11duty	1/12duty	1/13duty	1/14duty	1/15duty	1/16duty
0	1	1	0	fosc/1472 <203.8[Hz]>	fosc/1476 <203.3[Hz]>	fosc/1480 <202.7[Hz]>	fosc/1496 <200.5[Hz]>	fosc/1488 <201.6[Hz]>	fosc/1482 <202.4[Hz]>	fosc/1456 <206.0[Hz]>	fosc/1500 <200.0[Hz]>	fosc/1472 <203.8[Hz]>
1	1	1	0	fosc/1312 <228.7[Hz]>	fosc/1332 <225.2[Hz]>	fosc/1320 <227.3[Hz]>	fosc/1320 <227.3[Hz]>	fosc/1320 <227.3[Hz]>	fosc/1326 <226.2[Hz]>	fosc/1316 <228.0[Hz]>	fosc/1350 <222.2[Hz]>	fosc/1312 <228.7[Hz]>
0	0	0	1	fosc/1184 <253.4[Hz]>	fosc/1188 <252.5[Hz]>	fosc/1200 <250.0[Hz]>	fosc/1188 <252.5[Hz]>	fosc/1200 <250.0[Hz]>	fosc/1196 <250.8[Hz]>	fosc/1204 <249.2[Hz]>	fosc/1200 <250.0[Hz]>	fosc/1184 <253.4[Hz]>
1	0	0	1	fosc/1088 <275.7[Hz]>	fosc/1080 <277.8[Hz]>	fosc/1080 <277.8[Hz]>	fosc/1100 <272.7[Hz]>	fosc/1104 <271.7[Hz]>	fosc/1118 <268.3[Hz]>	fosc/1092 <274.7[Hz]>	fosc/1080 <277.8[Hz]>	fosc/1088 <275.7[Hz]>
0	1	0	1	fosc/1056 <284.1[Hz]>	fosc/1044 <287.4[Hz]>	fosc/1040 <288.5[Hz]>	fosc/1056 <284.1[Hz]>	fosc/1056 <284.1[Hz]>	fosc/1040 <288.5[Hz]>	fosc/1036 <289.6[Hz]>	fosc/1050 <285.7[Hz]>	fosc/1056 <284.1[Hz]>
1	1	0	1	fosc/992 <302.4[Hz]>	fosc/1008 <297.6[Hz]>	fosc/1000 <300.0[Hz]>	fosc/990 <303.0[Hz]>	fosc/984 <304.9[Hz]>	fosc/988 <303.6[Hz]>	fosc/980 <306.1[Hz]>	fosc/990 <303.0[Hz]>	fosc/992 <302.4[Hz]>
0	0	1	1	fosc/960 <312.5[Hz]>	fosc/972 <308.6[Hz]>	fosc/960 <312.5[Hz]>	fosc/946 <317.1[Hz]>	fosc/960 <312.5[Hz]>	fosc/962 <311.9[Hz]>	fosc/952 <315.1[Hz]>	fosc/960 <312.5[Hz]>	fosc/960 <312.5[Hz]>
1	0	1	1	fosc/928 <323.3[Hz]>	fosc/936 <320.5[Hz]>	fosc/920 <326.1[Hz]>	fosc/924 <324.7[Hz]>	fosc/936 <320.5[Hz]>	fosc/936 <320.5[Hz]>	fosc/924 <324.7[Hz]>	fosc/930 <322.6[Hz]>	fosc/928 <323.3[Hz]>
0	1	1	1	fosc/896 <334.8[Hz]>	fosc/900 <333.3[Hz]>	fosc/900 <333.3[Hz]>	fosc/902 <332.6[Hz]>	fosc/888 <337.8[Hz]>	fosc/884 <339.4[Hz]>	fosc/896 <334.8[Hz]>	fosc/900 <333.3[Hz]>	fosc/896 <334.8[Hz]>
1	1	1	1	fosc/864 <347.2[Hz]>	fosc/864 <347.2[Hz]>	fosc/860 <348.8[Hz]>	fosc/858 <349.7[Hz]>	fosc/864 <347.2[Hz]>	fosc/858 <349.7[Hz]>	fosc/868 <345.6[Hz]>	fosc/870 <344.8[Hz]>	fosc/864 <347.2[Hz]>

The value of "< >" is an LCD drive frame frequency when fosc is 300 [kHz]. The explanation mentioned above is used only to explain internal operation and how to use the LSI, and the characteristic of the products is uneven by a production variation and the terms of use of the LSI (Power supply voltage, temperature, etc.). Therefore, the customer should always evaluate and test devices mounted in the customer's products or equipment.

Explanation of the Internal Circuit Control

(1) State Setting of the Voltage Booster Circuit, Contrast Adjuster Circuit and LCD Drive Bias Voltage Generator Circuit (DBC, CTC0, CTC1)

The control data of the DBC can set the voltage booster circuit to the run state or stop state. The control data of the CT0 and CT1 can set the contrast adjuster circuit and LCD drive bias voltage generator circuit to the run state or stop state. This LCD system configuration example sets DBC="1", CTC0="1" and CTC1="1" to use the all circuits (voltage booster circuit, contrast adjuster circuit and LCD drive bias voltage generator circuit).

DBC	CTC0	CTC1	Voltage booster circuit	Contrast adjuster circuit	LCD drive bias voltage generator circuit
0	0	0	Stop	Stop	Stop
0	0	1	Stop	Stop	Run
0	1	0	Stop	Run	Stop
0	1	1	Stop	Run	Run
1	0	0	Run	Stop	Stop
1	0	1	Run	Stop	Run
1	1	0	Run	Run	Stop
1	**1**	**1**	**Run**	**Run**	**Run**

This LCD system configuration example sets as follows to use the quadruple voltage booster circuit.

VBTI1 : The REGE pad is set to VDD, and input the voltage from 4.5 [V] to VDD [V].
VBTI2 : The REGE pad is set to VDD, and outputs the base voltage for voltage booster.
VLCD : The quadruple VBTI2 voltage is outputted.

This LCD system configuration example sets as follows to use the contrast adjuster circuit.

VLCD0 : The VLCD0 outputs the LCD drive bias voltage (4/4 level) according to control data from CT0 to CT5 in "Set of display contrast" instruction. Make sure to connect a capacitor between VLCD0 and VLCD5.

This LCD system configuration example sets as follows to use the LCD drive bias voltage generator circuit and 1/4 bias circuit.

VLCD1 : The VLCD outputs the LCD drive bias voltage (3/4 level). Make sure to connect a capacitor between VLCD1 and VLCD5.
VLCD2 : The VLCD outputs the LCD drive bias voltage (2/4 level). Make sure to connect a capacitor between VLCD2 and VLCD5.
VLCD3 : Make sure to open VLCD3.
VLCD4 : The VLCD outputs the LCD drive bias voltage (1/4 level). Make sure to connect a capacitor between VLCD4 and VLCD5.
VLCD5 : Make sure to connect VLCD5 to VSS (0/4 level).

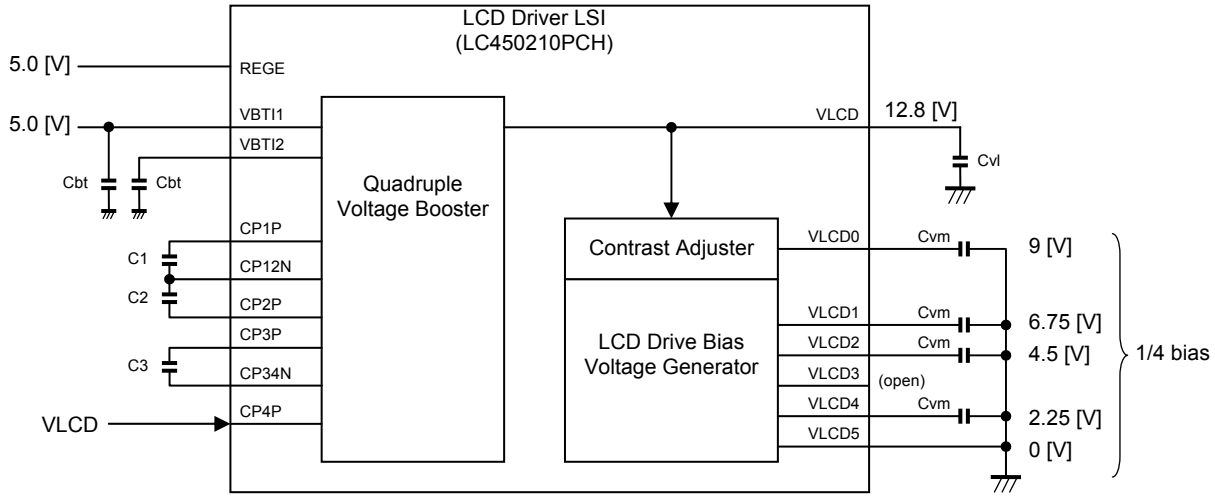


Figure 6. Peripheral circuits configuration example of the internal circuit for LC450210PCH

(2) Setting of the LCD Drive Bias Voltage Using the Contrast Adjuster Circuit (CT0 to CT5)

The control data from CT0 to CT5 can set the LCD drive bias voltage (VLCD0) using the contrast adjuster circuit. However, satisfy a condition of VLCD0 ≤ VLCD - 2.4 [V]. This LCD system configuration example sets CT0="0", CT1="1", CT2="0", CT3="0", CT4="0" and CT5="1" to use the LCD drive bias voltage (VLCD0) as 9.0 [V].

When VBTI1=5.0 [V], REGE=VDD, quadruple voltage booster and contrast adjuster are used, LCD power supply voltage (VLCD) becomes 12.8 [V] that quadruple the VBTI2 output of 3.2 [V] (Typical electrical characteristics). In addition, when the VBTI2 output of 3.3 [V] (Maximum electrical characteristics), the VLCD is 13.2 [V]. Moreover, when the VBTI2 output of 3.09 [V] (Minimum electrical characteristics), the VLCD is 12.36 [V]. The customer can select from step 28 (9.90 [V]) to step 63 (4.65 [V]) at the time of this setting state. When these are set from step 0 (14.10 [V]) to step 27 (10.05 [V]), the VLCD0 voltage is not guaranteed.

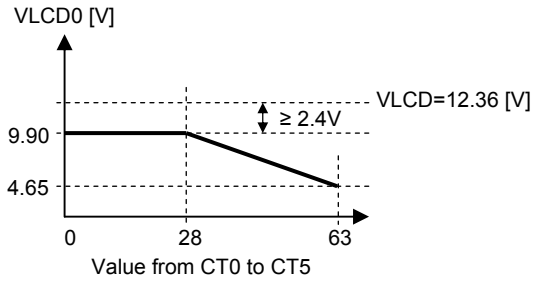


Figure 7. Adjustment range of the LCD drive bias voltage (VLCD0)

Table 4. Setting of settable contrast adjustment

Step	CT0	CT1	CT2	CT3	CT4	CT5	VLCD0 voltage
0	0	0	0	0	0	0	not guaranteed
1	1	0	0	0	0	0	not guaranteed
2	0	1	0	0	0	0	not guaranteed
3	1	1	0	0	0	0	not guaranteed
4	0	0	1	0	0	0	not guaranteed
5	1	0	1	0	0	0	not guaranteed
6	0	1	1	0	0	0	not guaranteed
7	1	1	1	0	0	0	not guaranteed
8	0	0	0	1	0	0	not guaranteed
9	1	0	0	1	0	0	not guaranteed
10	0	1	0	1	0	0	not guaranteed
11	1	1	0	1	0	0	not guaranteed
12	0	0	1	1	0	0	not guaranteed
13	1	0	1	1	0	0	not guaranteed
14	0	1	1	1	0	0	not guaranteed
15	1	1	1	1	0	0	not guaranteed
16	0	0	0	0	1	0	not guaranteed
17	1	0	0	0	1	0	not guaranteed
18	0	1	0	0	1	0	not guaranteed
19	1	1	0	0	1	0	not guaranteed
20	0	0	1	0	1	0	not guaranteed
21	1	0	1	0	1	0	not guaranteed
22	0	1	1	0	1	0	not guaranteed
23	1	1	1	0	1	0	not guaranteed
24	0	0	0	1	1	0	not guaranteed
25	1	0	0	1	1	0	not guaranteed
26	0	1	0	1	1	0	not guaranteed
27	1	1	0	1	1	0	not guaranteed
28	0	0	1	1	1	0	9.90 V
29	1	0	1	1	1	0	9.75 V
30	0	1	1	1	1	0	9.60 V
31	1	1	1	1	1	0	9.45 V
32	0	0	0	0	0	1	9.30 V
33	1	0	0	0	0	1	9.15 V
34	**0**	**1**	**0**	**0**	**0**	**1**	**9.00 V**
35	1	1	0	0	0	1	8.85 V
36	0	0	1	0	0	1	8.70 V
37	1	0	1	0	0	1	8.55 V
38	0	1	1	0	0	1	8.40 V
39	1	1	1	0	0	1	8.25 V
40	0	0	0	1	0	1	8.10 V
41	1	0	0	1	0	1	7.95 V
42	0	1	0	1	0	1	7.80 V
43	1	1	0	1	0	1	7.65 V
44	0	0	1	1	0	1	7.50 V
45	1	0	1	1	0	1	7.35 V
46	0	1	1	1	0	1	7.20 V
47	1	1	1	1	0	1	7.05 V
48	0	0	0	0	1	1	6.90 V
49	1	0	0	0	1	1	6.75 V
50	0	1	0	0	1	1	6.60 V
51	1	1	0	0	1	1	6.45 V
52	0	0	1	0	1	1	6.30 V
53	1	0	1	0	1	1	6.15 V
54	0	1	1	0	1	1	6.00 V
55	1	1	1	0	1	1	5.85 V
56	0	0	0	1	1	1	5.70 V
57	1	0	0	1	1	1	5.55 V
58	0	1	0	1	1	1	5.40 V
59	1	1	0	1	1	1	5.25 V
60	0	0	1	1	1	1	5.10 V
61	1	0	1	1	1	1	4.95 V
62	0	1	1	1	1	1	4.80 V
63	1	1	1	1	1	1	4.65 V

The explanation mentioned above is used only to explain internal operation and how to use the LSI, and the characteristic of the products is uneven by a production variation and the terms of use of the LSI (Power supply voltage, temperature, etc.). Therefore, the customer should always evaluate and test devices mounted in the customer's products or equipment.

(3) Explanation of the Setting to the Discharge Condition

The voltage booster circuit, the contrast adjuster circuit and the LCD drive bias voltage generator circuit have the discharge circuit to discharge an electric charge of the external capacitor.

When the voltage booster is set to the discharge condition, the VLCD level is same as VBTI1 level. When the contrast adjuster and the LCD drive bias voltage generator are set to the discharge condition, the levels from VLCD0 to VLCD4 are same as VLCD5 level.

Table 5. Discharge condition setting in the internal circuit

Pad	Control data				Voltage booster circuit (VLCD output)	Contrast adjuster circuit (VLCD0 output)	LCD drive bias voltage generator circuit (VLCD1 to VLCD4 outputs)
$\overline{RES}$	BU	DBC	CTC0	CTC1			
Low	X	X	X	X	Discharge	Discharge	Discharge
High	0	0	0	0	Stop (High-impedance)	Stop (High-impedance)	Stop (High-impedance)
		0	0	1	Stop (High-impedance)	Stop (High-impedance)	Run (Voltage output)
		0	1	0	Stop (High-impedance)	Run (Voltage output)	Stop (High-impedance)
		0	1	1	Stop (High-impedance)	Run (Voltage output)	Run (Voltage output)
		1	0	0	Run (Voltage output)	Stop (High-impedance)	Stop (High-impedance)
		1	0	1	Run (Voltage output)	Stop (High-impedance)	Run (Voltage output)
		1	1	0	Run (Voltage output)	Run (Voltage output)	Stop (High-impedance)
		1	1	1	Run (Voltage output)	Run (Voltage output)	Run (Voltage output)
High	1	0	0	0	Stop (High-impedance)	Stop (High-impedance)	Stop (High-impedance)
		0	0	1	Stop (High-impedance)	Stop (High-impedance)	Discharge (VLCD5 level)
		0	1	0	Stop (High-impedance)	Discharge (VLCD5 level)	Stop (High-impedance)
		0	1	1	Stop (High-impedance)	Discharge (VLCD5 level)	Discharge (VLCD5 level)
		1	0	0	Discharge (VBTI1 level)	Stop (High-impedance)	Stop (High-impedance)
		1	0	1	Discharge (VBTI1 level)	Stop (High-impedance)	Discharge (VLCD5 level)
		1	1	0	Discharge (VBTI1 level)	Discharge (VLCD5 level)	Stop (High-impedance)
		1	1	1	Discharge (VBTI1 level)	Discharge (VLCD5 level)	Discharge (VLCD5 level)

X : Don't care (0 or 1)

Explanation of the LCD Drive Control

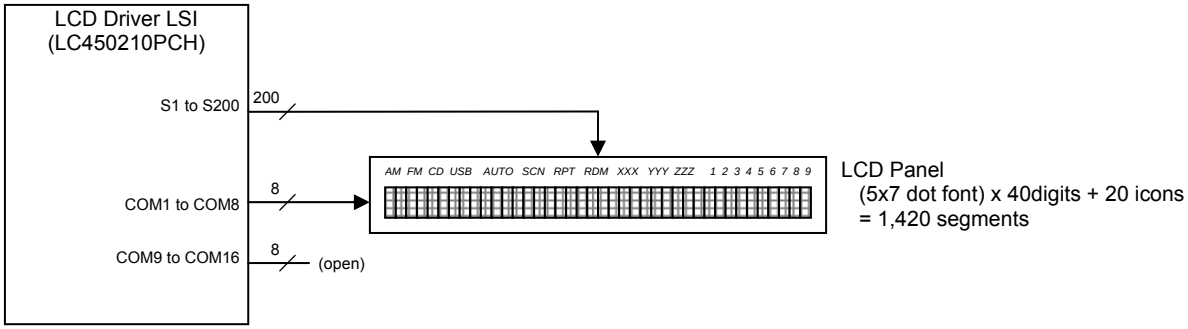


Figure 8. Peripheral circuits configuration example of the LCD driver outputs

(1) LCD Drive Waveform

It is explanation about the drive type of the 1/8 duty and 1/4 bias. The common outputs (COM1 to COM8) repeat VLCD0 level, VLCD1 level, VLCD4 level and VLCD5 level in turn. On the other hand, the segment outputs (S1 to S200) repeat VLCD0 level, VLCD2 level and VLCD5 level by a state of display ON/OFF (Display data setting register is 1/0). When the LCD segment is ON (It interrupt light), the potential difference of segment output and common output becomes VLCD0 level. When the LCD segment is OFF (It penetrate light), the potential difference of segment output and common output becomes 1/4 VLCD0 level. This drive method assigns a eighth of a frame to control of ON/OFF of one segments. Thus, this drive method is called the “1/8 duty and 1/4 bias drive”. When set the 1/8 duty, the 1/4 bias and the frame inversion drive mode, the following figure shows the LCD drive waveform.

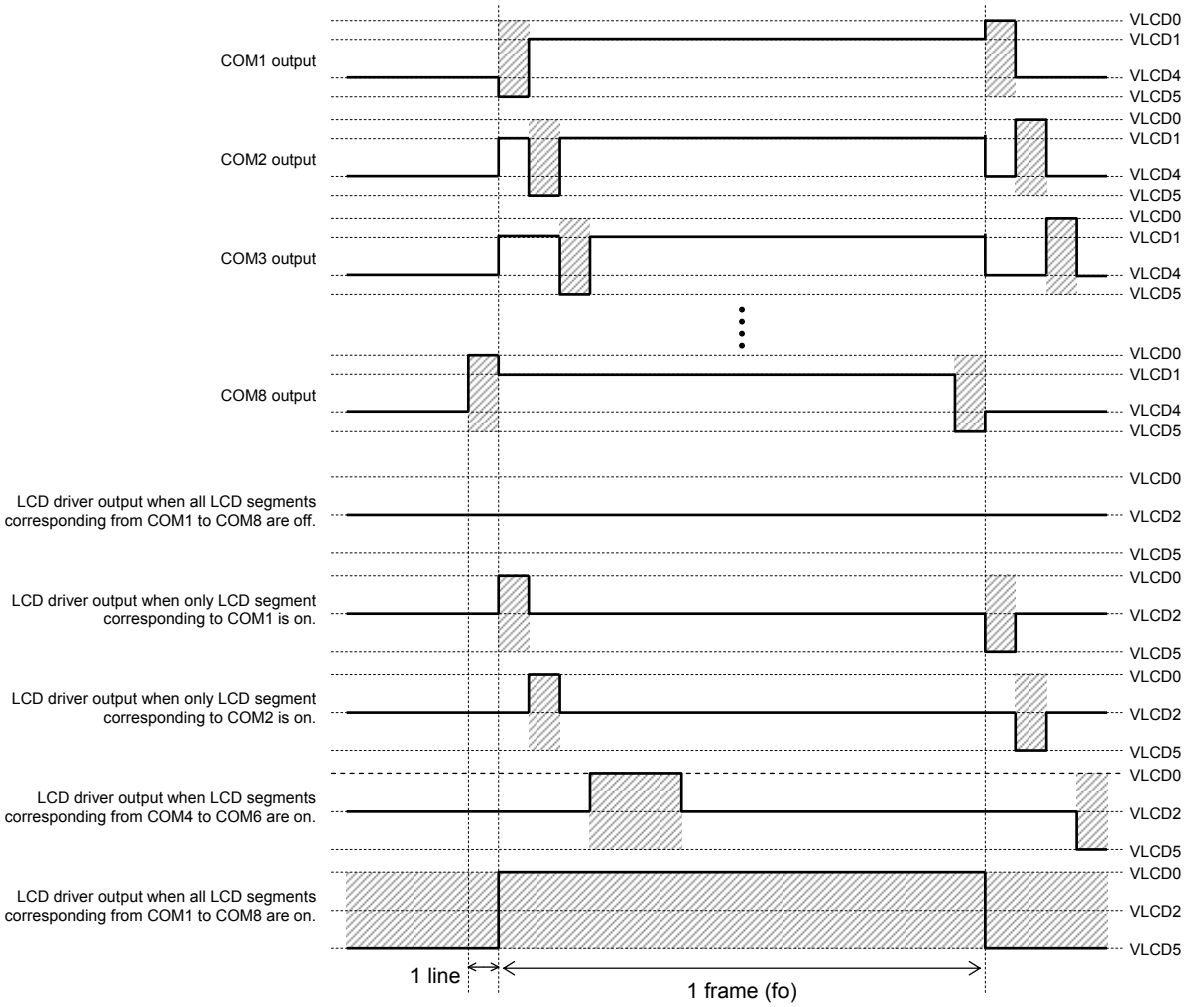


Figure 9. When the 1/8 duty, the 1/4 bias and the frame inversion are set, waveform of the LCD driver output

(2) Setting of the LCD Drive Duty (DT0 to DT3)

The control data from DT0 to DT3 can set the LCD drive duty from 1/8 to 1/16. The customer can select the LCD drive duty by the specifications of an LCD panel used. This LCD system configuration example is using LCD panel of the 1/8 duty. Therefore, this system sets DT0="0", DT1="0", DT2="0" and DT3="0". The COM signal not used outputs an off waveform.

DT0	DT1	DT2	DT3	LCD drive duty type	The state of COM1 to COM16			
					Pads which output scan pulse		Pads which output pulse of display off	
					Normal scan CDIR="0"	Reversed scan CDIR="1"	Normal scan CDIR="0"	Reversed scan CDIR="1"
0	**0**	**0**	**0**	**1/8 duty**	**COM1 to COM8**	**COM16 to COM9**	**COM9 to COM16**	**COM8 to COM1**
1	0	0	0	1/9 duty	COM1 to COM9	COM16 to COM8	COM10 to COM16	COM7 to COM1
0	1	0	0	1/10 duty	COM1 to COM10	COM16 to COM7	COM11 to COM16	COM6 to COM1
1	1	0	0	1/11 duty	COM1 to COM11	COM16 to COM6	COM12 to COM16	COM5 to COM1
0	0	1	0	1/12 duty	COM1 to COM12	COM16 to COM5	COM13 to COM16	COM4 to COM1
1	0	1	0	1/13 duty	COM1 to COM13	COM16 to COM4	COM14 to COM16	COM3 to COM1
0	1	1	0	1/14 duty	COM1 to COM14	COM16 to COM3	COM15, COM16	COM2, COM1
1	1	1	0	1/15 duty	COM1 to COM15	COM16 to COM2	COM16	COM1
X	X	X	1	1/16 duty	COM1 to COM16	COM16 to COM1	---	---

X : Don't care (0 or 1)

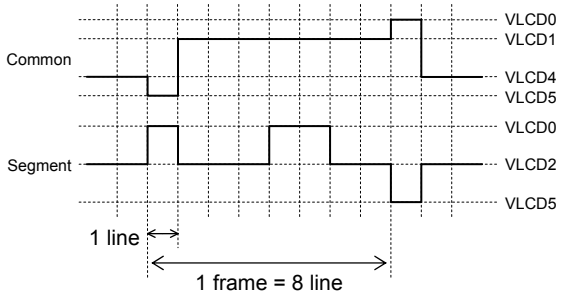


Figure 10. LCD drive waveform when 1/8 duty

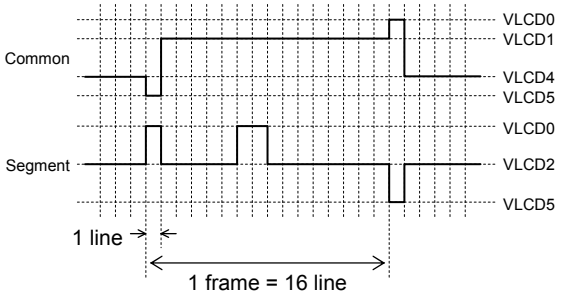


Figure 11. LCD drive waveform when 1/16 duty

(3) Setting of the LCD Drive Bias (DR)

The control data of the DR can set the 1/4 bias or 1/5 bias. Typically, the optimum LCD drive bias (maximum contrast) is determined according to an LCD drive duty, and it shown in the following equations. The customer can select the LCD drive bias by the specifications of an LCD panel used. This LCD system configuration example sets DR="0" to use the 1/4 bias.

Equations : $\sqrt{(\text{duty})} + 1$

For example, this LCD system configuration example is using LCD panel of 1/8 duty. Hence, $\sqrt{8} + 1 = 3.82 \Rightarrow 4$

DR	LCD drive bias type	The state from VLCD0 to VLCD5					
		VLCD0	VLCD1	VLCD2	VLCD3	VLCD4	VLCD5
0	**1/4 bias**	**VLCD0**	**3/4 VLCD0**	**2/4 VLCD0**	**Make sure to open VLCD3**	**1/4 VLCD0**	**VSS**
1	1/5 bias	VLCD0	4/5 VLCD0	3/5 VLCD0	2/5 VLCD0	1/5 VLCD0	VSS

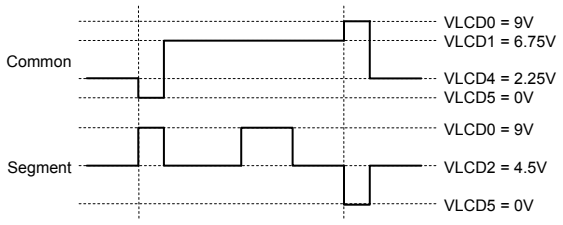


Figure 12. LCD drive waveform when 1/4 bias

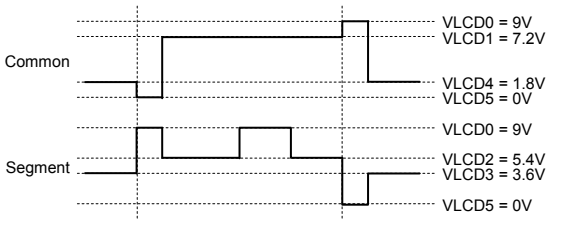


Figure 13. LCD drive waveform when 1/5 bias

(4) Setting of the Inversion Drive for LCD Drive Waveforms (WVC)

The control data of the WVC can set the line inversion or frame inversion. Typically, the line inversion drive can do display of high contrast, but there is more power consumption than frame inversion drive. In addition, the frame inversion drive is low little power consumption, but contrast decreases than line inversion drive. Therefore, the customer can select the inversion drive type by a purpose and the characteristic of the LCD panel used.

This LCD system configuration example sets WVC="1" to use the frame inversion.

WVC	Inversion drive type of LCD drive waveforms
0	Line inversion
1	**Frame inversion**

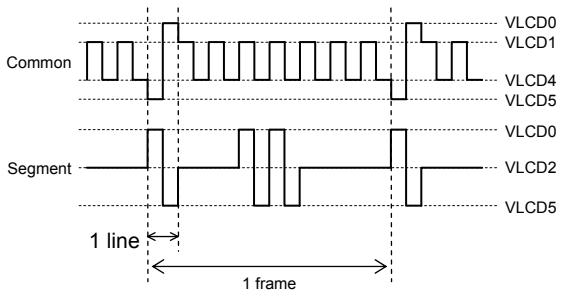


Figure 14. LCD drive waveform when line inversion

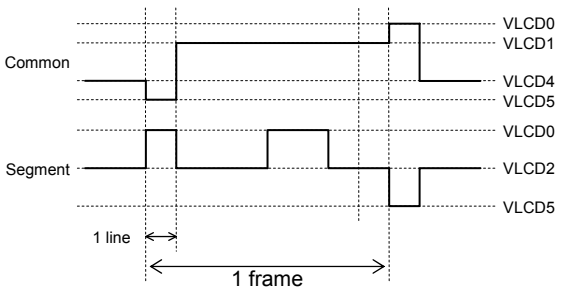


Figure 15. LCD drive waveform when frame inversion

(5) Setting of the Scan Direction for the Common Output (CDIR)

The control data of the CDIR can set the normal scan direction or reverse scan direction. Typically, the scan direction is a bottom from the top. The customer can select the scan direction for the common output by the mounted LSI position and the direction of the LCD panel. The SDIR and CDIR are often set in combination. This LCD system configuration example sets CDIR="0".

CDIR	Scan direction	Scan sequence
0	**Normal scan**	**COM1 => COM2 => COM3 => ..... => COM7 =>COM8**
1	Reverse scan	COM16 => COM15 => COM14 => ..... => COM10 => COM9

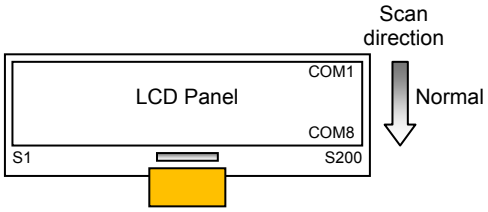


Figure 16. When LSI is mounted to become the normal scan direction

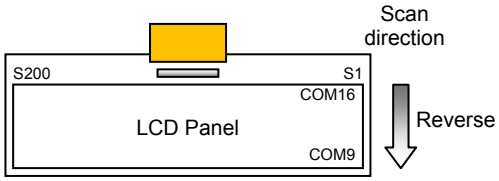


Figure 17. When LSI is mounted to become the reverse scan direction

(6) Setting of the Correspondence of a Segment Output and a Column Address of RAM (SDIR)

The control data of the SDIR can set the correspondence relation between a column address of the display data RAM and a segment output. The customer can select the correspondence relation between a column address of the display data RAM and a segment output by the mounted LSI position and the direction of the LCD panel. The SDIR and CDIR are often set in combination.

The display of LCD does not change by only changing the setting of SDIR data. When display data is written to RAM, column address of the display data RAM is converted. Then display data is saved to there.

This LCD system configuration example sets SDIR="0".

SDIR	Direction corresponding to the segment output	Correspondence relation between a column address of the display data RAM and a segment output
0	**Normal direction**	**The segment output of S1 corresponds to a column address (CRA0 to CRA7) of 00H, and the segment output of S200 corresponds to a column address (CRA0 to CRA7) of C7H.**
1	Reverse direction	The segment output of S1 corresponds to a column address (CRA0 to CRA7) of C7H, and the segment output of S200 corresponds to a column address (CRA0 to CRA7) of 00H.

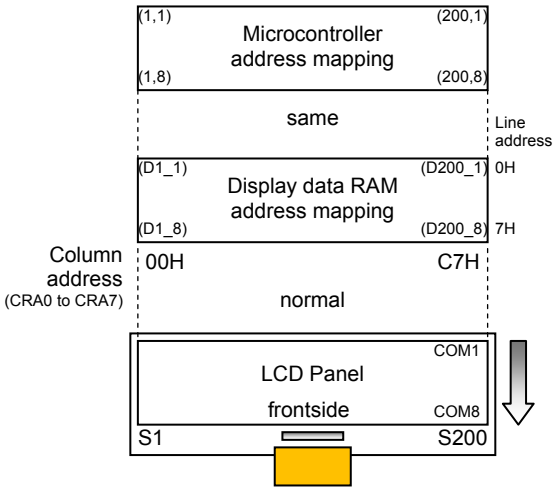


Figure 18. When LSI is mounted to become the normal direction corresponding to the segment output

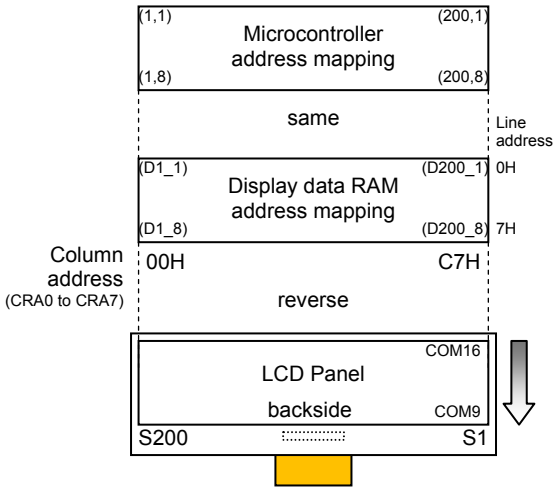


Figure 19. When LSI is mounted to become the reverse direction corresponding to the segment output

(7) Setting of the ON/OFF Reverse Display (PNC)

The control data of the PNC can set the normal display mode or the reverse display mode. When display states are normal mode (SC0="0", SC1="0"), the setting of PNC becomes effective. There are two kinds of an LCD panels: normally-white and normally-black. When the normally-black LCD panel, the display data of the microcontroller are same and can display correctly by setting this PNC to "1".

PNC	Display state	When display data (Dn_m) are set to "0"	When display data (Dn_m) are set to "1"
0	Normal mode	The segment is OFF display	The segment is ON display
1	Reverse display mode	The segment is ON display	The segment is OFF display

Note : Display data "Dn_m" is from D1_1 to D200_16.

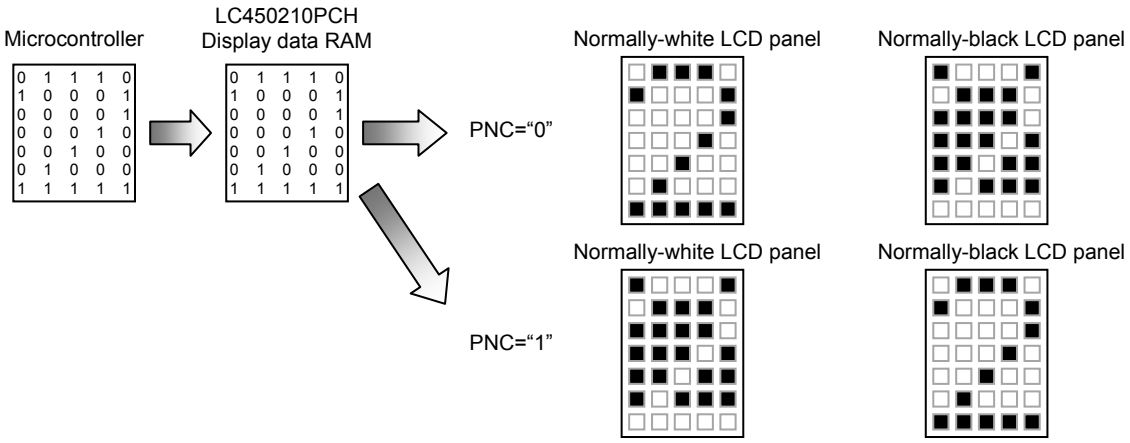


Figure 20. Relations of display data and the LCD panel display

(8) Setting of the Display State (SC0, SC1)

The control data of the SC0 and SC1 can set the normal mode, the display OFF mode, the display ON mode or the display forced OFF mode. When the display forced OFF mode, the segment outputs and the common outputs are outputted to VLCD5 level. Therefore, this setting is used to discharge the capacity of the liquid crystal display cell.

SC0	SC1	Display state	Segment outputs state (from S1 to S200)	Common outputs state (from COM1 to COM16)
0	0	Normal mode (Displayable)	Waveform corresponding to the display data	Scan pulse
1	0	Display OFF mode	OFF waveform	Scan pulse
0	1	Display ON mode	ON waveform	Scan pulse
1	1	Display forced OFF mode	VLCD5 level	VLCD5 level

(9) Setting of the Power Saving Mode (BU)

The control data of the BU can set the normal mode or power saving mode. When the power saving mode is set, all the internal circuits are stopped, and it becomes a low power consumption state. The LCD is not displayed then.

BU	Low power consumption mode	Internal operating conditions
0	Normal mode	Normal mode
1	Power saving mode	• Segment outputs (S1 to S200) are VLCD5 level. • Common outputs (COM1 to COM16) are VLCD5 level. • LCD driver block power supply output (VLCD) is same as VBTI1 level • LCD drive bias voltage outputs (from VLCD0 to VLCD4) are same as VLCD5 level. • The internal oscillator circuit is stopped. • External clock input is not received. • The voltage booster circuit is stopped and discharge state. • The contrast adjuster circuit is stopped and discharge state. • The LCD drive bias voltage generator circuit is stopped and discharge state. • The reception of serial data is possible. (Registers are updated)

(10) Setting of the line address of RAM (LNA0 to LNA3)

The control data from LNA0 to LNA3 can set a line address of RAM. The common address circuit is reset at the trigger of internal frame signal, and this circuit counts up synchronized with the scanning signal. Therefore, generates common address by this circuit. The common address increases from the top of the display line to the number of display lines set by control data of the LCD drive duty (DT0 to DT3). When the scan direction is set to normal scan (CDIR="0"), the common address begins outputting from COM1. When the scan direction is set to reverse scan (CDIR="1"), the common address begins outputting from COM16.

The RAM data of 200 bits on the line address set by the line counter are read from display data RAM. And these RAM data is latched to the display data latch. A controller writing to the display data RAM and the this LSI reading from the display data latch operate independently. Therefore, even if data is rewritten with the asynchronous, the display is not influenced. This LCD system configuration example sets LNA0="0", LNA1="0", LNA2="0" and LNA3="0" to begin to read it from a line address of "0H".

Table 6. Display data RAM address mapping when a line address (LNA0 to LNA3) is set to "0H"

		Segment outputs												
Normal direction (SDIR=0)		S1	S2	S3	S4	·····	S197	S198	S199	S200			Common address	**Normal direction (CDIR=0)**
Page address	PGA=0	D1_1	D2_1	D3_1	D4_1	·····	D197_1	D198_1	D199_1	D200_1	**0H**	**Line address LNA0 to LNA3**	**0H**	**COM1**
		D1_2	D2_2	D3_2	D4_2	·····	D197_2	D198_2	D199_2	D200_2	1H		1H	COM2
		D1_3	D2_3	D3_3	D4_3	·····	D197_3	D198_3	D199_3	D200_3	2H		2H	COM3
		D1_4	D2_4	D3_4	D4_4	·····	D197_4	D198_4	D199_4	D200_4	3H		3H	COM4
		D1_5	D2_5	D3_5	D4_5	·····	D197_5	D198_5	D199_5	D200_5	4H		4H	COM5
		D1_6	D2_6	D3_6	D4_6	·····	D197_6	D198_6	D199_6	D200_6	5H		5H	COM6
		D1_7	D2_7	D3_7	D4_7	·····	D197_7	D198_7	D199_7	D200_7	6H		6H	COM7
		D1_8	D2_8	D3_8	D4_8	·····	D197_8	D198_8	D199_8	D200_8	7H		7H	COM8
	PGA=1	D1_9	D2_9	D3_9	D4_9	·····	D197_9	D198_9	D199_9	D200_9	8H			
		D1_10	D2_10	D3_10	D4_10	·····	D197_10	D198_10	D199_10	D200_10	9H			
		D1_11	D2_11	D3_11	D4_11	·····	D197_11	D198_11	D199_11	D200_11	AH			
		D1_12	D2_12	D3_12	D4_12	·····	D197_12	D198_12	D199_12	D200_12	BH			
		D1_13	D2_13	D3_13	D4_13	·····	D197_13	D198_13	D199_13	D200_13	CH			
		D1_14	D2_14	D3_14	D4_14	·····	D197_14	D198_14	D199_14	D200_14	DH			
		D1_15	D2_15	D3_15	D4_15	·····	D197_15	D198_15	D199_15	D200_15	EH			
		D1_16	D2_16	D3_16	D4_16	·····	D197_16	D198_16	D199_16	D200_16	FH			
		00H	01H	02H	03H	·····	C4H	C5H	C6H	C7H				
		Column address CRA0 to CRA7												

Start

Table 7. Display data RAM address mapping when a line address (LNA0 to LNA3) is set to "4H"

		Segment outputs												
Normal direction (SDIR=0)		S1	S2	S3	S4	·····	S197	S198	S199	S200			Common address	**Normal direction (CDIR=0)**
Page address	PGA=0	D1_1	D2_1	D3_1	D4_1	·····	D197_1	D198_1	D199_1	D200_1	0H	**Line address LNA0 to LNA3**	**0H**	**COM1**
		D1_2	D2_2	D3_2	D4_2	·····	D197_2	D198_2	D199_2	D200_2	1H		1H	COM2
		D1_3	D2_3	D3_3	D4_3	·····	D197_3	D198_3	D199_3	D200_3	2H		2H	COM3
		D1_4	D2_4	D3_4	D4_4	·····	D197_4	D198_4	D199_4	D200_4	3H		3H	COM4
		D1_5	D2_5	D3_5	D4_5	·····	D197_5	D198_5	D199_5	D200_5	**4H**		4H	COM5
		D1_6	D2_6	D3_6	D4_6	·····	D197_6	D198_6	D199_6	D200_6	5H		5H	COM6
		D1_7	D2_7	D3_7	D4_7	·····	D197_7	D198_7	D199_7	D200_7	6H		6H	COM7
		D1_8	D2_8	D3_8	D4_8	·····	D197_8	D198_8	D199_8	D200_8	7H		7H	COM8
	PGA=1	D1_9	D2_9	D3_9	D4_9	·····	D197_9	D198_9	D199_9	D200_9	8H			
		D1_10	D2_10	D3_10	D4_10	·····	D197_10	D198_10	D199_10	D200_10	9H			
		D1_11	D2_11	D3_11	D4_11	·····	D197_11	D198_11	D199_11	D200_11	AH			
		D1_12	D2_12	D3_12	D4_12	·····	D197_12	D198_12	D199_12	D200_12	BH			
		D1_13	D2_13	D3_13	D4_13	·····	D197_13	D198_13	D199_13	D200_13	CH			
		D1_14	D2_14	D3_14	D4_14	·····	D197_14	D198_14	D199_14	D200_14	DH			
		D1_15	D2_15	D3_15	D4_15	·····	D197_15	D198_15	D199_15	D200_15	EH			
		D1_16	D2_16	D3_16	D4_16	·····	D197_16	D198_16	D199_16	D200_16	FH			
		00H	01H	02H	03H	·····	C4H	C5H	C6H	C7H				
		Column address CRA0 to CRA7												

Start

Table 8. Display data RAM address mapping when a line address (LNA0 to LNA3) is set to “0H”

Normal direction (SDIR=0)		Segment outputs S1	S2	S3	S4	·····	S197	S198	S199	S200		Line address LNA0 to LNA3
Page address	PGA=0	D1_1	D2_1	D3_1	D4_1	·····	D197_1	D198_1	D199_1	D200_1	**0H**	
		D1_2	D2_2	D3_2	D4_2	·····	D197_2	D198_2	D199_2	D200_2	1H	
		D1_3	D2_3	D3_3	D4_3	·····	D197_3	D198_3	D199_3	D200_3	2H	
		D1_4	D2_4	D3_4	D4_4	·····	D197_4	D198_4	D199_4	D200_4	3H	
		D1_5	D2_5	D3_5	D4_5	·····	D197_5	D198_5	D199_5	D200_5	4H	
		D1_6	D2_6	D3_6	D4_6	·····	D197_6	D198_6	D199_6	D200_6	5H	
		D1_7	D2_7	D3_7	D4_7	·····	D197_7	D198_7	D199_7	D200_7	6H	
		D1_8	D2_8	D3_8	D4_8	·····	D197_8	D198_8	D199_8	D200_8	7H	
	PGA=1	D1_9	D2_9	D3_9	D4_9	·····	D197_9	D198_9	D199_9	D200_9	8H	
		D1_10	D2_10	D3_10	D4_10	·····	D197_10	D198_10	D199_10	D200_10	9H	
		D1_11	D2_11	D3_11	D4_11	·····	D197_11	D198_11	D199_11	D200_11	AH	
		D1_12	D2_12	D3_12	D4_12	·····	D197_12	D198_12	D199_12	D200_12	BH	
		D1_13	D2_13	D3_13	D4_13	·····	D197_13	D198_13	D199_13	D200_13	CH	
		D1_14	D2_14	D3_14	D4_14	·····	D197_14	D198_14	D199_14	D200_14	DH	
		D1_15	D2_15	D3_15	D4_15	·····	D197_15	D198_15	D199_15	D200_15	EH	
		D1_16	D2_16	D3_16	D4_16	·····	D197_16	D198_16	D199_16	D200_16	FH	
		00H	01H	02H	03H	·····	C4H	C5H	C6H	C7H		
		Column address CRA0 to CRA7										

Start

Common address	**Reverse direction (CDIR=1)**
0H	**COM16**
1H	COM15
2H	COM14
3H	COM13
4H	COM12
5H	COM11
6H	COM10
7H	COM9

Table 9. Display data RAM address mapping when a line address (LNA0 to LNA3) is set to “4H”

Normal direction (SDIR=0)		Segment outputs S1	S2	S3	S4	·····	S197	S198	S199	S200		Line address LNA0 to LNA3
Page address	PGA=0	D1_1	D2_1	D3_1	D4_1	·····	D197_1	D198_1	D199_1	D200_1	0H	
		D1_2	D2_2	D3_2	D4_2	·····	D197_2	D198_2	D199_2	D200_2	1H	
		D1_3	D2_3	D3_3	D4_3	·····	D197_3	D198_3	D199_3	D200_3	2H	
		D1_4	D2_4	D3_4	D4_4	·····	D197_4	D198_4	D199_4	D200_4	3H	
		D1_5	D2_5	D3_5	D4_5	·····	D197_5	D198_5	D199_5	D200_5	**4H**	
		D1_6	D2_6	D3_6	D4_6	·····	D197_6	D198_6	D199_6	D200_6	5H	
		D1_7	D2_7	D3_7	D4_7	·····	D197_7	D198_7	D199_7	D200_7	6H	
		D1_8	D2_8	D3_8	D4_8	·····	D197_8	D198_8	D199_8	D200_8	7H	
	PGA=1	D1_9	D2_9	D3_9	D4_9	·····	D197_9	D198_9	D199_9	D200_9	8H	
		D1_10	D2_10	D3_10	D4_10	·····	D197_10	D198_10	D199_10	D200_10	9H	
		D1_11	D2_11	D3_11	D4_11	·····	D197_11	D198_11	D199_11	D200_11	AH	
		D1_12	D2_12	D3_12	D4_12	·····	D197_12	D198_12	D199_12	D200_12	BH	
		D1_13	D2_13	D3_13	D4_13	·····	D197_13	D198_13	D199_13	D200_13	CH	
		D1_14	D2_14	D3_14	D4_14	·····	D197_14	D198_14	D199_14	D200_14	DH	
		D1_15	D2_15	D3_15	D4_15	·····	D197_15	D198_15	D199_15	D200_15	EH	
		D1_16	D2_16	D3_16	D4_16	·····	D197_16	D198_16	D199_16	D200_16	FH	
		00H	01H	02H	03H	·····	C4H	C5H	C6H	C7H		
		Column address CRA0 to CRA7										

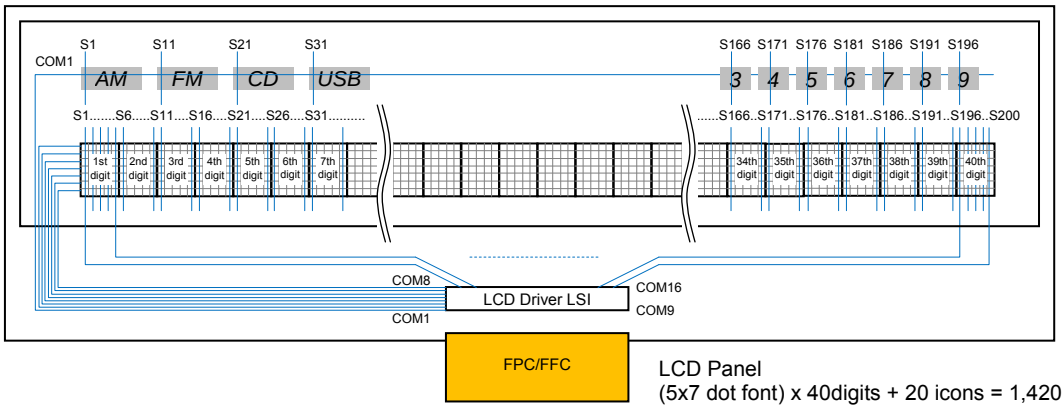
Start

Common address	**Reverse direction (CDIR=1)**
0H	**COM16**
1H	COM15
2H	COM14
3H	COM13
4H	COM12
5H	COM11
6H	COM10
7H	COM9

Explanations of How to Write a Display Data RAM

(1) LCD panel segment allotment

This LCD system configuration example uses the LCD panel of the segment allotment as shown below. When the LCD panel of 1/8 duty is used, the customer sets a page address (PGA) and a column address (CRA0 to CRA7) by “Write display data to RAM (8 x 15 bits in a lump)” instruction, and display data of 120 bits (8 common outputs x 15 segment outputs)” is written to the display data RAM in a lump.



	Segment outputs														
Normal direction (SDIR=0)	S1	·····	S5	S6	·····	S10	S11	·····	S15	S16	·····	S195	S196	·····	S200
Page address PGA=0	**D1_1 (AM)**	·····	D5_1	D6_1	·····	D10_1	**D11_1 (FM)**	·····	D15_1	D16_1	·····	D195_1	**D196_1 (9)**	·····	D200_1
	D1_2	·····	**D5_2**	**D6_2**	·····	**D10_2**	**D11_2**	·····	**D15_2**	**D16_2**	·····	**D195_2**	**D196_2**	·····	**D200_2**
	D1_3	·····	**D5_3**	**D6_3**	·····	**D10_3**	**D11_3**	·····	**D15_3**	**D16_3**	·····	**D195_3**	**D196_3**	·····	**D200_3**
	D1_4	·····	**D5_4**	**D6_4**	·····	**D10_4**	**D11_4**	·····	**D15_4**	**D16_4**	·····	**D195_4**	**D196_4**	·····	**D200_4**
	D1_5	·····	**D5_5**	**D6_5**	·····	**D10_5**	**D11_5**	·····	**D15_5**	**D16_5**	·····	**D195_5**	**D196_5**	·····	**D200_5**
	D1_6	·····	**D5_6**	**D6_6**	·····	**D10_6**	**D11_6**	·····	**D15_6**	**D16_6**	·····	**D195_6**	**D196_6**	·····	**D200_6**
	D1_7	·····	**D5_7**	**D6_7**	·····	**D10_7**	**D11_7**	·····	**D15_7**	**D16_7**	·····	**D195_7**	**D196_7**	·····	**D200_7**
	D1_8	·····	**D5_8**	**D6_8**	·····	**D10_8**	**D11_8**	·····	**D15_8**	**D16_8**	·····	**D195_8**	**D196_8**	·····	**D200_8**
Page address PGA=1	D1_9	·····	D3_9	D4_9	·····	D10_9	D11_9	·····	D15_9	D16_9	·····	D195_9	D196_9	·····	D200_9
	D1_10	·····	D3_10	D4_10	·····	D10_10	D11_10	·····	D15_10	D16_10	·····	D195_10	D196_10	·····	D200_10
	D1_11	·····	D3_11	D4_11	·····	D10_11	D11_11	·····	D15_11	D16_11	·····	D195_11	D196_11	·····	D200_11
	D1_12	·····	D3_12	D4_12	·····	D10_12	D11_12	·····	D15_12	D16_12	·····	D195_12	D196_12	·····	D200_12
	D1_13	·····	D3_13	D4_13	·····	D10_13	D11_13	·····	D15_13	D16_13	·····	D195_13	D196_13	·····	D200_13
	D1_14	·····	D3_14	D4_14	·····	D10_14	D11_14	·····	D15_14	D16_14	·····	D195_14	D196_14	·····	D200_14
	D1_15	·····	D3_15	D4_15	·····	D10_15	D11_15	·····	D15_15	D16_15	·····	D195_15	D196_15	·····	D200_15
	D1_16	·····	D3_16	D4_16	·····	D10_16	D11_16	·····	D15_16	D16_16	·····	D195_16	D196_16	·····	D200_16
Allotment	1st digit			2nd digit			3rd digit			4th digit		39th digit	40th digit		
	00H	·····	04H	05H	·····	09H	0AH	·····	0EH	0FH	·····	C3H	C4H	·····	C7H
	Column address CRA0 to CRA7														

Figure 21. Relations between an LCD panel and the segment of the LCD driver LSI

(2) Setting of the column address (CRA0 to CRA7)

The control data from CRA0 to CRA7 can set a column address of RAM. The settable range of a column address from CRA0 to CRA7 are from “00H” to “C7H”. When a column address is set more than “BAH”, display data is written from start position and the overflowed data from RAM is canceled.

(3) Setting of the page address (PGA)

The control data of the PGA can set a page address of RAM. When the display data of 120 bits are written to the display data RAM in a lump by “Write display data to RAM (8 x 15 bits in a lump)” instruction, the recommended setting of the page address (PGA) is “0”, and the display data is written from start position. At this time, the overflowed data from RAM is canceled.

(4) Setting of the display data which are written to RAM (Dn_m, Dn_m+1 to Dn+14_m+7)

The control data from Dn_m to Dn+14_m+7 can set a display data which are written to RAM. The start position of writing to RAM is set by the data from CRA0 to CRA7 and PGA. At this time, note that the overflowing data from RAM is canceled by the setting from CRA0 to CRA7 and PGA.

Table 10. How to write a display data in an LCD panel used in this LCD system configuration example

Instruction data bit number	D128	D129	D130	…	D247	D248	…	D255	D256	D257	D258	D259	D260	D261	D262	D263	D264
Allotment	Dn_m	Dn_ m+1	Dn_ m+2	…	Dn+14_ +m+7	0	…	0	CRA0	CRA1	CRA2	CRA3	CRA4	CRA5	CRA6	CRA7	PGA
1st to 3rd digit +AM, FM icon	D1_1 (AM)	D1_2	D1_3	…	D15_8	0	…	0	0	0	0	0	0	0	0	0	0
4th to 6th digit +CD icon	D16_1	D16_2	D16_3	…	D30_8	0	…	0	1	1	1	1	0	0	0	0	0
7th to 9th digit +USB, AUTO icon	D31_1 (USB)	D31_2	D31_3	…	D45_8	0	…	0	0	1	1	1	1	0	0	0	0
10th to 12th digit +SCN icon	D46_1	D46_2	D46_3	…	D60_8	0	…	0	1	0	1	1	0	1	0	0	0
13th to 15th digit +RPT icon	D61_1	D61_2	D61_3	…	D75_8	0	…	0	0	0	1	1	1	1	0	0	0
16th to 18th digit +RDM icon	D74_1	D74_2	D74_3	…	D90_8	0	…	0	1	1	0	1	0	0	1	0	0
19th to 21th digit +XXX icon	D91_1	D91_2	D91_3	…	D105_8	0	…	0	0	1	0	1	1	0	1	0	0
22th to 24th digit +YYY icon	D106_1	D106_2	D106_3	…	D120_8	0	…	0	1	0	0	1	0	1	1	0	0
25th to 27th digit +ZZZ icon	D121_1	D121_2	D121_3	…	D135_8	0	…	0	0	0	0	1	1	1	1	0	0
28th to 30th digit	D136_1	D136_2	D136_3	…	D150_8	0	…	0	1	1	1	0	0	0	0	1	0
31th to 33th digit +1, 2 icon	D151_1	D151_2	D151_3	…	D165_8	0	…	0	0	1	1	0	1	0	0	1	0
34th to 36th digit +3, 4, 5 icon	D166_1 (3)	D166_2	D166_3	…	D180_8	0	…	0	1	0	1	0	0	1	0	1	0
37th to 39th digit +6, 7, 8 icon	D181_1 (6)	D181_2	D181_3	…	D195_8	0	…	0	0	0	1	0	1	1	0	1	0
40th digit +9 icon	D196_1 (9)	D197_2	D198_3	…	0	0	…	0	1	1	0	0	0	0	1	1	0

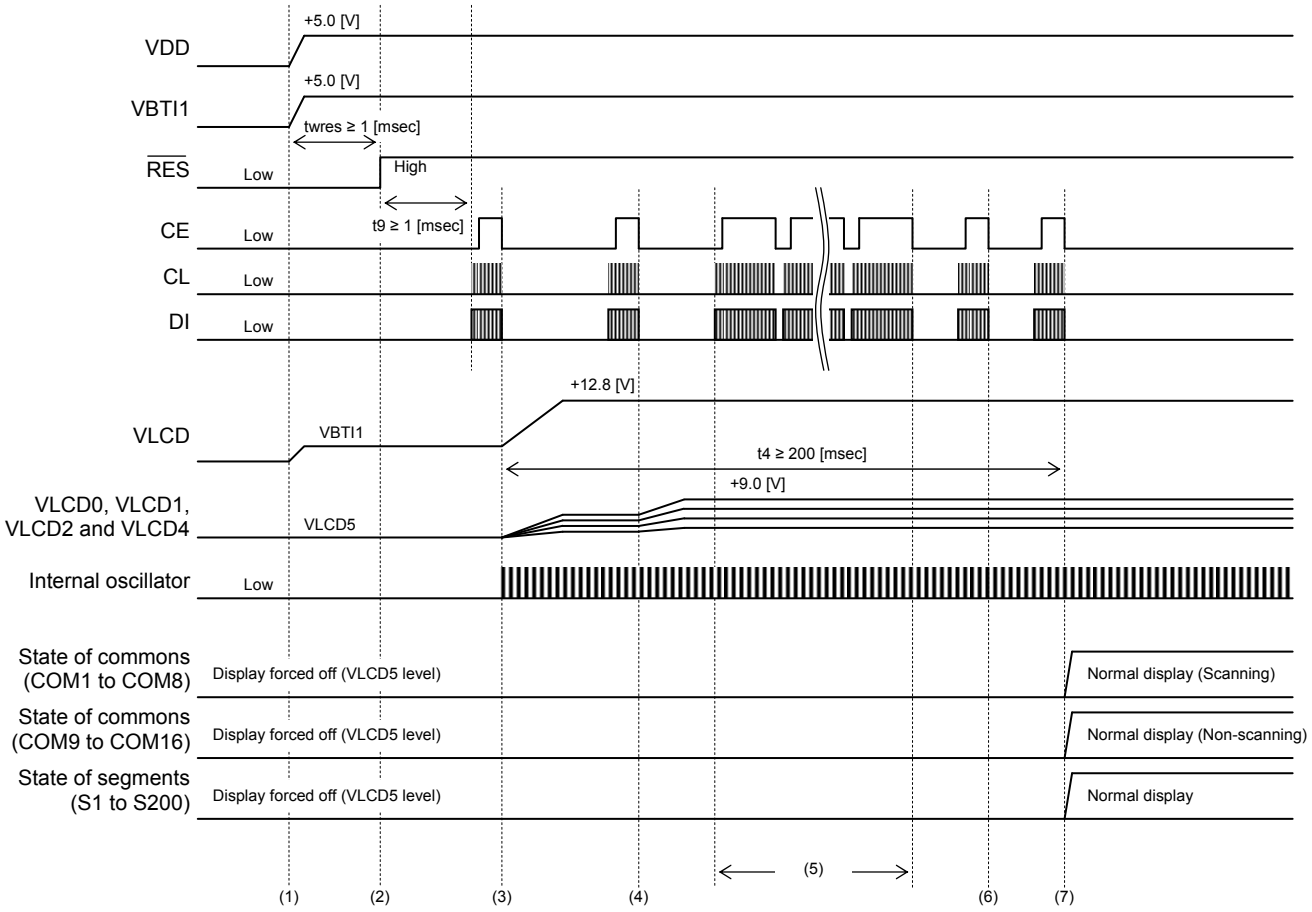
Note : The display data of the icon are assigned to D1_1(AM), D11_1(FM), D21_1(CD), D31_1(USB), D41_1(AUTO), D56_1(SCN), D71_1(RPT), D86_1(RDM), D101_1(XXX), D116_1(YYY), D131_1(ZZZ), D156_1(1), D161_1(2), D166_1(3), D171_1(4), D176_1(5), D181_1(6), D186_1(7), D191_1(8), D196_1(9), and other bits are set to “0”.

Dn_m, Dn_m+1 to Dn+14_m+7 : A display data which are written to RAM.
CRA0 to CRA7 : Control data to set a column address of RAM.
PGA : Control data to set a page address of RAM.

Software Control Example of the LCD Controller

(1) Timing Chart from Power-on State to LCD Display ON

First, the following figure shows the timing waveform from power-on state to initial setting and LCD display ON in this LCD system configuration example.

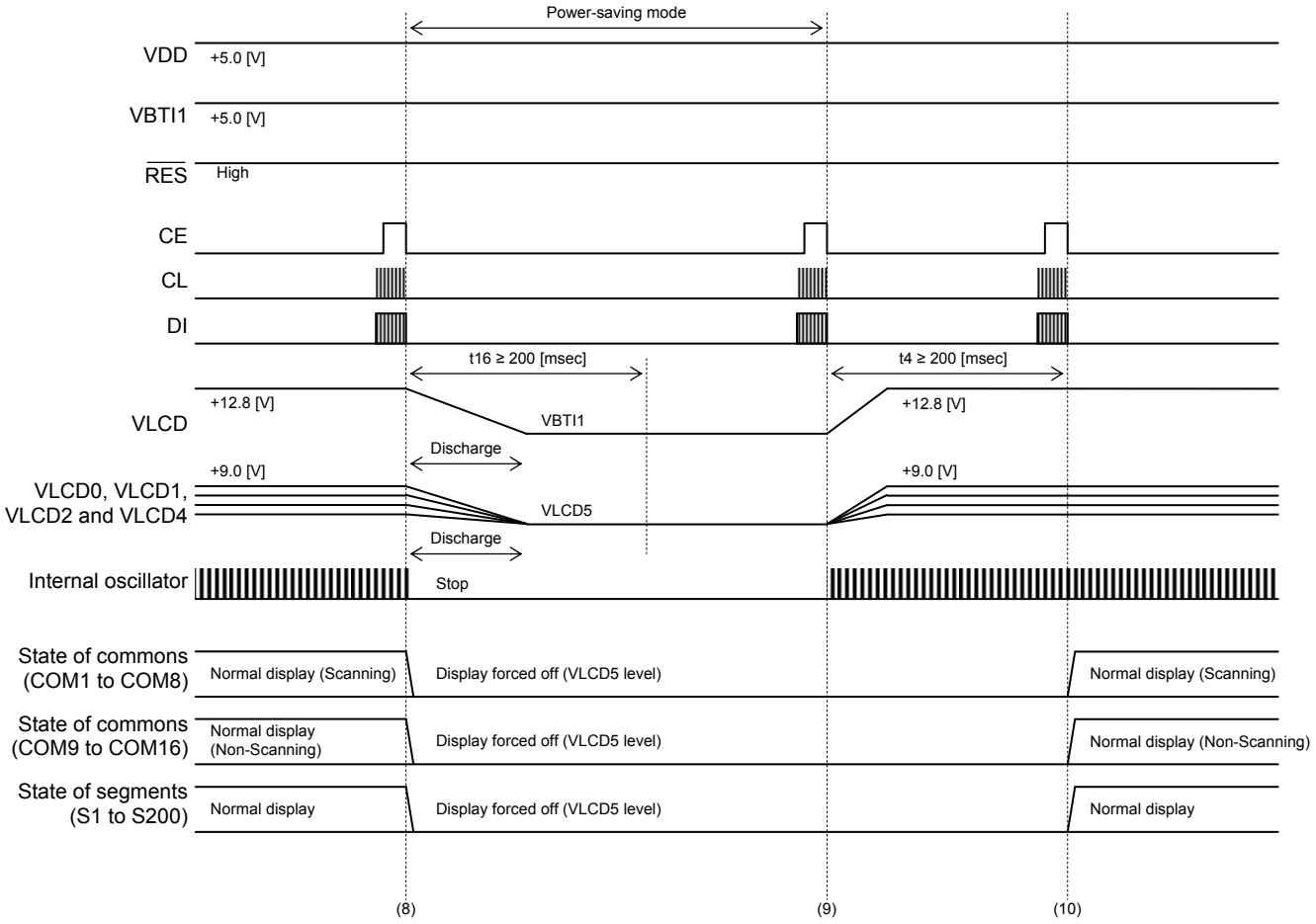


< Operation sequence >

(1) Power-on. Please input the 5V signal into CE, CL, DI, $\overline{RES}$ and OSCI by all means to prevent the destruction of these input pads after a logic power supply (VDD) was turned on.
(2) The $\overline{RES}$ signal is set to High level.
(3) The instruction of initial setting is transferred after passage of the “Wait time for inputting of serial data: t9 ≥ 1 [msec]”. Make sure to execute “Set of display method” instruction first. The “Set of display method” instruction is executed. (OC=0, DBC=1, CTC0=1, CTC1=1, DT0=0, DT1=0, DT2=0, DT3=0, DR=0, WVC=1, CDIR=0, SDIR=0, DBF0=0, DBF1=1, DBF2=1, FC0=0, FC1=1, FC2=0, FC3=0)
(4) The “Set of display contrast” instruction is executed. (CT0=0, CT1=1, CT2=0, CT3=0, CT4=0, CT5=1)
(5) The “Write display data to RAM (8x15 bits in a lump)” instructions are executed.
(6) The “Set of line address” instruction is executed. (LNA0=0, LNA1=0, LNA2=0 ,LNA3=0)
(7) The instruction of display ON setting is transferred after passage of the “Stabilization time of voltage booster, contrast adjuster and LCD drive bias voltage generator: t4 ≥ 200 [msec]” from operation sequence (3). The “Control of display ON / OFF” instruction is executed. (PNC=0, SC0=0, SC1=0, BU=0)

(2) Timing Chart Power-Saving Mode is Set and Canceled

The following figure shows the timing waveform from normal display state to power-saving mode setting and from power-saving mode state to normal display setting in this LCD system configuration example.



< Operation sequence >

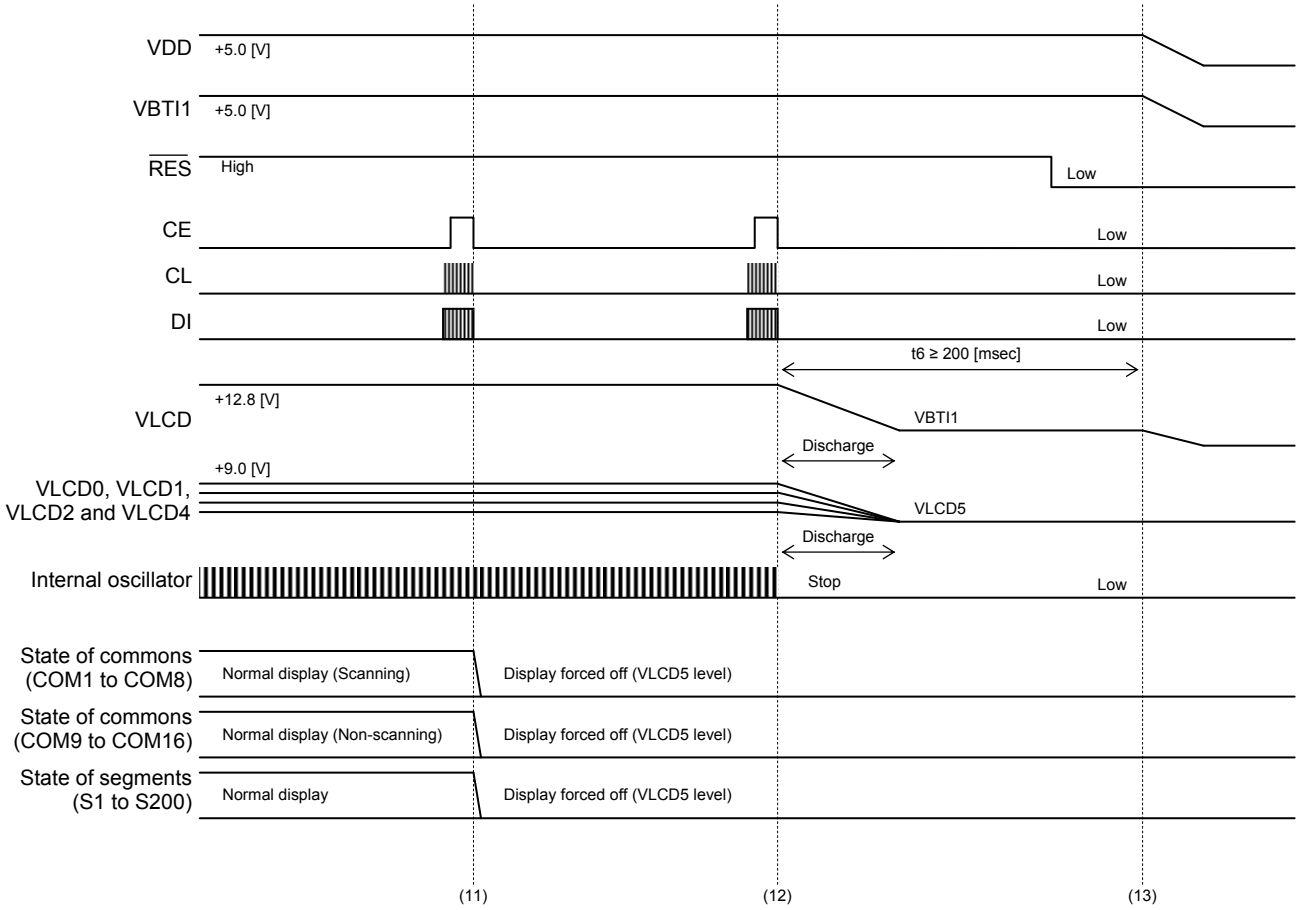
(8) The instruction of the power saving mode setting is transferred. The “Control of display ON / OFF” instruction is executed (PNC=0, SC0=1, SC1=1, BU=1). The output of these circuits becomes the discharge condition by the setting of the power saving mode (BU=1) because the voltage booster, the contrast adjuster and the LCD drive bias voltage generator are set to run state (DBC=1, CTC0=1, CTC1=1).

(9) The instruction of the power saving mode cancellation setting is transferred. The “Control of display ON / OFF” instruction is executed. (PNC=0, SC0=1, SC1=1, BU=0)

(10) The instruction of display ON setting is transferred after passage of the “Stabilization time of voltage booster, contrast adjuster and LCD drive bias voltage generator: t4 ≥ 200 [msec]” from operation sequence (9). The “Control of display ON / OFF” instruction is executed. (PNC=0, SC0=0, SC1=0, BU=0)

(3) Timing Chart from Normal Display to Power-off State

The following figure shows the timing waveform set from normal display to power-off state.



< Operation sequence >

(11) The instruction of display OFF setting is transferred. The “Control of display ON / OFF” instruction is executed. (PNC=0, SC0=1, SC1=1, BU=0) In addition, the customer can be set by one instruction transfer at the same time because display OFF setting (SC0, SC1) and power saving mode setting (BU) are assigned to the same instruction.

(12) The instruction of power-saving mode setting is transferred. The “Control of display ON / OFF” instruction is executed. (PNC=0, SC0=1, SC1=1, BU=1)

(13) Power-off. Please input a signal of 0V into CE, CL, DI, $\overline{RES}$ and OSCI by all means to prevent the destruction of these input pads before a logic power supply (VDD) was turned off.

Additional Explanation of Peripheral Circuits

(1) About the resistors of the logic signal (OSCI, $\overline{\text{RES}}$, CE, CL and DI)

The resistors are the dumping resistance for waveform shaping. In addition, when waveform shaping is more necessary, connect a capacitor between logic input pad and VSS. (For example, from 100 to 1000 [pF])

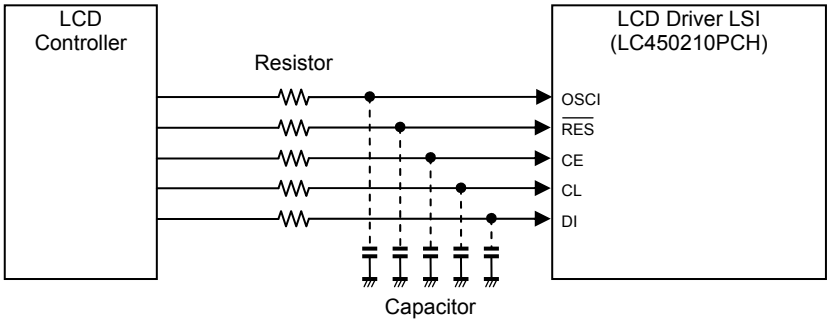


Figure 22. Peripheral circuits of the logic input signal

Also make sure that the waveform of the input signal is not heavily distorted. The following figure shows the waveform example when waveform shaping by only a resistors.

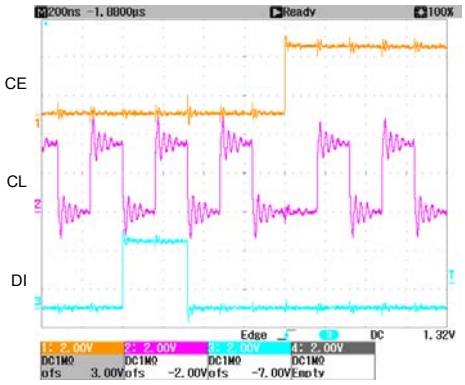


Figure 23. CCB serial data Signal (LCD controller output)

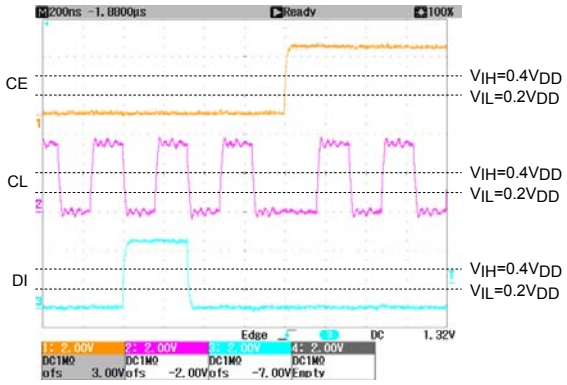


Figure 24. CCB serial data Signal (LCD Driver LSI input)

(2) About the resistors of the OSCI signal

When internal oscillator operating mode is set (OC="0"), make sure to connect OSCI to VSS. At this time, it may be connected to VSS through a pull-down resistor for the protection of the input circuit. The reason to insert a pull-down resistor are the incorrect operation by the noise, destruction with the excess voltage (the abnormal voltage of instants such as at the time of power-up), and consumption electric current reduction. If nothing inputs from the outside, the customer may be connected to the direct VSS without using the resistor, but the one that is not connected to direct VSS is safer. However, there is some demerit: parts increase, it may become weak in noise because impedance from VSS increases and there are not most of the consumption electric current reduction effects.

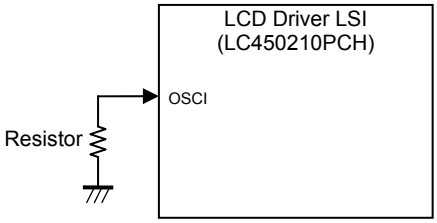


Figure 25. Peripheral circuits of the OSCI signal

(3) About the zener diode of the VBTI1

The voltage booster circuit, the contrast adjuster circuit and the LCD drive bias voltage generator circuit have the discharge circuit to discharge an electric charge of the external capacitor.

When the voltage booster is set to the discharge condition, the VLCD level is same as VBTI1 level. When the contrast adjuster and the LCD drive bias voltage generator are set to the discharge condition, the levels from VLCD0 to VLCD4 are same as VLCD5 level.

When the booster circuit was set to the discharge condition, the electric charge accumulated to the capacitors for booster circuit passes through to the VBTI1 pad. Therefore, when the impedance of the VBTI1 power supply line is high or there is not an electric discharge route (For example, the diode is inserted in series), the voltage of the VBTI1 pad may rise temporarily. In the case of the system configuration that VBTI1 and VBTI2 or VBTI1 and VDD are connected, if the absolute maximum ratings are exceeded, device functionality should not be assumed, damage may occur and reliability be affected. The measures of this case connect the zener diode to a power supply line of VBTI1, and please suppress the rise in voltage.

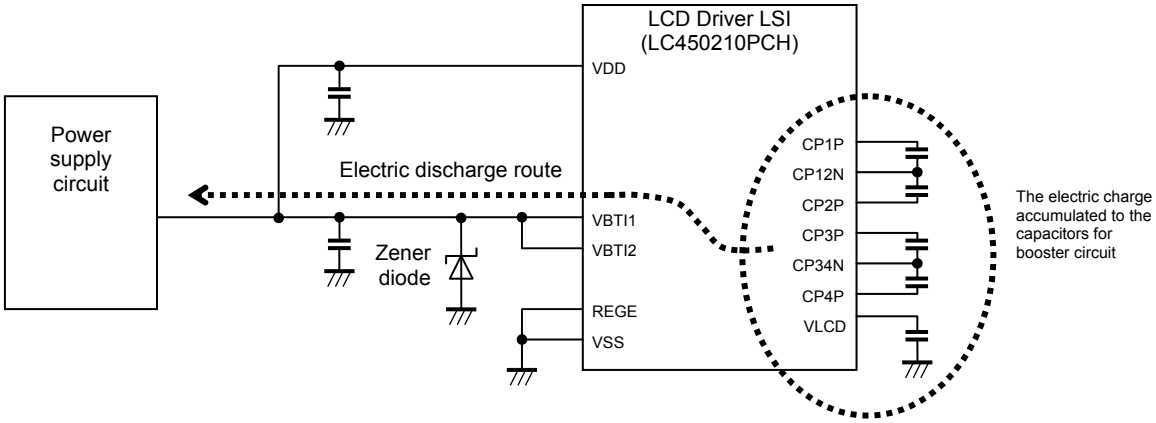


Figure 26. Peripheral circuits of the VBTI1

Application Circuit

(1) In the Case of the LCD System Configuration to Input an External Clock (300 [kHz])

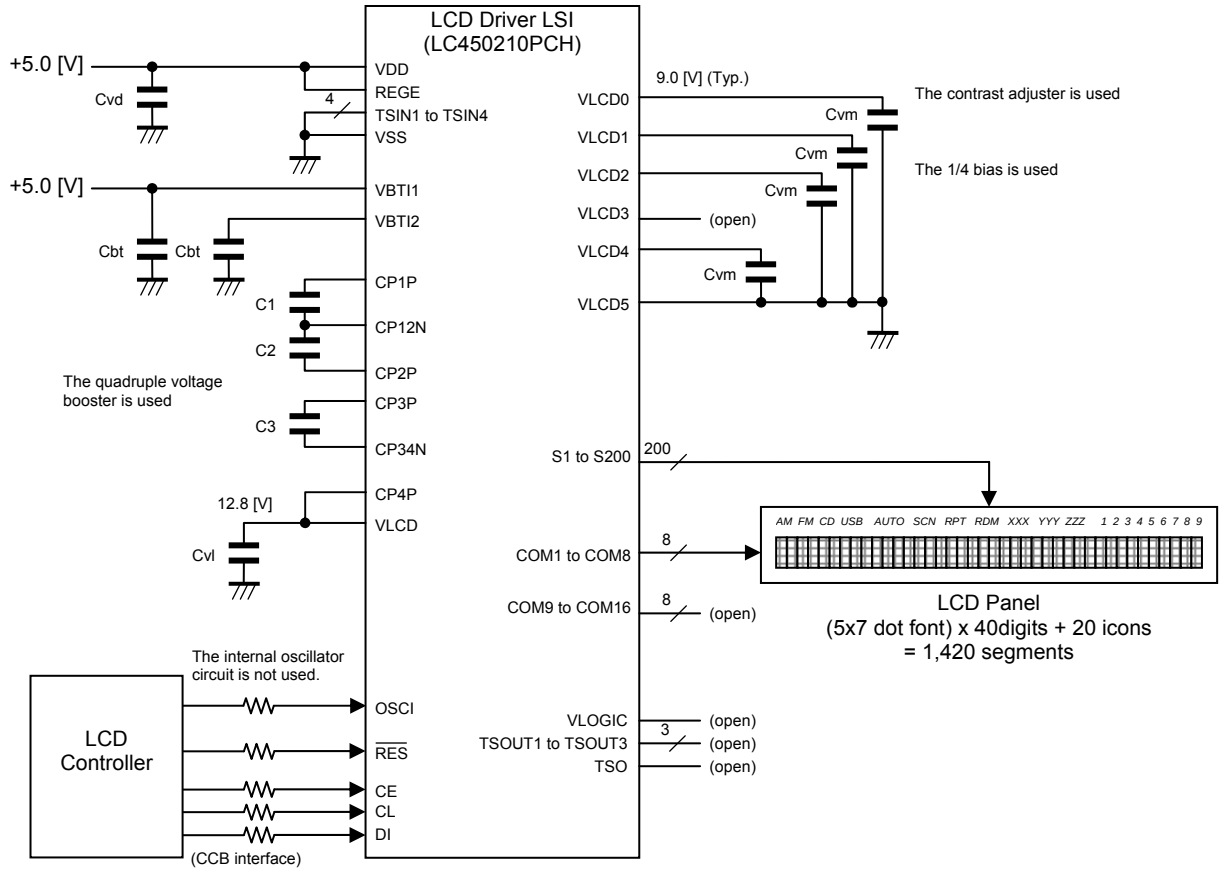


Figure 27. LCD system configuration to input an external clock (300 [kHz])

The LC450210PCH is able to set the “Internal oscillator operating mode” or “External clock input operating mode”. The reason why a customer selects the LCD system configuration using the “External clock input operating mode” is because the characteristic of the internal oscillator clock frequency (fosc) is uneven by a production variation and the terms of use of the LSI (Power supply voltage, temperature, etc.). Therefore the customer may worry about the flicker of the liquid crystal display occurring by interference with other frequency. Furthermore, there may be a customer hoping to lower clock frequency more because of the low power consumption and EMI (Electro Magnetic Interference) measures, etc.

First of all, the following table shows the pin explanation of the external clock input pin (OSCI) and the specifications of the allowable operating ranges.

Pad name	Pad function
OSCI	External clock input pad (When external clock operating mode was set) When internal oscillator operating mode is set (OC=“0”), make sure to connect OSCI to VSS. When external clock operating mode is set (OC=“1”), the OSCI is used to input the external clock.

Allowable operating ranges at Ta= -40°C to +105°C, VSS=0V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	VDD, REGE=VDD	4.5		6.3	V
		VDD, REGE=VSS	2.7		3.6	V
Input High Level Voltage	V_{IH1}	OSCI, VDD=4.5V to 5.5V (REGE=VDD)	0.5 V_{DD}		5.5	V
		OSCI, VDD=2.7V to 3.6V (REGE=VSS)	0.8 V_{DD}		3.6	V
Input Low Level Voltage	V_{IL1}	OSCI, VDD=4.5V to 5.5V (REGE=VDD)	0		0.2 V_{DD}	V
		OSCI, VDD=2.7V to 3.6V (REGE=VSS)	0		0.2 V_{DD}	V
External Clock Input Frequency	f_{ck}	OSCI, External clock input operating mode	10	300	600	kHz
External Clock Duty Ratio	D_{ck}	OSCI, External clock input operating mode	30	50	70	%

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

The following explains a setting method example of serial data in this case.

This system sets OC="1" to use the "External clock 300 [kHz] input mode"

OC	Fundamental clock operating mode	The state of OSCI
0	Internal oscillator operating mode	Make sure to connect OSCI to VSS
1	**External clock operating mode**	**Input the clock of 300 [kHz](Typ.)**

The registers from DBF0 to DBF2 can set the voltage booster clock frequency. When OC is set to "1" the following table shows the voltage booster clock frequency.

DBF0	DBF1	DBF2	Voltage Booster Clock Frequency (fcp)	The voltage booster clock frequency when fCK is 300 [kHz]
0	0	0	fCK/12	25.00 [kHz]
0	0	1	fCK/14	21.43 [kHz]
0	1	0	fCK/18	16.66 [kHz]
0	**1**	**1**	**fCK/22**	**13.63 [kHz]**
1	0	0	fCK/26	11.54 [kHz]
1	0	1	fCK/28	10.71 [kHz]
1	1	0	fCK/30	10.00 [kHz]
1	1	1	fCK/34	8.82 [kHz]

The explanation mentioned above is used only to explain internal operation and how to use the LSI, and the characteristic of the products is uneven by a production variation and the terms of use of the LSI (Power supply voltage, temperature, etc.). Therefore, the customer should always evaluate and test devices mounted in the customer's products or equipment.

The registers from FC0 to FC3 can set the LCD drive frame frequency (fo). When OC is set to "1", the following table shows the LCD drive frame frequency.

FC0	FC1	FC2	FC3	LCD drive frame frequency (fo)								
				1/8duty	1/9duty	1/10duty	1/11duty	1/12duty	1/13duty	1/14duty	1/15duty	1/16duty
0	0	0	0	fCK/4352 <68.9[Hz]>	fCK/4320 <69.4[Hz]>	fCK/4320 <69.4[Hz]>	fCK/4400 <68.2[Hz]>	fCK/4320 <69.4[Hz]>	fCK/4264 <70.4[Hz]>	fCK/4256 <70.5[Hz]>	fCK/4320 <69.4[Hz]>	fCK/4352 <68.9[Hz]>
1	0	0	0	fCK/3712 <80.8[Hz]>	fCK/3744 <80.1[Hz]>	fCK/3760 <79.8[Hz]>	fCK/3784 <79.3[Hz]>	fCK/3744 <80.1[Hz]>	fCK/3744 <80.1[Hz]>	fCK/3808 <78.8[Hz]>	fCK/3720 <80.7[Hz]>	fCK/3712 <80.8[Hz]>
0	**1**	**0**	**0**	**fCK/2944 <101.9[Hz]>**	fCK/2952 <101.6[Hz]>	fCK/2960 <101.4[Hz]>	fCK/2992 <100.3[Hz]>	fCK/2976 <100.8[Hz]>	fCK/2964 <101.2[Hz]>	fCK/2968 <101.1[Hz]>	fCK/3000 <100.0[Hz]>	fCK/2944 <101.9[Hz]>
1	1	0	0	fCK/2368 <126.7[Hz]>	fCK/2376 <126.3[Hz]>	fCK/2400 <125.0[Hz]>	fCK/2376 <126.3[Hz]>	fCK/2400 <125.0[Hz]>	fCK/2392 <125.4[Hz]>	fCK/2408 <124.6[Hz]>	fCK/2400 <125.0[Hz]>	fCK/2368 <126.7[Hz]>
0	0	1	0	fCK/1984 <151.2[Hz]>	fCK/1944 <154.3[Hz]>	fCK/2000 <150.0[Hz]>	fCK/1936 <155.0[Hz]>	fCK/1968 <152.4[Hz]>	fCK/1976 <151.8[Hz]>	fCK/1960 <153.1[Hz]>	fCK/1980 <151.5[Hz]>	fCK/1984 <151.2[Hz]>
1	0	1	0	fCK/1696 <176.9[Hz]>	fCK/1692 <177.3[Hz]>	fCK/1720 <174.4[Hz]>	fCK/1672 <179.4[Hz]>	fCK/1728 <173.6[Hz]>	fCK/1716 <174.8[Hz]>	fCK/1708 <175.6[Hz]>	fCK/1710 <175.4[Hz]>	fCK/1696 <176.9[Hz]>
0	1	1	0	fCK/1472 <203.8[Hz]>	fCK/1476 <203.3[Hz]>	fCK/1480 <202.7[Hz]>	fCK/1496 <200.5[Hz]>	fCK/1488 <201.6[Hz]>	fCK/1482 <202.4[Hz]>	fCK/1456 <206.0[Hz]>	fCK/1500 <200.0[Hz]>	fCK/1472 <203.8[Hz]>
1	1	1	0	fCK/1312 <228.7[Hz]>	fCK/1332 <225.2[Hz]>	fCK/1320 <227.3[Hz]>	fCK/1320 <227.3[Hz]>	fCK/1320 <227.3[Hz]>	fCK/1326 <226.2[Hz]>	fCK/1316 <228.0[Hz]>	fCK/1350 <222.2[Hz]>	fCK/1312 <228.7[Hz]>

FC0	FC1	FC2	FC3	LCD drive frame frequency (fo)								
				1/8duty	1/9duty	1/10duty	1/11duty	1/12duty	1/13duty	1/14duty	1/15duty	1/16duty
0	0	0	1	fCK/1184 <253.4[Hz]>	fCK/1188 <252.5[Hz]>	fCK/1200 <250.0[Hz]>	fCK/1188 <252.5[Hz]>	fCK/1200 <250.0[Hz]>	fCK/1196 <250.8[Hz]>	fCK/1204 <249.2[Hz]>	fCK/1200 <250.0[Hz]>	fCK/1184 <253.4[Hz]>
1	0	0	1	fCK/1088 <275.7[Hz]>	fCK/1080 <277.8[Hz]>	fCK/1080 <277.8[Hz]>	fCK/1100 <272.7[Hz]>	fCK/1104 <271.7[Hz]>	fCK/1118 <268.3[Hz]>	fCK/1092 <274.7[Hz]>	fCK/1080 <277.8[Hz]>	fCK/1088 <275.7[Hz]>
0	1	0	1	fCK/1056 <284.1[Hz]>	fCK/1044 <287.4[Hz]>	fCK/1040 <288.5[Hz]>	fCK/1056 <284.1[Hz]>	fCK/1056 <284.1[Hz]>	fCK/1040 <288.5[Hz]>	fCK/1036 <289.6[Hz]>	fCK/1050 <285.7[Hz]>	fCK/1056 <284.1[Hz]>
1	1	0	1	fCK/992 <302.4[Hz]>	fCK/1008 <297.6[Hz]>	fCK/1000 <300.0[Hz]>	fCK/990 <303.0[Hz]>	fCK/984 <304.9[Hz]>	fCK/988 <303.6[Hz]>	fCK/980 <306.1[Hz]>	fCK/990 <303.0[Hz]>	fCK/992 <302.4[Hz]>
0	0	1	1	fCK/960 <312.5[Hz]>	fCK/972 <308.6[Hz]>	fCK/960 <312.5[Hz]>	fCK/946 <317.1[Hz]>	fCK/960 <312.5[Hz]>	fCK/962 <311.9[Hz]>	fCK/952 <315.1[Hz]>	fCK/960 <312.5[Hz]>	fCK/960 <312.5[Hz]>
1	0	1	1	fCK/928 <323.3[Hz]>	fCK/936 <320.5[Hz]>	fCK/920 <326.1[Hz]>	fCK/924 <324.7[Hz]>	fCK/936 <320.5[Hz]>	fCK/936 <320.5[Hz]>	fCK/924 <324.7[Hz]>	fCK/930 <322.6[Hz]>	fCK/928 <323.3[Hz]>
0	1	1	1	fCK/896 <334.8[Hz]>	fCK/900 <333.3[Hz]>	fCK/900 <333.3[Hz]>	fCK/902 <332.6[Hz]>	fCK/888 <337.8[Hz]>	fCK/884 <339.4[Hz]>	fCK/896 <334.8[Hz]>	fCK/900 <333.3[Hz]>	fCK/896 <334.8[Hz]>
1	1	1	1	fCK/864 <347.2[Hz]>	fCK/864 <347.2[Hz]>	fCK/860 <348.8[Hz]>	fCK/858 <349.7[Hz]>	fCK/864 <347.2[Hz]>	fCK/858 <349.7[Hz]>	fCK/868 <345.6[Hz]>	fCK/870 <344.8[Hz]>	fCK/864 <347.2[Hz]>

The value of "< >" is an LCD drive frame frequency when fCK is 300 [kHz]. The explanation mentioned above is used only to explain internal operation and how to use the LSI, and the characteristic of the products is uneven by a production variation and the terms of use of the LSI (Power supply voltage, temperature, etc.). Therefore, the customer should always evaluate and test devices mounted in the customer's products or equipment.

The setting method about the registers except the above is the same as "Explanation of the Internal Circuit Control", "Explanation of the LCD Drive Control" and "Explanation of How to Write a Display Data RAM".

(2) In the case of an LCD system to compose of only the 3.3V power supply

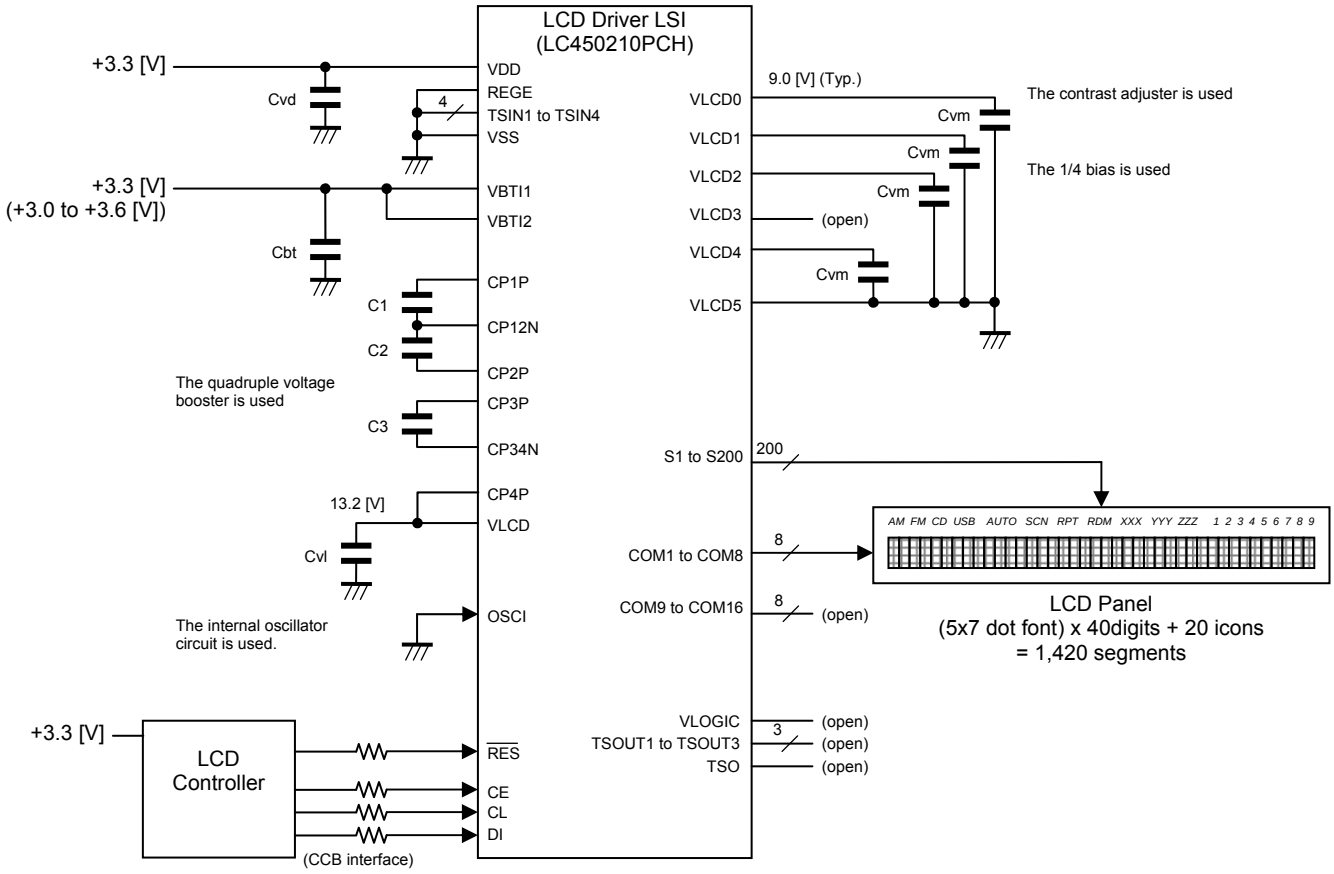


Figure 28. LCD system to compose of only the 3.3V power supply

This LCD system configuration example sets DBC="1", CTC0="1" and CTC1="1" to use the all circuits (voltage booster circuit, contrast adjuster circuit and LCD drive bias voltage generator circuit).

The control data from CT0 to CT5 can set the LCD drive bias voltage (VLCD0) using the contrast adjuster circuit. However, satisfy a condition of VLCD0 ≤ VLCD - 2.4[V]. This LCD system configuration example sets CT0="0", CT1="1", CT2="0", CT3="0", CT4="0" and CT5="1" to use the LCD drive bias voltage (VLCD0) as 9.00 [V].

When VBTI1=VBTI2=3.3 [V], REGE=VSS, quadruple voltage booster and contrast adjuster are used, LCD power supply voltage (VLCD) becomes 13.2 [V] that quadrupled the VBTI2 input of 3.3 [V] (Typical allowable operating range). In addition, when the VBTI2 input of 3.6 [V] (Maximum allowable operating range), the VLCD is 14.4 [V]. Moreover, when the VBTI2 input of 3.0 [V] (The voltage that subtracted a change of 0.3 [V] from the 3.3 [V] voltage), the VLCD is 12.0 [V]. The customer can select from step 30 (9.60 [V]) to step 63 (4.65 [V]) at the time of this setting state. When these are set from step 0 (14.10 [V]) to step 29 (9.75 [V]), the VLCD0 voltage is not guaranteed.

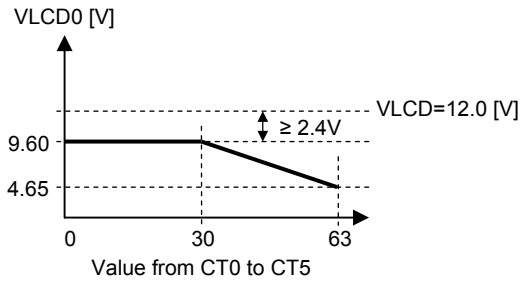


Figure 29. Adjustment range of the LCD drive bias voltage (VLCD0)

Table 11. Setting of settable contrast adjustment

Step	CT0	CT1	CT2	CT3	CT4	CT5	VLCD0 voltage
0	0	0	0	0	0	0	not guaranteed
1	1	0	0	0	0	0	not guaranteed
2	0	1	0	0	0	0	not guaranteed
3	1	1	0	0	0	0	not guaranteed
4	0	0	1	0	0	0	not guaranteed
5	1	0	1	0	0	0	not guaranteed
6	0	1	1	0	0	0	not guaranteed
7	1	1	1	0	0	0	not guaranteed
8	0	0	0	1	0	0	not guaranteed
9	1	0	0	1	0	0	not guaranteed
10	0	1	0	1	0	0	not guaranteed
11	1	1	0	1	0	0	not guaranteed
12	0	0	1	1	0	0	not guaranteed
13	1	0	1	1	0	0	not guaranteed
14	0	1	1	1	0	0	not guaranteed
15	1	1	1	1	0	0	not guaranteed
16	0	0	0	0	1	0	not guaranteed
17	1	0	0	0	1	0	not guaranteed
18	0	1	0	0	1	0	not guaranteed
19	1	1	0	0	1	0	not guaranteed
20	0	0	1	0	1	0	not guaranteed
21	1	0	1	0	1	0	not guaranteed
22	0	1	1	0	1	0	not guaranteed
23	1	1	1	0	1	0	not guaranteed
24	0	0	0	1	1	0	not guaranteed
25	1	0	0	1	1	0	not guaranteed
26	0	1	0	1	1	0	not guaranteed
27	1	1	0	1	1	0	not guaranteed
28	0	0	1	1	1	0	not guaranteed
29	1	0	1	1	1	0	not guaranteed
30	0	1	1	1	1	0	9.60 V
31	1	1	1	1	1	0	9.45 V
32	0	0	0	0	0	1	9.30 V
33	1	0	0	0	0	1	9.15 V
34	**0**	**1**	**0**	**0**	**0**	**1**	**9.00 V**
35	1	1	0	0	0	1	8.85 V
36	0	0	1	0	0	1	8.70 V
37	1	0	1	0	0	1	8.55 V
38	0	1	1	0	0	1	8.40 V
39	1	1	1	0	0	1	8.25 V
40	0	0	0	1	0	1	8.10 V
41	1	0	0	1	0	1	7.95 V
42	0	1	0	1	0	1	7.80 V
43	1	1	0	1	0	1	7.65 V
44	0	0	1	1	0	1	7.50 V
45	1	0	1	1	0	1	7.35 V
46	0	1	1	1	0	1	7.20 V
47	1	1	1	1	0	1	7.05 V
48	0	0	0	0	1	1	6.90 V
49	1	0	0	0	1	1	6.75 V
50	0	1	0	0	1	1	6.60 V
51	1	1	0	0	1	1	6.45 V
52	0	0	1	0	1	1	6.30 V
53	1	0	1	0	1	1	6.15 V
54	0	1	1	0	1	1	6.00 V
55	1	1	1	0	1	1	5.85 V
56	0	0	0	1	1	1	5.70 V
57	1	0	0	1	1	1	5.55 V
58	0	1	0	1	1	1	5.40 V
59	1	1	0	1	1	1	5.25 V
60	0	0	1	1	1	1	5.10 V
61	1	0	1	1	1	1	4.95 V
62	0	1	1	1	1	1	4.80 V
63	1	1	1	1	1	1	4.65 V

The explanation mentioned above is used only to explain internal operation and how to use the LSI, and the characteristic of the products is uneven by a production variation and the terms of use of the LSI (Power supply voltage, temperature, etc.). Therefore, the customer should always evaluate and test devices mounted in the customer's products or equipment.

The setting method about the registers except the above is the same as "Explanation of the Clock Control", "Explanation of the Internal Circuit Control", "Explanation of the LCD Drive Control" and "Explanation of How to Write a Display Data RAM".

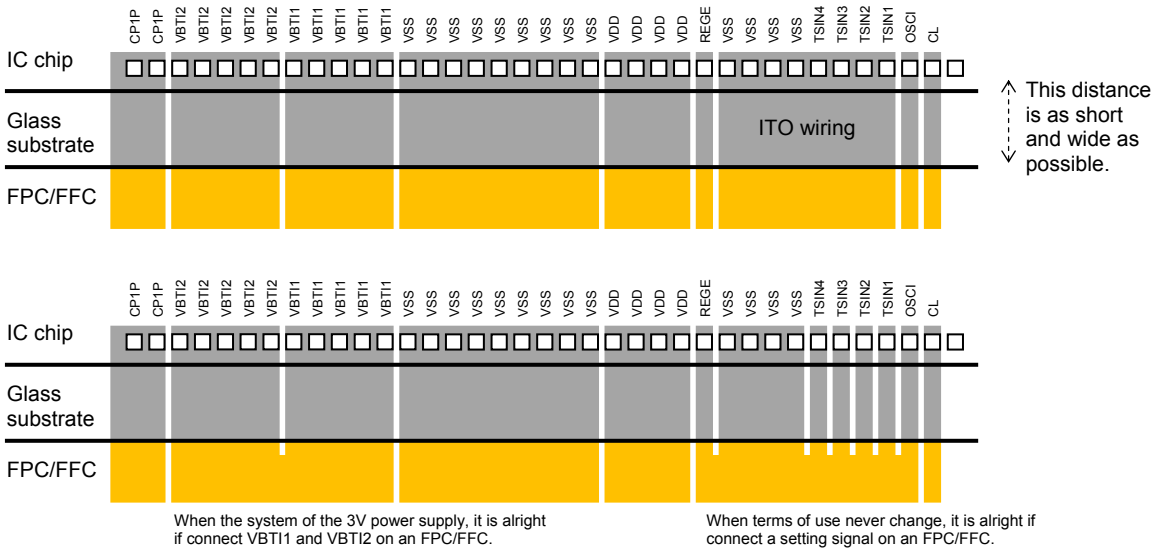
Caution of the ITO Wiring Design

Caution of the ITO wiring design is provided as follows for the stable operation of this LSI. In reference to these, it is necessary to design an application or the set, in consideration of an LCD specification and condition.

Design the ITO line of a power supply and the voltage booster signal as short and wide as possible, because it is necessary to minimize the parasitic resistance of the ITO line. Particularly, in the case of the COG (The LSI chip is mounted on glass substrate), minimize the resistance of ITO lines from the pad of the LSI to FPC/FFC. In addition, connect the PAD between the adjacent same signals (However, the DUMMY pad is excluded) at the outside of the LSI.

The following figure shows the design example of the ITO wiring.

(1) Good wiring example



(2) Bad wiring example