AND9078/D

Designing with and Testing the NCN5192 DAC

ON Semiconductor®

APPLICATION NOTE

Introduction

The NCN5192 HART modem integrates a 16 bit DAC to simplify analog current−loop implementation for a HART slave device. In this application note, we will look in detail at the DAC itself, how to design your application to achieve the 16 accuracy and how to test it.

NCN5192 DAC Topology

The build−in DAC in the NCN5192 HART modem is a 16 bit sigma−delta DA convertor. In practice, this means that the output of the filter is a pulse−width modulated signal that first needs to pass through a low−pass filter to get a useful analog value. This low−pass filter must be designed with a corner frequency chosen according to the desired bandwidth. The higher the corner frequency of the low pass filter, the more switching noise gets through, and hence, the less accurate the output value will be. Choosing a lower corner frequency implies that the output will respond slower to change in the DAC code. This means that a longer settling time must be taken into account before measurements can be made.

The sigma−delta modulator is build to achieve 16 bit accuracy with a bandwidth of 10 Hz or less, which corresponds with the desired analog signal bandwidth.
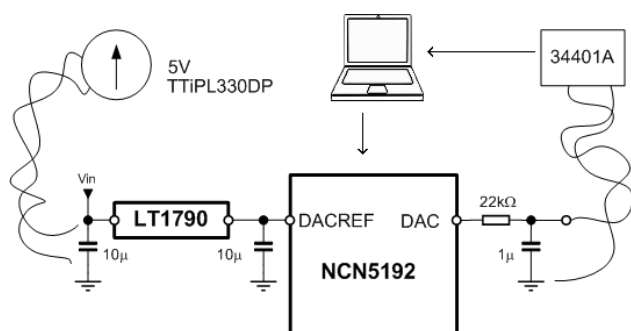

Figure 1. Measurement Setup

Noise Sources and Design Tips

Next, let's look at different sources of noise in the DAC and how to avoid them.

The most important noise source is the DAC reference voltage (DACREF). This voltage is used to generate the high level of the DAC. That means that, during the on time of the PWM output signal, the output is connected directly to DACREF, and any noise present on this signal is coupled directly through to the output. This will result in noise that is proportional with the code applied to the DAC. To achieve 16 bit accuracy it is critical that the DACREF pin is connected to a separate reference signal. If accuracy is not a requirement for your design, you can connect DACREF to AREF or even to VDD. However, when the 16 bit accuracy is required, these signals − or any other shared reference voltages − are generally too noisy to be used for this purpose. Even the slightest dip or peak can result in non−linearity because the least significant bit (LSB) has an order of magnitude of only ~20 μV. When designing the circuit around the NCN5192 for high accuracy, take care to select a reference generation with high bandwidth feedback loop and high supply noise rejection ratio. Also take care to decouple this reference signal close to the IC with high capacitance (1 − 10 μF) and to keep the traces away from other high−frequency signals that might couple over.

Test Setup

To test the DAC in a real−world situation, we have modified a NCN5192 evaluation board to accommodate the above advice. The NCN5192 evaluation board normally has DACREF connected to the VDD of the board. This is done because in the average HART/current loop application accuracy is not critical. This means that using the NCN5192 evaluation board "as is" will results in a loss of several bits accuracy.

We have modified the board to include a second 3V3 regulator (LT1790) as the source of DACREF. This reference is decoupled with a 10 μF capacitor at the IC pin. The DAC output pin is connected to a first−order RC filter with a corner frequency at 7 Hz (22 kΩ, 1 μF). The voltage over the capacitor is measured by an Agilent 34401A benchtop multimeter. Connection to the multimeter is done over twisted cables to reduce interference from radiated disturbers. In a noisy environment, using shielded twisted pair (STP) can improve the measurements even more. After

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setting the DAC code, the test program waits 10 seconds before capturing a measurement sample, to make sure the signal is fully settled, and no timing issues occur.

The board itself is powered by a benchtop linear regulated power supply (TTi PL330DP) to minimize noise on the VDD voltage coupling trough to the DAC output. To achieve even better measurements battery powered operation can be considered. However, we found that using a benchtop power supply achieves enough accuracy to demonstrate the DAC capabilities.

Calculations

After taking the measurements, some calculations are needed to acquire meaningful figures on the DAC performance.

Since we like to control the DAC in a linear way, we will first determine the best first−order approximation of the measured values. This is done through a least−square algorithm, giving two coefficients that best fit the following relation, where n is the input code:

$$V_{DAC, lin}(n) = a * n + b$$
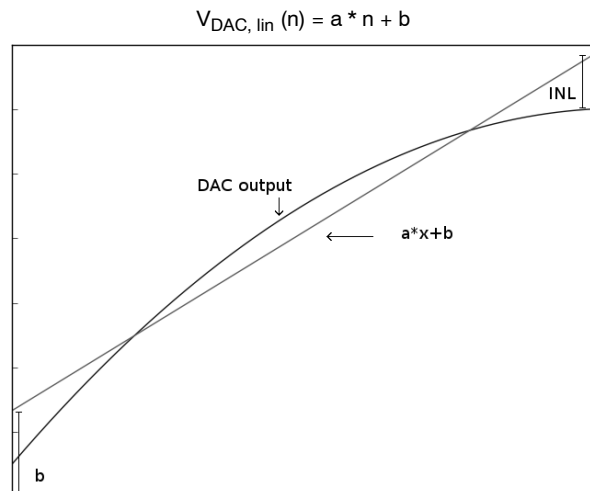
Figure 2. DAC Output and Linear Approximation

In the context of a DAC we also call the coefficient a the step size, or least significant bit (LSB). The coefficient b is called the offset and is usually expressed in LSB.

To account for the non−linearity of the DAC the following figures of merit are used: integral non−linearity (INL) and differential non−linearity (DNL).

These are defined as follows:

$$INL = max\left(\left|V_{DAC,meas}(n) - V_{DAC,lin}(n)\right|\right)$$

$$DNL = \left|\frac{max\left(V_{DAC,meas}(n) - V_{DAC,meas}(n-1)\right)}{LSB} - 1\right|$$

Test Results

Table 1 summarizes the test results for the different modes of operation of the NCN5192. The NCN5192 can work in 14 and 16 bit mode. There is no actual difference in

implementation between the two modes. When operating in 14 bit mode, the NCN5192 simply adds two least significant zeros to the input code.

The output of the DAC can also be set to return to zero (RTZ) or non−RTZ. This is important when the rise and fall time of the signal are not identical. This will cause a DC offset depending on the number of rising and falling edges. As the output bits of a sigma−delta modulator are randomly arranged (ie. for the same setting we could get 01110000 or 01010100), the number of edges might vary over time for a non return to zero signal. Setting the DAC to "return to zero" forces the output to have a rising and falling edge for each logic "1" bit, so that no offset from pulse asymmetry can occur.
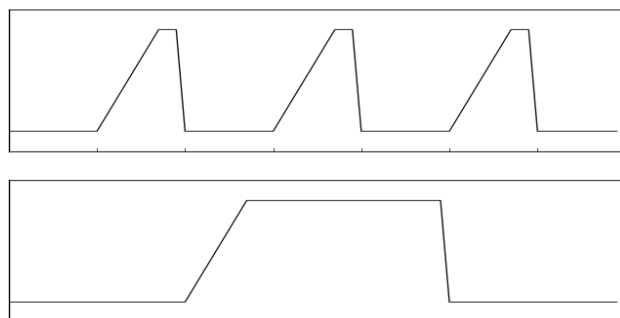
Figure 3. Effect of Asymmetrical Edges on RTZ Mode (top) and nRTZ Mode (bottom)

However, this will decrease the range of the modulator to 50% of DACREF, as the maximum duty cycle is 50% instead of 100% for nRTZ.

Table 1. TEST RESULTS

Mode	LSB	Offset	INL	DNL
14 bit, nRTZ	201.07 μV	2.90 bit	0.93 bit	0.21 bit
14 bit, RTZ	100.58 μV	5.11 bit	0.92 bit	0.22 bit
16 bit, nRTZ	50.25 μV	3.19 bit	0.87 bit	0.54 bit
16 bit, RTZ	25.14 μV	5.76 bit	0.83 bit	0.73Bit

Figures 4 − 7 show the DNL over the different codes for the four modes of operation. These graphs clearly show that the DNL rises with the input code. This is a sign that the main noise source is noise on the power supply. Reducing power supply noise further can still improve the measurements. We also see that the RTZ graphs have higher DNL for the lower codes compared to the nRTZ graphs. This is because in RTZ the LSB is smaller, and hence, closer to the noise floor.

In these measurements, the RTZ gives a similar or worse result than the nRTZ. This is a clear indication that there is no edge asymmetry in the test setup. Because the RTZ LSB is smaller than the nRTZ, the performance is more affected by noise, hence the worse performance on 16 bits.

Conclusion

When designing with these guidelines in mind, the full accuracy of the NCN5192 DAC can be achieved, as shown in the experimental results. When your design has asymmetrical edges on the DAC output signal, RTZ mode might be interesting. Otherwise, nRTZ will likely be the most interesting as larger LSB size decreases power supply noise sensitivity.
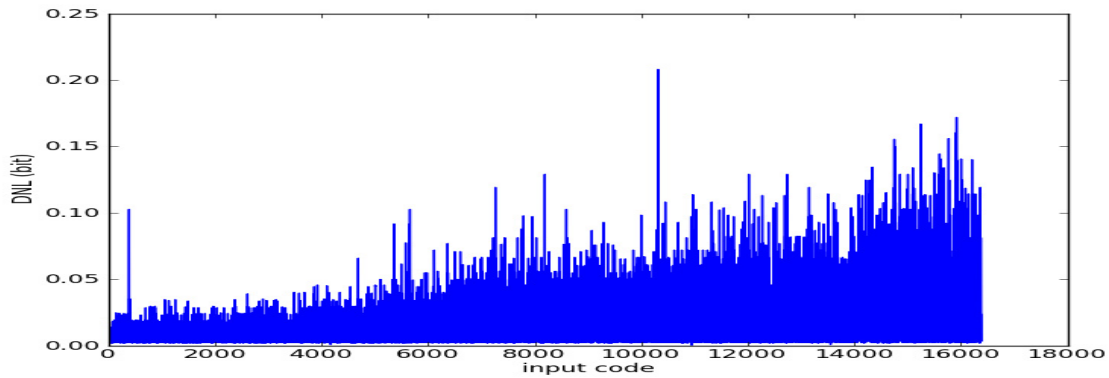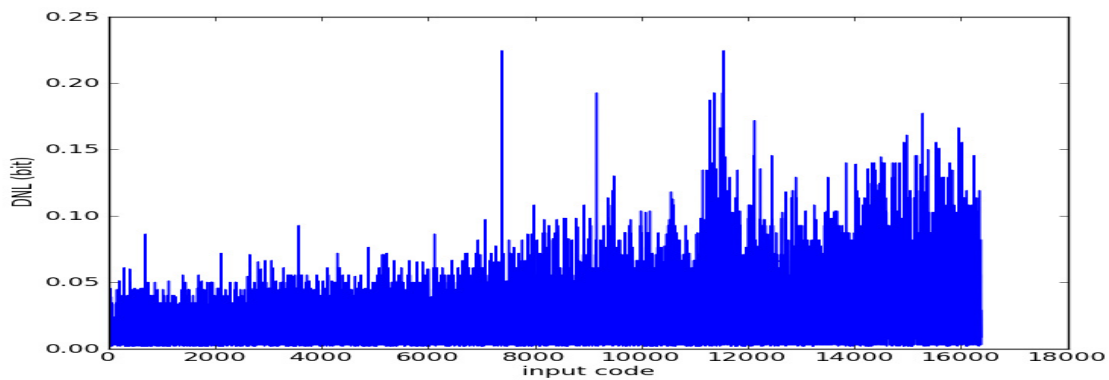
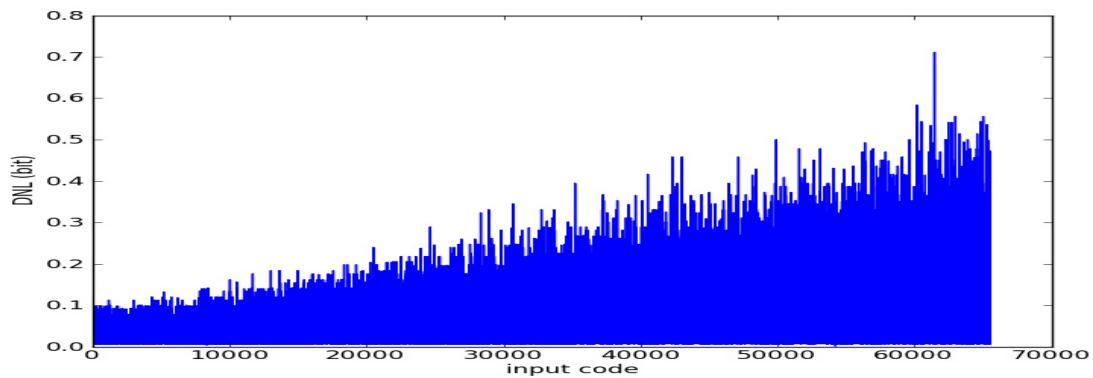

Figure 4. 14 bit nRTZ

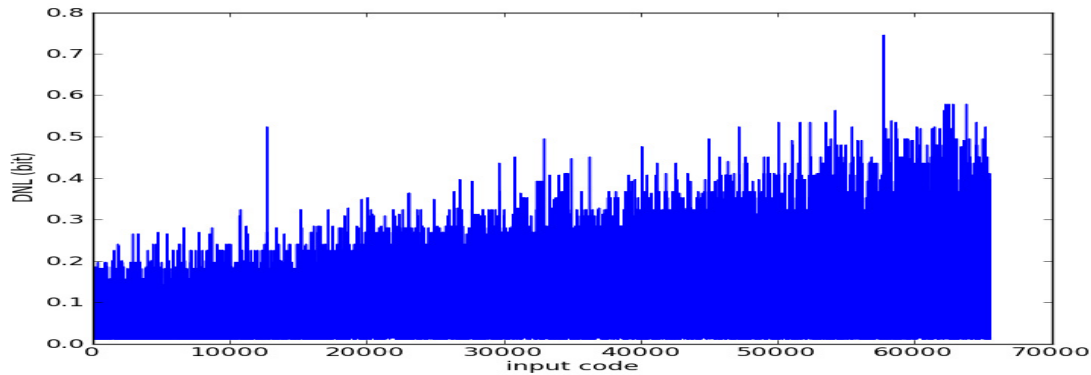**Figure 5. 14 bit RTZ**

Figure 6. 16 bit nRTZ

Figure 7. 16 bit RTZ